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The AppliedMicro S28010 PHY Gearbox Mux/Demux enables 100Gbps client interfaces for optical links up to 40km over single-mode fibre. The flexible design can be used within CFP-compliant MSA optical modules or on high-performance line-cards with CFP2 optical modules. The CMOS architecture offers a low-power solution without compromising performance. The PHY connects 10-lanes at 10-Gbps to 4-lane optical assemblies at 25Gbps for 100G Ethernet and other direct-detect applications.

Features
- Single-chip integrated bi-directional 100G transceiver for direct-detect applications
- CAUI and OTL-4.10 compliant 10-lane system interface operates from 10.3Gbps to 11.22 Gbps
- 100GBASE-R4 and OTL-4.4 compliant client interface supports:
  - 100GBASE-R4 at 25.78125 Gbps
  - OTU4 at 27.95 Gbps
  - 32G Fibre Channel at 28.05 Gbps
- Transmit buffer pre- and post-cursor emphasis (0 – 6dB)
- Programmable 28Gbps output voltage to 800mVppd
- 40mVppd minimum input sensitivity on 28Gbps client interface with integrated peaking and limiting amp
- Internal 100Ω termination on CML inputs
- Reference clock at 1/16th or 1/64th the system interface rate
- Recovered receive clock for syncE applications
- Support for optional external VCXO or frequency synthesizer
- Optional independent Rx Reference clock input
- MDIO interface to host controller
- I2C interface to external EEPROM
- LOS inputs from optical detectors
- Compatible with IEEE802.3bf Time Sync/ IEEE-1588
- Integrated network and system loopbacks
- Integrated PRBS generator/checkers

Reducing Power and Enabling Bandwidth
The 100G PHY Gearbox from AppliedMicro targets CFP and CFP2 multi-source agreement compliant modules for direct-detect client-side applications. The 100G PHY Gearbox incorporates proven AppliedMicro expertise in electronic equalization to extend reach and improve performance while minimizing power. The gearbox interfaces seamlessly to 28Gbps ROSA and TOSA assemblies for 1310nm (nom) optical media. Equalization can be extended to compensate for impairment associated with CFP2 electrical connectors.

The fully integrated multiplexer and demultiplexer is compliant with OTU-4.4, 32G Fibre Channel and IEEE802.3 standards. In the transmit direction, the Gearbox accepts 10-lanes at (nominally) 10Gbps and performs per-lane clock and data recovery. Data is demultiplexed into twenty virtual lanes and multiplexed into 4 physical lanes at 28Gbps (nominally). Output data is gated by the Tx reference clock to attenuate jitter.

In the receive direction, data from the external optical detectors is recovered in clock and data recovery circuits, demultiplexed into 20 virtual lanes and then multiplexed into 10 physical lanes. The optional Rx reference clock input can be used to center the CDR circuits.

System and client side loopbacks and PRBS generators/checkers are included for diagnostic purposes offering designers a feature-rich, state-of-the-art product in a small package outline.
## Specifications

### CAUI Interface
- Operates from 10.3 Gbps to 11.22 Gbps

### Line Interface
- Operates from 25.7 to 28.1 Gbps

### Transmit Equalization
- 3-Tap FIR driver on 28Gbps output

### Receive Equalization
- CTLE equalization on receiver compliant with OIF-28G-SR and VSR

### Case Temperature Range
- -40°C to +85°C

### Power Supply
- 0.9V (core), 1.2 V and 2.5V (I/O)

### Packaging
- FC-CBGA, 17x17mm with 1.0mm pitch
- RoHS6/6 compliant

## Applications
- CFP Modules
- 100GBASE-LR4 and -ER4 client interfaces
- Data centers
- Core Routers

## APM Support
AppliedMicro offers an evaluation kit for product evaluation and for early software development.