OC-12 AAL5 SAR

PortMakerI firmware provides proven, reliable and fully supported binary applications for the MXT4400 Traffic Stream Processor. The ATM Adaptation Layer 5 (AAL5) application provides a uni-directional OC-12 throughput ITU I.363.5 SAR, traffic shaping and a rich set of other features.

AAL5 Segmentation and Reassembly (SAR)

The PortMakerI AAL5 firmware application complies with the ITU I.363.5 standard, and also conforms to the ATM Forum PICS Proforma for the AAL Type 5 tests. The firmware provides OC-12 throughput with 64K connections in uni-directional mode (i.e., two chip solution). It can also be configured in a bi-directional mode (i.e., one chip solution) with 2xOC-3 throughput and 32K connections. ATM cell traffic uses the Utopia interface on the MXT4400, while packet traffic can use either the Utopia/PDS interface for streaming mode operation, or the PCI bus for shared memory operation. Host based management of the SAR is accomplished via the PCI bus using commands, acknowledgements, indications and alarms.

Traffic Shaping

Traffic shaping is provided at the output of the segmentation function. Each connection has two Generic Cell Rate Algorithms (GCRAs) that support the CBR.1, VBR.1, UBR.1 and UBR.2 conformance definitions in the ATM Forum Traffic Management 4.1 Specification. The host selects the shaping parameters and priority on a per VC basis at open channel time. A four-level, strict priority, scoreboard based mechanism is used to schedule cells for transmission, allowing quality of service (QoS) level guarantees. Shaping rates are available from 0.006% to 100% of line rate, with 1% accuracy.

KEY FEATURES

- Uni-directional OC-12 throughput
- ITU I.363.5 compliant AAL5 SAR
- ATM Forum TM 4.1 traffic shaping
- Traffic shaping rates configurable from 0.006% to 100% of line rate, with 1% accuracy
- Supports 64K connections
- Supports up to 16 PHYs
- Choice of segmenter queue admission policies:
  - Random Early Detection (RED)
  - Per VC flow control
  - Per VC Early Packet Discard (EPD)
- Per VC queuing
- VP Tunnels (with shaping)
- Encapsulation/De-encapsulation
- Reassembly time-out
- Support for OAM and raw cells (AAL0)
- Per PHY and per connection statistics
- Host routing for control packets
- LANE LECID echo cancellation
- LAN FCS generation and checking
- Host control via PCI bus and software API
Buffer Management
Two pools of buffers are supported: internal buffers and host buffers. Internal buffers occupy local SDRAM and are 64 bytes in length. Internal buffers are allocated to one of 15 buffer classes during initialization. Host buffers are configurable in size and can be placed either in local SDRAM or in host memory on the PCI bus. Host buffers are optionally used for packets output from the reassembler, when the shared memory mode of operation is used. Up to 256 Mbytes of local SDRAM are supported for both internal and host buffers, as well as channel context.

Congestion Control
Segmenter Packets are stored in per VC queues. Queue admission is controlled by one of three methods selected at open channel time: 1) Random Early Detection (RED), 2) per VC flow control, or 3) per VC Early Packet Discard (EPD). The RED algorithm discards packets in a manner that optimizes the overall network performance of TCP/IP connections. Four sets of RED parameters are supported, selected on a per channel basis. The per VC flow control option sends indications to the host when a configurable high and low threshold are crossed (with hysteresis). Per VC EPD is similar to flow control except that packets are dropped when the high threshold is exceeded, and no indications are sent.

Statistics
The segmenter provides the following per-channel counters: cells transmitted, packets transmitted and packets discarded. The segmenter provides the following per-port counters: packets received, packets discarded [8 separate error counters] and cells transmitted.

The reassembler provides the following per-channel counters: cells received, packets received, packets discarded. The reassembler provides the following per-port counters: cells received and packets discarded [12 separate error counters] and packets transmitted.

Memory Requirements
The PortMaker AAL5 application supports up to 256 Mbytes of SDRAM used for data buffers and context. A typical configuration consists of 16 Mbytes of SDRAM, with larger memories providing additional data buffers if required by the application. 1 Mbyte of SRAM is required for program storage.

Applications
The PortMaker AAL5 firmware is intended for use in enterprise, aggregation, edge and core routers, multi-service edge switches, optical edge equipment and DSLAMS. Two typical applications using the MXT4400 running PortMaker AAL5 firmware are shown at right.

Development Tools
TSP SimMaker provides hardware simulation models (SWIFT and Verilog), test benches, bus functional models, IBIS models and a reference design. Reference code is provided to facilitate host application integration. A comprehensive set of diagnostics is provided to assist with testing.
Uni-directional (two chip) Block Diagram

Bi-directional (one chip) Block Diagram
Product Features

Functions
- ITU I.363.5 AAL5 SAR
- OC-12 throughput
- 64K uni-directional connections per chip
- Supports up to 16 PHYs
- Traffic Shaping - dual GCRA per connection
- Supports the following traffic shaping conformance definitions:
  - CBR.1
  - VBR.1
  - UBR.1
  - UBR.2
- VP Tunnels with WRR access
- Congestion Control:
  - Random Early Detection (RED)
  - Per VC flow control
  - Per VC Early Packet Discard (EPD)
- Reassembly time-out
- Encapsulation/De-encapsulation
- Support for OAM and raw cells (AAL0)
- Host control via PCI bus
- Host routing for control packets
- LANE LECID echo cancellation
- LAN FCS generation and checking
- Per channel and per port statistics
- Memory Requirements (per MXT4400)
  - 16 to 256 Mbytes of SDRAM
  - 1 Mbyte of SRAM

See the MXT4400 data sheet for a description of the hardware interfaces and device characteristics.

Ordering Information
- MXA-ptsar-bn