**M853xx Known Issues**

**Products Affected:** M85373G-13/M85374G-13/M85375G-13/M85376G-13

This document describes the known issues with the M853xx devices.

**Sync Mode Issue**

**Background**

- The Sync mode bootstrap is EXP_A_3 on the M853xx parts. Sync mode is enabled when this bootstrap is pulled high at boot. Async mode is enabled when the bootstrap is low.
- Sync mode controls the timing of the ARM interface to the internal bus and peripherals. In Sync mode, the bus and peripherals are clocked on a multiple of the system clock. In Async mode, the timing is controlled by handshake.

**Issue description**

The internal System Watchdog and Global and Functional Software Resets will no longer be supported for all M853xx devices when operating in Sync mode.

**Workaround**

An external Watchdog/Master Reset device (controlled via GPIOs, driving the Hardware Reset pin) is recommended.

**GPIO Unknown Initial State After Device Power-Up**

**Description**

The general purpose input output (GPIO) signals may not be in tri-state mode following power-up if the system clock does not toggle before the VCore power supply comes up.

GPIOs are expected to be pulled high by an internal pull-up resistor after reset is released, but if the system clock does not toggle before VCore rises, they may be driven low until they are initialized by software. If a GPIO is used to drive an external master reset device, the board may not come out of reset.

**Workaround**

Either design the board's power-up sequence so that the system clock toggles before VCore rises, or insert a DC-blocking capacitor followed by a pull-up resistor in series with a GPIO that is used to drive an external master reset part.

Once software has initialized the GPIO control registers, they will behave normally.
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