

M08045

DEVICE OVERVIEW

3G/HD/SD Serial Digital Video Reclocker

The M08045 is a serial digital video reclocker with integrated trace equalization, automatic rate detect (ARD) circuitry, and a 4:1 mux at the input. It operates at data at 2.97 Gb/s, 1.485 Gb/s, and 270 Mb/s. The device has an input jitter tolerance (IJT) of greater than 0.6 unit intervals (UI) and can provide retimed serial outputs with very low output jitter. The reclocker requires a single, external, 27MHz crystal, which is used as the reference clock for all four channels. It includes per lane analog input equalization for up to 40" of FR4 trace and two connectors in addition to output de-emphasis.

This device features integrated supply regulators, allowing it to be powered from 1.2V, 1.8V, 2.5V, or 3.3V supply voltages. When operating at 1.2V, it consumes only 230mW. Furthermore, the power rails for the core, input, and output circuitry are electrically independent thus may be connected to different voltage rails on the board. This feature enables the M08045 to be DC coupled to any upstream or downstream device regardless of its input/output voltage level.

The 4:1 mux at the input allows any of the 4 inputs to be routed to the integrated reclocker and its output. The device, and the input mux, may be configured by setting the internal registers through standard two-wire and four-wire interfaces. Optionally, the reclocker may be configured at power-up through an external EEPROM device. Limited configuration through hardware pin settings is also available.

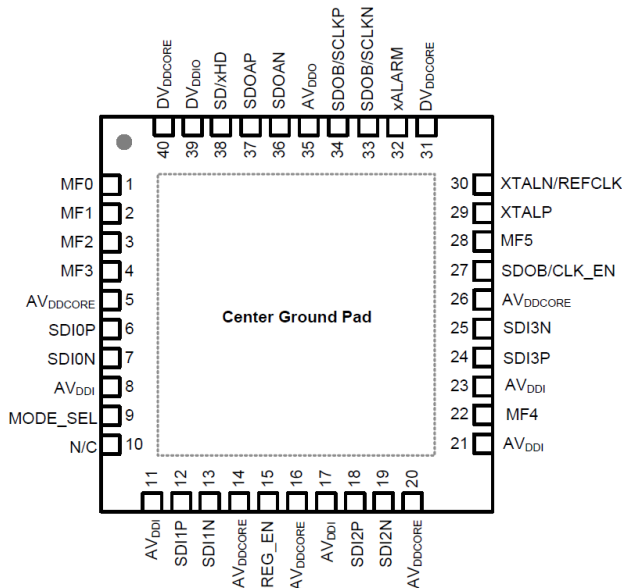


Figure 1 – M08045 Pin-out diagram



M08045

Serial Digital Video
Reclocker for
2.97 Gb/s,
1.485 Gb/s,
and 270 Mb/s
data rates

> Applications

- Digital Video Recorders (DVR)
- Video Mixers and Switchers
- Surveillance / CCTV Cameras
- Industrial and Professional Cameras
- Digital Image Transfer / Capture Devices
- Distribution Amplifiers
- Repeaters

Features	Benefits
0.6 UI input jitter tolerance	Enable robust, error free designs
Optimized data rates at 270 Mb/s, 1.485 Gb/s, and 2.97 Gb/s	Single Chip Solution for multiple data rates
Integrated 50Ω input termination	Saves board area and enable high density designs
4:1 input multiplexer	Enables high density designs, flexibility, low cost
Input equalization up to 40" of FR4 trace and 2 connectors, and output de-emphasis	Ease of high speed design and layout
Integrated regulators extending operation from 1.2V to 3.3V	Reduces number of power rails required on board
Electrically isolated input, output, and core supply rails	Allows DC interface which saves board area and cost
Automatic and manual modes for rate indication and selection	Ease of use and flexibility
Loss of lock (LOL), Loss of signal (LOS), and data rate indication	Ease of status update and diagnostics
Low power dissipation (230mW at 1.2V)	Low power and thermal management costs
Small form factor and foot print (6x6 mm ² , 40-pin QFN package)	Industry standard package
Industrial operating temperature range: -40°C to +85 °C	Provides higher tolerance and additional design margin

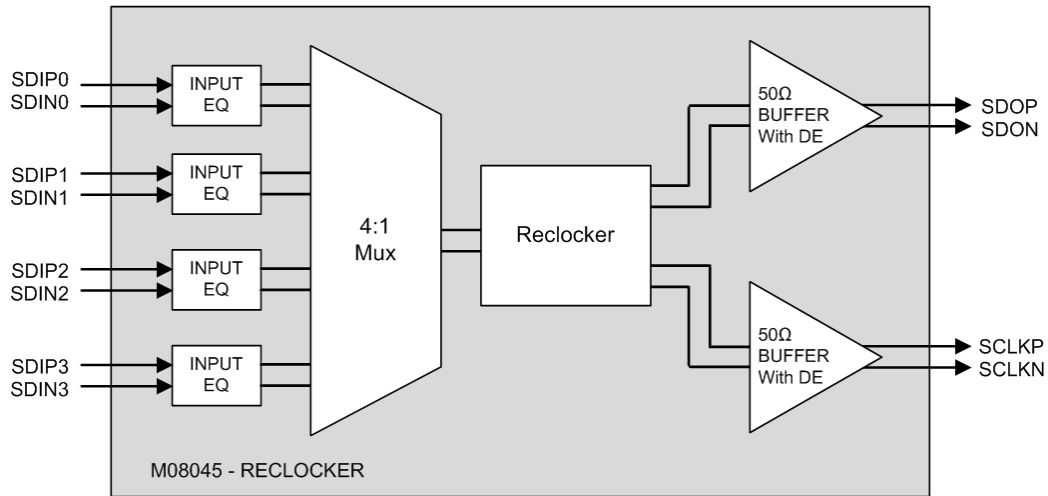


Figure 2 – M08045 Functional Block Diagram

Package (RoHS Compliant)

- 6x6 mm², 40-pin QFN



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