T1/E1 Framer and Line Interface

Bt8370/8375/8376

Fully Integrated T1/E1 Framer and Line Interface

Conexant’s Bt8370 provides OEMs with a fully-featured single chip framer and line interface implementation for T1/E1 and Integrated Service Digital Network (ISDN) primary rate interfaces operating at 1.544 Mbps or 2.048 Mbps.

By combining a sophisticated framer and transmit/receive slip buffers with an on-chip short/long-haul physical line interface, the Bt8370 delivers a reliable, high performance system solution for T1/E1, HDSL terminal units, Multiplexers, Channel/Data Service Units (CSU/DSU), Digital Access Cross-Connect Systems (DACS), PBXs, PCM channel banks and other applications. A programmable clock rate adapter eases system bus interfacing by synthesizing standard clock signals from the receive or transmit line rate clocks or from an external clock reference input.

For applications that do not require long-haul performance, the Bt8375 and Bt8376 are available.

The following table summarizes the capabilities of the Bt8370 family.

<table>
<thead>
<tr>
<th>Feature</th>
<th>Bt8370</th>
<th>Bt8375</th>
<th>Bt8376</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single Chip T1/E1</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>T1 long-haul</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Number of HDLC controllers</td>
<td>2</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>Clock Adapter output (KHz)</td>
<td>8-16384</td>
<td>8-16384</td>
<td>None</td>
</tr>
</tbody>
</table>
Compliant with Standards
Current ANSI, ETSI, ITU-T and Bellcore standards are supported. Physical layer support is provided for alarm generation and detection, error monitoring, per-channel trunk conditioning and Facility Data Link (FDL) maintenance. Data link layer support is provided for signaling channels (LAPD/SS7) as well as robbed bit (T1) and time slot 16 (E1) Channel Associated signaling buffers.

A serial Time Division Multiplexed (TDM) system bus interface allows the backplane PCM data highway to operate at rates from 1.536 to 8.192 Mbps. Extensive test and diagnostic functions include a full set of digital and analog loopbacks, PRBS test pattern generation, BER meter, and forced error insertion.

The Bt8370's parallel 8-bit microprocessor port supports Intel or Motorola style interfaces. Control and status registers may be memory mapped and all interrupts from real time events may be separately masked and latched.

Short-haul and Long-haul
The capability of the Bt8370 to be used in both short- and long-haul applications means that a single board design is suitable for use both with and without an external CSU.

The physical line interface circuit recovers clock and data from analog signals with +3 to -43 dB cable attenuation, appropriate for both short-haul (up to 18 dB cable attenuation) and long-haul T1/E1 applications. Receive line equalization (EQ) and transmit Line Build Out (LBO) filters are implemented using DSP circuits for reliable performance. Data and/or clock jitter attenuation can be inserted in either receive or transmit paths. The transmit section includes precision pulse shaping and amplitude pre-emphasis for DSX applications as well as up to three LBO filters for long-haul CSU applications. A complementary driver output is provided to couple 75/100/120 ohm lines via an external transformer.
Bt8370 functional block diagram

Bt8370EVM–Bt8370 evaluation module, Quad T1/E1 ISDN PRI board
Product Highlights

- Single-chip T1/E1 framer with short/long-haul physical line interface (Bt8370) or short-haul only (Bt8375/6)
- Supports popular T1/E1 framing formats:
  - T1: SF, ESF, SLC®96, T1DM
  - E1: PCM-30, G.704, G.706, G.732 ISDN primary rate
- On-chip physical line interface compatible with:
  - DS-1 (T1.403) and ETU (leased line) long-haul signals
- Two-frame transmit and receive PCM slip buffers
- Clock rate adapter synthesizes low jitter system clocks from an internal or external reference
- Parallel 8-bit microprocessor port supports Intel or Motorola buses
- Automatic one second performance report message generation
- Bit Error Rate Test (BERT) generation and counting
- Two full-duplex HDLC controllers for simultaneous facility data link and LAPD/SS7 signaling
- Compatible with the latest ETSI and ANSI standards including CTR4, CTR12, CTR13, T1.403, T1.231
- Up to four devices connect to single PCM system bus
- System bus clock operates at 1.536, 1.544, 2.048, 4.096, 8.192 MHz
- Programmable transmit pulse shapes
- Remote line, payload and per-channel loop-backs
- Local analog, digital, payload and per-channel loop-backs
- Channel Associated Signaling (CAS) stack with signaling change detection
- Manual or automatic E bit generation in E1 mode
- Manual or automatic Remote Alarm Indication (RAI) bit generation in E1 mode
- All Sa bits buffered per multiframe in E1 mode
- Fractional T1/E1 support (per-channel signaling, loop-backs and idle code generation)
- B8ZS/HDB3/Bit 7 zero code suppression
- 80-pin MQFP surface-mount package
- Operates from a single +5 Vdc ± 5% power supply
- Low-power CMOS Technology

Evaluation Module Features

- Four T1 or E1 ports – line and frame formats may be individually configured
- Command line interface via serial port and VT100 terminal
- LEDs for alarms and status
- ROM device driver and real-time operating system
- User may control ports via menu selection, then display complete set of register values for reference

Applications

- WAN access equipment
  - Router
  - Remote Access Server (RAS)
  - Frame Relay switch
  - Edge switch (Frame Relay or ATM)
  - Enterprise switch (Frame Relay or ATM)
- Test equipment
  - Traffic load generation
  - Line monitoring equipment
  - Field test equipment
- Wireless communication
  - GSM pico– base station controllers
  - PCS base stations
  - DECT system units
- Voice switches
  - T1, E1, ISDN and V5.1/V5.2 PABX equipment
- Remote concentrators
- Central office equipment
- Digital Access Cross-connects (DACs)
- Voice compression
- Multiplexers (M13, E13, ATM, SDH/SONET Add-Drop Multiplexers [ADM])
- DSL T1/E1 transport

Order: 500115 A M01-0417