Octal ATM Transmission Convergence Physical Layer (PHY) Device

Conexant’s RS8228 dramatically improves performance for switch and access system low-speed ports, by integrating all of the ATM physical layer processing functions found in the ATM Forum Cell-Based Transmission Convergence Sublayer specification for eight individual ports. All ports can be independently configured for operation at speeds ranging from 64 Kbps to 50 Mbps, and each TC port has a powerdown mode. A UTOPIA Level 2 multi-PHY interface connects the RS8228 to the host switch or terminal system and concentrates the ATM cell traffic onto one interface.

Typical system implementations center around the concentration of ATM cells over standard PDH data rates such as T1/E1, T3/E3, and multiple Digital Subscriber Line (DSL) formats such as HDSL, ADSL or VDSL. For each format, external devices perform the appropriate Physical Media Dependent (PMD) layer functions and present the RS8228 with a payload bit stream. The RS8228 then performs all cell alignment functions on that bit stream. This gives system designers a simple, modular, and low-cost architecture for supporting all UNI and NNI ATM interfaces below 50 Mbps. The RS8228 integrates all the ATM physical layer cell processing functions for eight individual ports, each port configurable for operation at data rates ranging from 64 Kbps to 50 Mbps.

The RS8228 takes the bit- or byte-synchronous data stream from all eight ports and concentrates the ATM cell traffic onto a single cell-bus (UTOPIA-L2) interface to the ATM layer router or switch fabric. Since the RS8228 performs only the cell delineation portion of the protocol stack, board designers have the flexibility to select the preferred framer/ LIU on a port-by-port basis or reuse existing devices/software.

Distinguishing Features

- Integrated 8-port solution, each individually configurable for low-speed (T1/E1, T3/E3, xDSL) data inputs
- UTOPIA Level 2, multi-PHY addressing cell-bus interface supports up to 31 PHYs
- Programmable bit- or byte-synchronous serial interfaces
- Supports all ATM physical layer cell alignment processing functions
- Microprocessor interface (8-bit data bus) for accessing available read/write registers
**features and specifications**

**Product Features**

- **Frame Interface Section**
  - Programmable bit- or byte-synchronous serial interface
  - Direct connection to external Conexant components for:
    - T1/E1
    - T3/E3
    - xDSL
- Direct connection to external J2 framers UTOPIA Level 2 interface
- **PHY cell to UTOPIA interface**
- 50 MHz maximum data rate
- 8/16-bit data path interface
- Multi-PHY capability
- Compatible with UTOPIA Level 1

**Cell Alignment Framing Section**

- ATM cell interface support for:
  - Circuit-based physical layer
  - Cell-based physical layer
- Passes or rejects idle cells or selected cells based on header register configuration
- Recovers cell alignment from HEC
- Performs single-bit HEC error correction and multiple-bit detection

**Microprocessor Interface**

- SRAM-like interface mode
- Glueless Bi1233/RS8234 SAR interface
- 8-bit data bus
- Open-drain interrupt output
- Open-drain ready output
- 8 - 50 MHz operation
- All registers are read/write

**Counters/Status Register**

- Summary interrupt indications
- Configuration of interrupt enables
- One-second status latching
- One-second counter latching

**Applications**

- xDSL (ADSL/HDSL/SDSL) Access Multiplexers
- ATM Multiservice Access Concentrators
- Inverse Multiplexing over ATM (IMA)

**Further Information**

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