Programmable Traffic Management and Protocol Interworking Processors

Product Family Overview

The TSP3 family is the third generation of the highly successful traffic stream processor (TSP) architecture. It is targeted for a variety of programmable traffic management and protocol interworking functions. Unlike fixed-function devices, new features can be introduced with a software upgrade making TSP3-based hardware deployed in networks “future-proof” to evolving requirements. The family supports a broad set of applications and processing speeds that allow “common card” hardware to be used interchangeably for access, edge and core designs.

The TSP3 product family consists of four fully software compatible devices of increasing processor power: M27480, M27481, M27482 and M27483 up to 2.5 Gbps throughput – promoting software and hardware design reuse.

The TSP3 product family can be used as a “Universal” hardware and software platform across packet and cell applications, port speeds and vendor systems. The datapath, control path, processing throughput and external memory interfaces vary across the product family to meet the distinct needs of multiple network infrastructure market segments – including enterprise, access, and metro networks.

The TSP3 family supports fine-grained packet and cell traffic management functions such as queuing, hierarchical shaping and scheduling, policing, switching, and congestion management on up to 256K traffic streams. Layer 2 interworking functions include, but are not limited to, transport of Layer 2 frames over MPLS (draft-ietf-PWE3), IP-to-ATM (AAL2, AAL5 SARing), Ethernet-to-ATM (RFC2684), Frame Relay-to-ATM (frf.5/8), and IMA.

To shorten time-to-market, Mindspeed provides a suite of TSP3 applications including but not limited to PortMaker, BroadbandMaker and VoiceMaker. Source code licenses and consulting services are also available for customization. Additional applications for the TSP3 family are under development.

Flexible Communications Processing Power

The foundation of the TSP3 architecture is based on programmable Octave™ microprocessor core(s) accompanied by several hardware co-processing engines. This provides a powerful architectural advantage by combining the distinct benefits associated with both software-based programmability and hardwired devices (deterministic performance). The architecture is equally adept at handling packets and cells. The industry standard UTOPIA L2/3, POS L2/3, Ethernet, and PCI interfaces provide the flexibility to design TSP3 processors into a broad array of system architectures.
The TSP3 architecture enables feature differentiation at the traffic management and Layer 2 level such as customized queuing algorithms, hierarchical shaping and scheduling schemes, per-queue rate-limiting, proprietary encapsulations and rich customizable statistics for billing. In addition, the programmability of the TSP3 architecture enables continued compliance with changing protocol standards.

**Applications**

The TSP3 family of devices fits within a variety of system architectures, spanning many equipment categories, including routers (enterprise, edge, and core), multi-service switches, Ethernet switches, access aggregation (xDSL, cable head-ends, xPON, next-generation DLC), voice and wireless gateways, and both fixed and mobile wireless equipment. These devices can also be used as backplane or control plane SARs.

TSP3 devices have been designed to work gluelessly with complementary Mindspeed products resulting in complete system level solutions. Examples include TSP3 and M827xx Concerto Carrier VoIP processors for high density voice aggregation, M825xx Concerto Enterprise VoIP processors for triple-play voice and data linecards, CX28985 ZipWireMulti Octal g.shdsl transceiver for DSL aggregation, CX28250 OC-3 PHY for enterprise routers and CX29316 6-port T3/E3 framer for integrated T3/E3 linecards. EVM’s for the TSP3 platform are available for demonstration and development purposes.

The Octave processors are 32-bit RISC engines with specialized instructions for communications processing - optimized to meet the demands of traffic stream processing. These processors are tightly coupled to surrounding hardware engines through functionspecific registers and instructions, providing efficient dispatching of parallel hardware operations.

Compute-intensive traffic management functions such as multi-protocol classification, context fetching, class of service queue management, data transformation, traffic scheduling and multi-level shaping are offloaded to the dedicated hardware co-processors. As a result, the TSP3 architecture is capable of performing sophisticated traffic management functions at wire speed without sacrificing software programmability, as the event driven micro-processors are responsible for coordinating and manipulating the data stream processing.

**Figure 1: TSP3 development**

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