Integrated Multiservice Network Edge Solution

The EdgeMaker/CX2751x platform delivers a new class of data link processing for both IP and ATM-based network edge applications. EdgeMaker firmware running on the CX2751x Edge Stream Processor (ESP) delivers unique system-level features such as:

- Multiple full-featured services including HDLC, AAL1, AAL2, AAL5, IMA and Cell Switching that can run concurrently and be dynamically reconfigured with no processor downtime. Enterprises deploying CPE equipment based on EdgeMaker are protected from changing WAN service offerings as well as service pricing plans. Carrier equipment can support on-demand provisioning of any service, on any link, down to a single DS0.

- DiffServ-enabled services, supporting multiple priority classes and queueing on a per-logical-channel basis. Voice, video, and multiple data class traffic can be prioritized and shaped on a single connection to ensure optimal network performance.

- A high-level API with a consistent look and feel across all services. This API accelerates time to market and allows for development leverage across multiple applications/services.

Written for the CX2751x ESP, EdgeMaker firmware provides communication services up to OC-3 rates over TDM, xDSL, UTOPIA and PCI interfaces. A powerful suite of development tools to ease system design, create value-added applications, and adapt to new or changing standards is also available.

Key Features

- Versatile network processing platform for network edge applications such as Frame Relay, Voice over IP, xDSL and ATM
- Off-the-shelf firmware with integrated HDLC, AAL1, AAL2, AAL5, IMA and Cell Switching services
- On-demand service provisioning
- Concurrent services selectable to the DS0 level
- Implementation of multiple services on a single card with common hardware and software

Edge Stream Processing Services

EdgeMaker running on the CX2751x delivers a broad set of industry-standard communication services which integrates packets and Nx56/64 Kbps TDM circuits over IP, xDSL and ATM network connections. The following services are included:

- Service-Frame: An HDLC controller facility that can be used to implement packet-based data link protocols such as PPP and Frame Relay. HDLC functions such as CRC-16, CRC-32, bit stuffing/de-stuffing, FCS checking/generation and flag detection/generation are provided. HDLC channels are supported on unchannelized links or, for NxDS0 connections, on channelized links.
Service-AAL1: Service-AAL1 is an I.363.1-compliant AAL1 SAR firmware module capable of providing circuit emulation for all TDM interfaces utilizing either structured data transfer (SDT) or unstructured data transfer (UDT). Service-AAL1 SDT can map an entire T1/E1 or selected DS0s from a link to an ATM channel. It supports CAS and partial cell-fill modes. Service-AAL1 UDT provides circuit emulation for T1s and E1s. Integrated clocking support requires no external hardware.

Service-AAL2: Service-AAL2 is an I.363.2-compliant AAL2 SAR supporting CPS layer switching, Traffic Management 4.1, and raw cell insertion and extraction. Service-AAL2 supports 672 voice channels with typical CODECs.

Service-AAL5: Service-AAL5 is an I.363-compliant AAL5 SAR for bi-directional data traffic up to OC-3, with support for Traffic Management 4.1 shaping, four traffic priorities, and four class-of-service queues per VC.

Service-IMA: Service-IMA is an ATM Forum Version 1.0/11-compliant cell processing service supporting all protocol cell formats, frame formats, and state behaviors for up to 16 T1/E1 IMA links which can be combined into up to 16 IMA groups. IMA groups can be used to transport cells from a mixture of ATM AAL5, AAL2, and AAL1 services. Service-IMA creates IMA ports which can be connected to other ATM-based services or switched cell ports.

Service-Switch: Service-Switch provides transfer of cells between any two ports, along with ATM header translation and QoS policing and shaping. Other traffic management features such as CLP water marking, early packet discard, and partial packet discard are also available. In addition, EdgeMaker is capable of switching to the granularity of a single DS0.

Hardware Features
The core of the CX2751x is the network-optimized SWAN™ processor, which combines the pipelined architecture of a RISC processor with the CISC-like instruction set of a specialized communications processor. Standard packet, cell and circuit interfaces are tightly coupled with the high-performance communications-processing engine to support WAN edge applications.

Application Examples
Integrated Access Devices
An integrated access device (IAD) combines several standalone communications functions into one manageable, cost-effective solution. The EdgeMaker/CX2751x combination is an ideal platform for such an application.
By using a CX2751x ESP in the depicted WAN access card configuration, a high level of networking integration can be achieved on a single service card and a common software platform.

In this example, the EdgeMaker/CX2751x combination is used to simultaneously manage LAN data and compressed and uncompressed voice traffic between the enterprise and WAN. With the breadth of interfaces inherent to the CX2751x architecture, it works across a multitude of WAN edge infrastructures including NxT1/E1, Frame Relay, xDSL, ATM, OC-3 and DS3. EdgeMaker firmware enables industry-standard, best-of-breed, multiservice capabilities across all interfaces.

**Multiservice Edge Concentrator**

Multiservice edge switching is another application that takes advantage of the processing power and versatility of the EdgeMaker/CX2751x platform. The TDM interfaces — up to 16 links — connect gluelessly to T1/E1 framer chips and offer flexible support for a variety of circuit-based applications. At the same time, the Level I/II-compliant bi-directional UTOPIA interface built into the CX2751x, provides a means of transmitting over a switching fabric.

Using the CX2751x within an edge switching card, as illustrated, the EdgeMaker firmware package services an assortment of internetworking applications at the access point between a customer premises and the core of an ATM network. EdgeMaker delivers unprecedented provisioning speed and flexibility to service providers. This flexibility enables equipment vendors and service providers to reduce their inventory requirements.

**Development Tools**

The ESP Design Toolkit provides a full-featured set of hardware and software co-development tools for the ESP product family. The toolkit reduces design-cycle time significantly by allowing hardware integration, software integration and debugging to start early in the product-development cycle. The toolkit consists of a hardware and software co-simulator, an assembler and a debugger.

The ESP SIMMaker™ toolkit provides simulation models (SWIFT and Verilog), test benches, bus functional models, IBIS models and a reference design. Reference Code is provided to facilitate host application integration. In addition, the EdgeBuilder production driver environment is available to speed up the pace of your host development activity.
Product Highlights

Off-the-Shelf Services
- HDLC
- ATM AAL5, AAL0
- ATM AAL2
- ATM AAL1 SDT and UDT
- Cell and DS0 Switching
- Cell relay
- Supported over TDM, xDSL, UTOPIA or PCI

Applications
- Integrated access devices
- xDSL equipment
- Routers
- Wireless infrastructure equipment
- SONET edge equipment
- ATM/Frame Relay internetworking
- Multiservice edge concentrators
- Voice/data line cards

Software Flexibility
- Any service, any DS0, any time
- High-level API for minimal development time
- Adaptable to changing standards and new features

Reduced System Cost
- High port density
- Industry-standard interfaces
- Support for multiple services on common hardware

Hardware Performance
- Parallel service-optimized hardware engines
- 133 MHz custom RISC core
- HDLC formatter/de-formatter
- Full-duplex data rates up to 155 Mbps

Physical Interfaces
UTOPIA
- Level I/II
- Master or slave mode
- 8-bit Tx/Rx
- Cell or packet mode
- Independently clocked from processor core

PCI
- Revision 2.1-compliant
- 32-bit bus
- Independently clocked to 66 MHz
- PCI master and target

TDM/Serial
- 4, 8 or 16 links
- Direct CAS interface for circuit emulation
- Integrated synchronous and adaptive clocking modes

External Memory
Program and Context Memory
- Flow-through, burst-mode synchronous SRAM
- 1 MB

Scatter Memory
- Pipelined synchronous SRAM
- 512 KB

Gather Memory
- Pipelined synchronous SRAM
- 512 KB

Performance Guidelines
- HDLC: 16 T1/E1 (at least 512 DS0s with up to 32 DS0s per channel)
- AAL5: OC-3
- AAL1: 16 T1/E1
- AAL2: DS3 (voice)
- IMA: 16 T1/E1
- Edge switching: 16 T1/E1 any service, any DS0

Device Information
- Power supply 1.8V and 3.3V (optional 5V tolerant operation)
- Power dissipation: 2 watts at 133 MHz
- Package: 553 PBGA
- Body size: 37.5mm x 37.5mm x 2.33mm
- Lead pitch: 1.27mm
- Ball diameter: 0.75mm
- θJA (°C/W): 13.3 still air, 11.5 at 1 mps air flow
- Operation temperature: -40°C to +85°C
- Maximum device junction temperature: +110°C

Development Tools
- Hardware and software co-simulator
- Simulation models and test benches
- Debugger
- Assembler

Ordering Information
- CX27511-12: 4 TDM links
- CX27512-12: 8 TDM links
- CX27513-12: 16 TDM links
- ESP SIMMaker
- ESP Design Toolkit
- Please contact your local sales office for firmware and tools part numbers