The M21105/6/7 are high-performance 4x4 crosspoint switches with integrated multi-rate clock and data recovery (CDR) circuits, optimized for multi-lane telecom, and datacom applications. Each channel has an independent multi-rate CDR capable of operating at bit rates between 42 Mbps and 3.2 Gbps, allowing maximum flexibility in system design.

Signal conditioning features include adaptive input equalization and output pre-emphasis, allowing robust reception and transmission of signals to other devices up to 60" away.

User-selectable input interface types allow DC-coupled input to CML, LVDS, and LVPECL. The outputs can also be DC-coupled to CML, LVDS, and LVPECL.

Frequency acquisition is accomplished with an external reference clock. The built-in frequency synthesizer allows multi-rate operation, while operating with a single reference clock. The device can be controlled either through hardwired pins or an I2C-compatible interface. The hard-wired mode eliminates the need for an external microcontroller, while allowing control of the key features of the device. The I2C-compatible interface allows complete control of the device features.
**Product Features**

- Flexible control through I2C-compatible interface or hardwired pins
- Simple protection switching configuration through hardwired pins
- Fully non-blocking architecture (any input to any output)
- Broadcast and multicast feature
- Built-in pattern generator and receiver for module and system testing
- Optimized for PRBS- or 8b/10b-like data patterns

**Applications**

- Protection switching and redundancy
- Backplane reach extension
- SONET OC-48, OC-48 with FEC systems and modules
- Fibre Channel (1x, 2x, 10x) systems
- Gigabit Ethernet systems
- 10GBASE-CX4/LX4 XAUI systems & modules
- Serial transceiver functions
- Serial-ATA redundancy
- Port bypass

**Ordering Information**

Number: M21105 (42 Mbps – 3.2 Gpbs)  
M21106 (1 Gbps – 3.2 Gbps)  
M21107 (42 Mbps – 800 Mpbs)

Package data: 72-terminal, 10mm, MLF

---

**Figure 1: The M21105/6/7 System Diagram - Equalization**

**Figure 2: The M21105/6/7 System Diagram - Pre-Emphasis**