# M02140 Evaluation Module

## User Guide

02140-EVMD-001-B
June 2004

MINDSPEED™

## Revision History

| Revision | Level | Date | Description |
|---|---|---|---|
| B | Final | 06/25/2004 | Update LOS Resistor Values |
| A | Final | 06/25/2002 | Initial Release |

# Contents

# Tables

# Figures

# 1.0 Operation of Evaluation Module

## 1.1 Functional Description

The M02140 Evaluation Board has been designed to demonstrate the performance of the M02140, a highly integrated limiting amplifier targeted for use in optical receivers operating up to 12.5 Gbps.

The evaluation board enables the user to investigate the full functionality of the device and facilitate programming of various features. The high speed data inputs and outputs are DC-coupled, with controlled impedance lines and good quality SMA connectors providing the interface to test equipment. The laminate (Rogers RO4003) used for the design of this board, offers superior high frequency performance and ensures a good quality transmission medium for the signals delivered to and output from the board.

### Features:

- Single -3.3V supply to enable direct connection of inputs and outputs to test equipment
- SMA connectors for all high-speed I/O connections
- DC-coupled CML Outputs
- Operates with Differential input levels up to 1 V p-p.
- Loss of Signal (LOS) indication
- Analog Received Signal Strength Indicator (RSSI) output

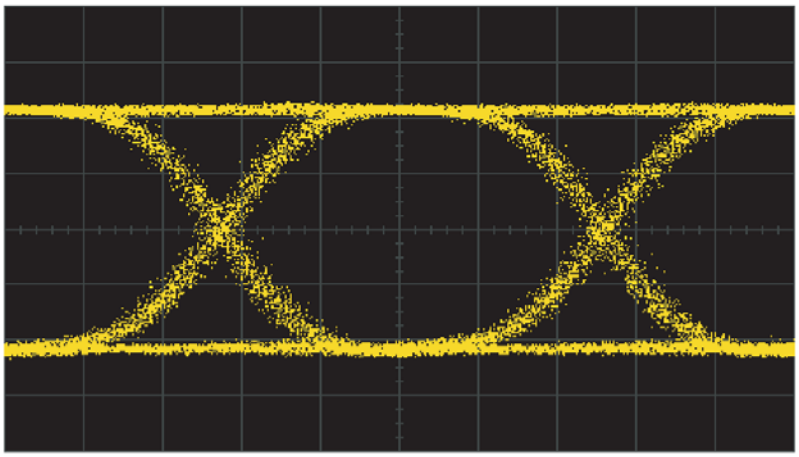
### Programmability

- Programmable CML output levels
- Loss of Signal threshold level adjustment
- Selectable data output power down/squelch operation (Jam)

### Test Points Available

- Receive Signal Strength (RSSI) level
- Bandgap reference
- Status Outputs
- PWDN input
- LOS threshold setting voltage
- AMPSET voltage that defines CML output levels

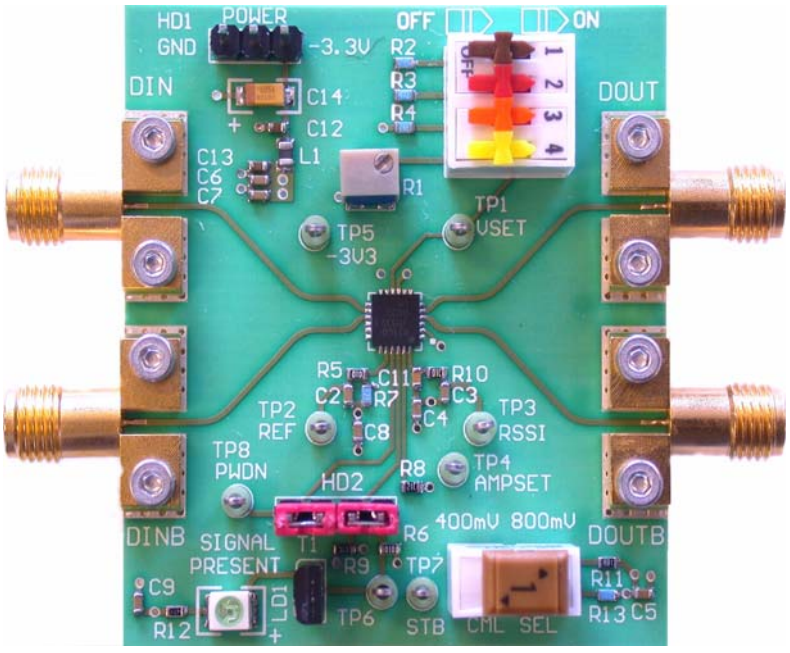
*Figure 1-1. Typical Eye Diagram*



**Conditions** 10 mVpp differential input
10.3 Gbps, Pattern $2^{23}$ -1
LOW output CML level

**Scale** Time 20 ps/Div.
Amp 50 mV/Div

*Figure 1-2. Evaluation Board*



### 1.1.1 Power

A single negative -3.3V (± 5%) power supply is required to power this board. Power is applied via 3 pin header HD1. Indication of polarity on the printed circuit board is provided to enable correct connection. With low CML output levels selected, the typical operating current of this board is 46 mA, under nominal operating conditions.

### 1.1.2 $I_{REF}$

R7 is a 12.1 kΩ 1% resistor that is used to set an on chip reference current. This current, typically 100 μA, is the main reference for determining the bias current for the rest of the device. Note: R5 and C2 are not required in the application but are required to aid non-intrusive measurement of the reference voltage. Direct capacitive loading of $I_{REF}$ pin could cause instability.

### 1.1.3 Data Inputs

Data is applied via SMA Edge launched connectors SK2 & SK3. The board has primarily been designed to accommodate differential DC-coupled input signals in the range of 6-1000 mVpp. It is important that the common mode voltage at each input does not go below $V_{CC}$-250 mV. AC-coupled operation can be supported with the use of externally connected DC blocks.

### 1.1.4 Data Outputs

The differential data outputs are available at SK1 & 4 and can be directly connected to 50 Ω test equipment. The outputs are back terminated with 50 Ω pull-ups to the most positive supply. The outputs are Current Mode Logic (CML) compatible. The output swing can be selected using SW2 and can be either 400 mVpp or 800 mV pp differential. The single ended output current ($I_{EE}$) in each mode is typically 8 mApp and 16 mApp.

Microstrip transmission lines have been used to provide good quality transmission from the device to the test equipment. Figure 1 demonstrates the typical performance with 400 mV output swing selected.

The Single Ended Output Voltage Swing
= $I_{EE}$ x (Rout || Rload)

Where:

$I_{EE}$ = 8 mA or 16 mA

For lowest overall power consumption the low CML output swing should be selected.

***Table 1-1. $R_{AMPSET}$ Settings***

| Differential Voltage Swing (mVpp) | $I_{EE}$ - Single Ended Output Current (mA) | RAMPSET (Ω) |
|---|---|---|
| 400 mV | 8 | 0 |
| 800 mV | 16 | 887 |

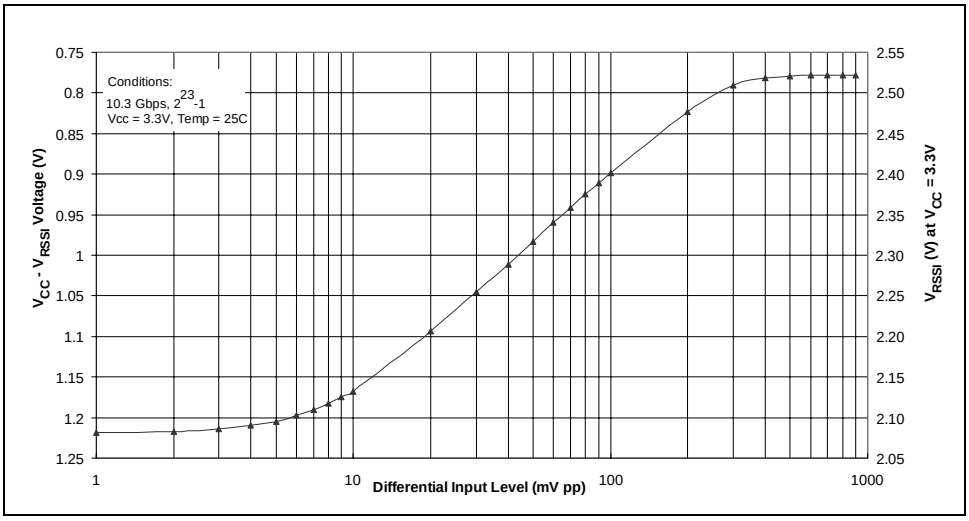
## 1.1.5 Receive Signal Strength Indication (RSSI)

Receive Signal Strength Indication is provided by this device and can be monitored at TP3.

This function provides a linear output voltage that is a logarithmic function of the input signal. It should be noted that the voltage developed at the RSSI pin is referenced to the most positive supply.

Capacitor C11 integrates the detected signal to prevent glitches at the output and this component also determines the signal detect reaction time. Components R10 and C3 allow non-intrusive monitoring of the RSSI voltage at TP3. The RSSI voltage is utilized by the loss of signal function (LOS). This voltage, when compared with a presetable reference, helps determine the loss of signal threshold. The typical characteristics of the RSSI function are presented in Figure 1-3.

***Figure 1-3. RSSI Characteristics***




## 1.1.6 Loss of Signal Function (LOS)

Loss of signal threshold adjustment and status indication are provided. The evaluation board provides the option to either set the LOS threshold to one of three presetable levels or have the flexibility to be able to adjust the threshold over the full operating range. An external resistance, $R_{LOS}$, connected between pin $LOS_{SET}$ and $V_{CC}$ enables the user to program the LOS threshold level.

The RSSI function develops a voltage that is directly compared with the voltage set at $LOS_{SET}$. When the voltage at the RSSI pin is lower than that programmed at $LOS_{SET}$,

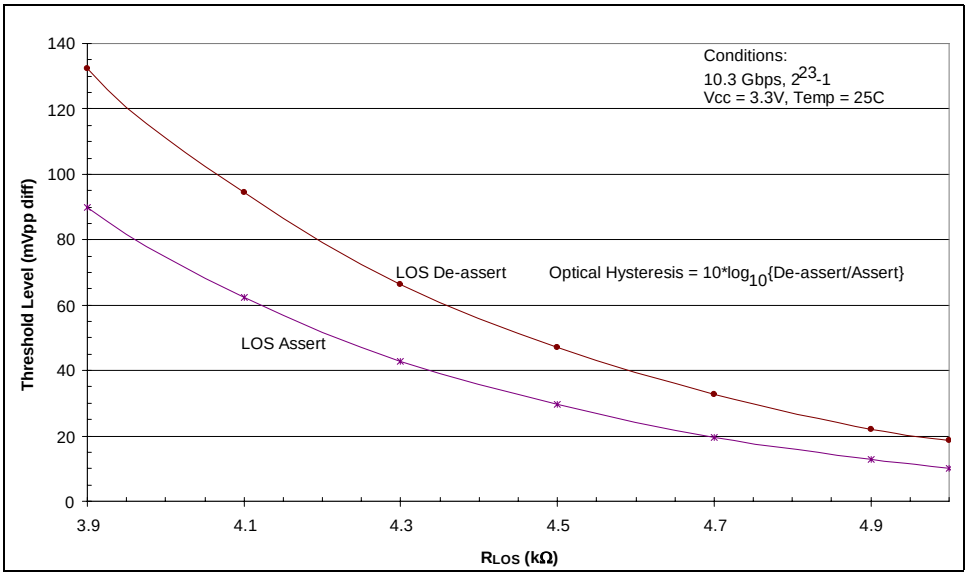
then LOS is asserted and Status (ST) is de-asserted. When the input level increases above the $LOS_{SET}$ voltage then LOS is de-asserted and Status asserted. If header HD2 pins 1 & 2 are connected, then LOS is indicated on the board by LED LD1, which is illuminated when the signal is above the LOS threshold, i.e. "signal present", and off when loss of signal has occurred.

The evaluation board includes a switch, SW1, which allows the user to make his selection of desired LOS level or to allow continuous adjustment of the LOS threshold via R1. Resistors R2-R4 define the three preset levels.

Fig. 4 has been included to aid the selection of the appropriate resistance $R_{LOS}$ and desired LOS threshold setting level.

More detailed description of both the RSSI and LOS functions are included in the data sheet.

***Figure 1-4. LOS Characteristics***




## 1.1.7 Power Down (PWDN)

Power Down (PWDN) is a CMOS compatible input that can be used to inhibit the data outputs when forced to a logic high. If connected directly to the LOS output pin, then when LOS is asserted the data outputs will be forced to $V_{CC}$ ensuring that no data is propagated through the system. Header, HD2, provides the flexibility to either connect LOS to PWDN or leave unconnected. Visual indication of the LOS status can also be enabled or disabled by linking the relevant pins at HD2.

Connect HD2 pins 3 & 4 to connect LOS to PWDN.

Connect HD2 pins 1 & 2 to provide visual indication of LOS status.

# 2.0 EVM Bill of Materials

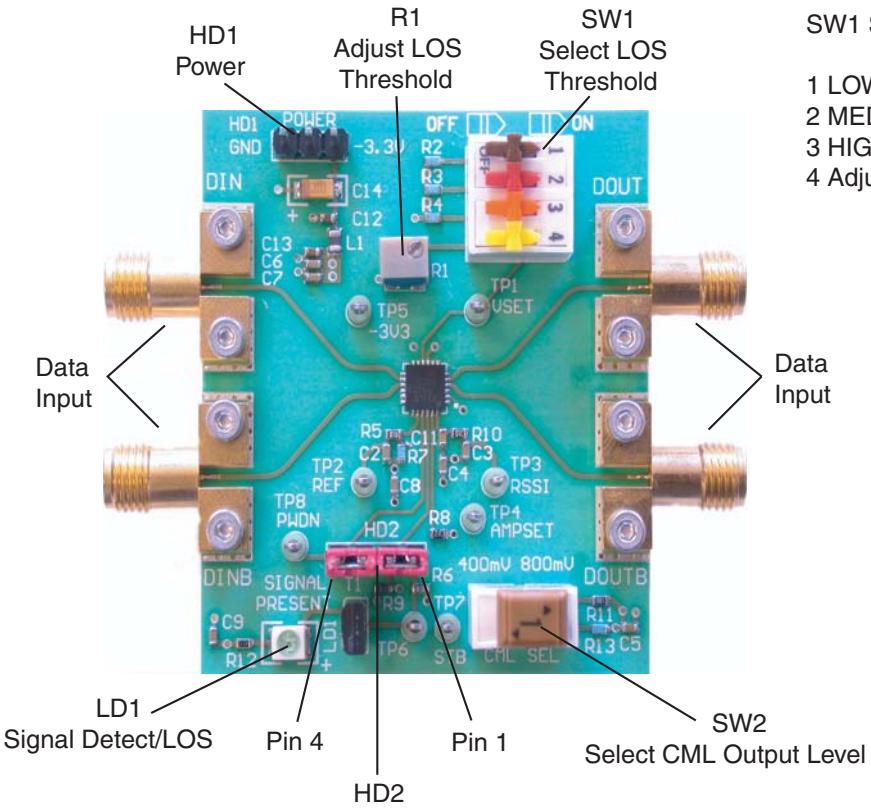
*Table 2-1. Bill of Materials*

| Quantity | Circuit Reference | Description |
|---|---|---|
| 9 | C1 to C9 | 10 nF ±10%, 50 V ceramic capacitor (0603), Murata GRM188R71H103KA01B |
| 1 | C10 | 100 pF ±10%, 250 V ceramic capacitor (0603), American Technical Ceramics 600S101KW250XT |
| 1 | C11 | 4.7 nF ±10%, 10 V ceramic capacitor (0603), Murata GRM188R71H103KA01B |
| 2 | C12, C13 | 100 nF ±10%, 16 V ceramic capacitor (0603), Murata GRM188R71H103KA01B |
| 1 | C14 | 10 µF ±10%, 10 V tantalum capacitor (1206), AVX TPS106K010R1800 |
| 1 | R1 | 10 kΩ, Bourns - 3214W series, 5 turn |
| 1 | R2 | 4.99 kΩ ±1%, resistor (0603) |
| 1 | R3 | 4.75 kΩ ±1%, resistor (0603) |
| 1 | R4 | 3.92 kΩ ±1%, resistor (0603) |
| 2 | R5, R6 | 100 kΩ ±1%, resistor (0603) |
| 1 | R7 | 12.1 kΩ ±1%, resistor (0603) |
| 2 | R8, R9, R10 | 10.0 kΩ ±1%, resistor (0603) |
| 1 | R11 | 887 Ω ±1%, resistor (0603) |
| 1 | R12 | 470 Ω ±1%, resistor (0603) |
| 1 | R13 | 0 Ω ±1%, resistor (0603) |
| 1 | L1 | BLM21R601SK, Murata (0805) |
| 1 | LD1 | (LED) KA3258LIT, Kingbright |
| 1 | HD1 | 3 pin header, 0.1” pitch |
| 1 | HD2 | 4 pin header, 0.1” pitch |
| 1 | SW1 | SDS4-014 4SPST DIL switch, ERG |
| 1 | SW2 | SDC1-014 1 pole change over DIL switch, ERG |
| 4 | SK1 to SK4 | 32K243-40ME3, Rosenberger |
| 1 | T1 | ZVP4424A, Zetex (3pin ELINE) |
| 8 | TP1 to TP8 | 200-208, W. Hughes |

# 3.0 Schematics and Layout

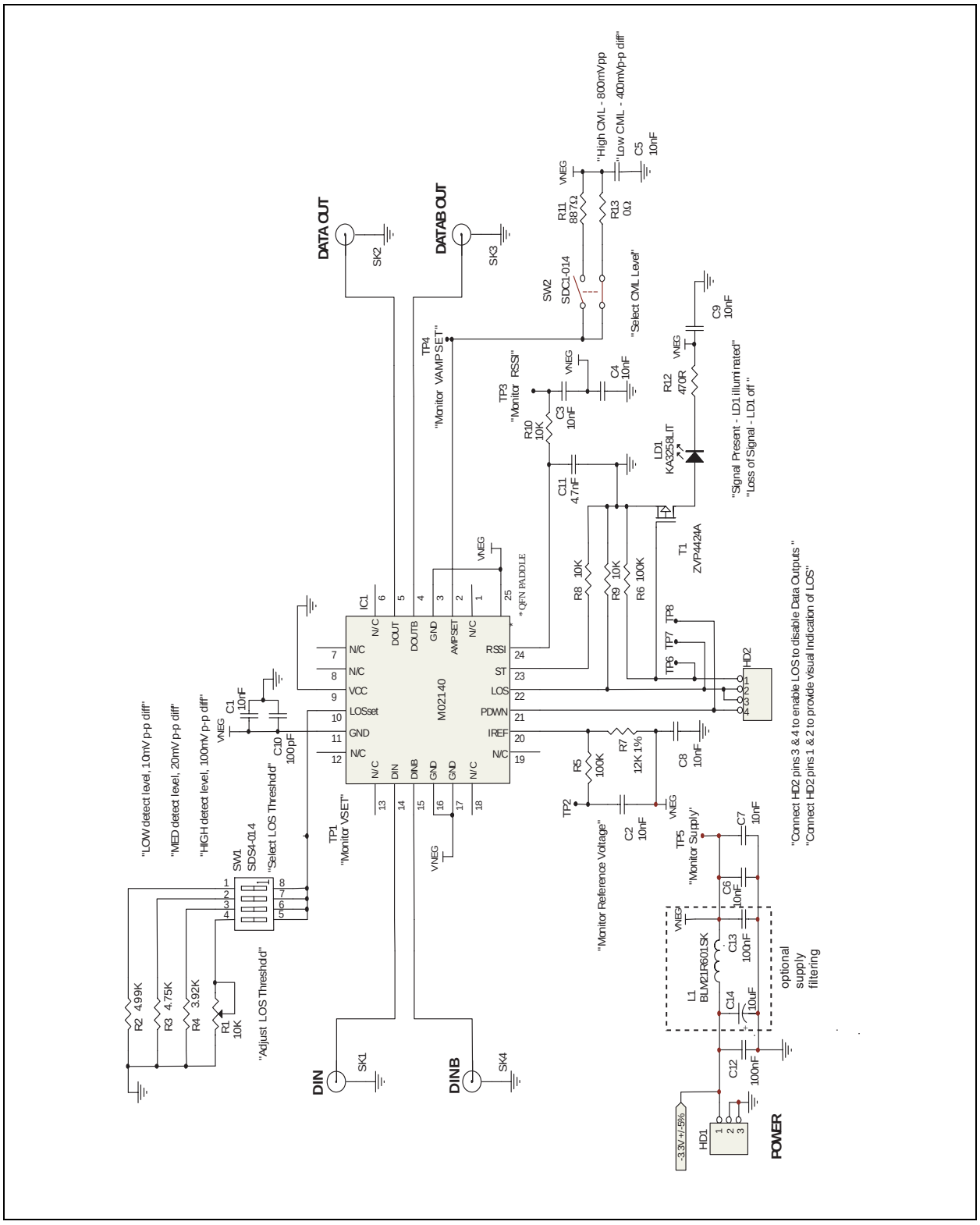
## 3.1 Board Layout

***Figure 3-1. Board Layout***



# 3.2 Schematics

***Figure 3-2. Schematic Diagram***



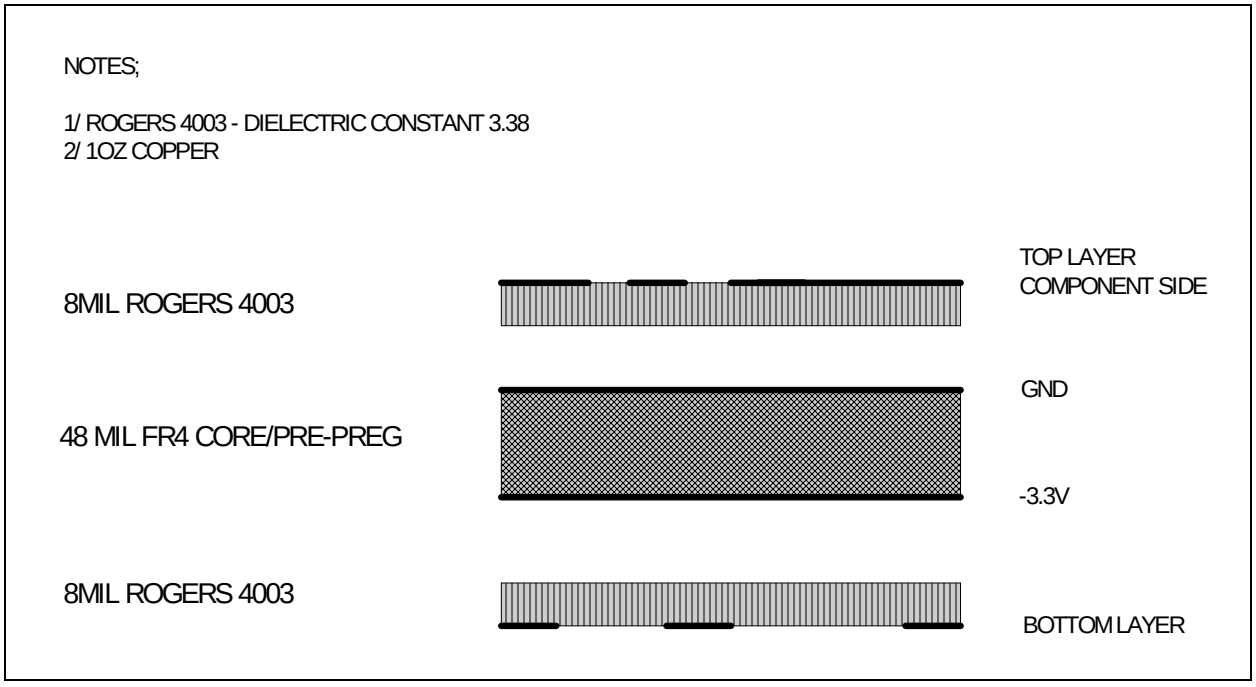
### 3.2.1 Printed Circuit Board Details

The Printed Circuit Board (PCB) is designed using mixed laminates. The board is constructed using a four layer stack, with Rogers 4003 laminate utilized on the top and bottom layers. FR4 core pre-preg is used for the inner layer which has power planes that supply power to the limiting amplifier. The Rogers 4003 laminate offers superior high frequency performance when compared to standard FR4. The laminate can be processed using conventional epoxy/glass processes and can be used in mixed laminate builds. The layer stack-up for this board is highlighted in Fig. 7.

Microstrip lines (19 MIL trace width) are incorporated on the component side and provide a 50 Ω controlled impedance to and from the device. The internal power planes provide a low impedance path for the ground and -3.3V power connections. In addition to the use of planes, a combination of low frequency and high frequency power supply decoupling is incorporated on the board.

Gerber information is available.

***Figure 3-3. Layer Stack***



MINDSPEED™

**www.mindspeed.com**

Tel. (949) 579-3000
Headquarters  Newport Beach
4000 MacArthur Blvd., East Tower
Newport Beach, CA. 92660