

Low Power 3.3 Volt Limiting Amplifier for Applications up to 12.5 Gbps

M02140

Low power, high sensitivity 12.5 Gbps limiting amplifier in 4X4 MLF package

The M02140 is a high-gain limiting amplifier for applications up to 12.5 Gbps, and incorporates a limiting amplifier, a CML buffer and an input signal level detection circuit. The M02140 also features a fully integrated DC-offset cancellation loop that does not require any external components.

The user is provided with the flexibility to set the output amplitude levels and the signal detect threshold. Optional output buffer disable (squelch/jam) can be implemented using the power down (PWDN) input.

The data inputs are internally biased to VCC via 50Ω resistors, and may be AC or DC-coupled. Note that if the inputs are AC-coupled, the coupling capacitor should be of sufficient value to pass the lowest frequencies of interest, bearing in mind the number of consecutive identical bits, and the input resistance (The use of a 2 to 10 nF capacitor is recommended). The coupling capacitor should also be of sufficient quality as to pass the high frequency content of the input data stream.

The M02140 contains internal DC feedback requiring no external components to remove the effects of DC offsets and to act as a DC auto-zero circuit. This circuit is configured such that the feedback is effective only at frequencies well below the lowest frequency of interest. The low frequency cut off is typically less than 50 kHz.

KEY FEATURES

- Wide dynamic range with 5.5 mV typical input sensitivity at 10 Gbps
- Received signal strength indicator (RSSI)
- Programmable input signal level detect
- Operates with +3.3 V supply
- CML data outputs with typical 23 ps rise and fall time
- Wide -40 to +85 °C operating temperature range
- On-chip DC offset cancellation circuit

The output swing is linearly proportional to the value of R_{AMPSET} . It is possible to set the output voltage swing linearly between 400 mVpp differential and 800 mVpp differential, when the outputs are properly terminated. See the applications information section for further details on setting the output swing amplitude.

The RSSI output voltage is proportional to the log of the input signal amplitude (the RSSI output voltage is linearly proportional to the optical modulation amplitude (OMA)). An external 4.7 nF capacitor must be connected from the RSSI output to VCC. The capacitor integrates the RSSI output and also sets the loss of signal reaction time. The RSSI voltage is compared with a selectable reference to determine loss of signal as described in the next section.

Using an external resistor, R_{LOS} , between pin LOS_{SET} and VCC, the user can program the input signal threshold. The signal detect status is indicated on the LOS and ST open-drain output pins. The LOS signal is active when the signal is below the threshold value, ST is active when the signal is above the threshold value.



RLOS establishes a threshold voltage at the LOS_{SET} pin. The input signal develops a voltage at the RSSI pin. This voltage is proportional to the input signal peak-to-peak value. The voltage at LOS_{SET} is internally compared to the voltage at the RSSI ($V(RSSI)$) pin. When the voltage at $V(RSSI)$ is less than $V(LOS_{SET})$, LOS is asserted (ST de-asserted) and will stay asserted until the input signal level increases by a predefined amount of hysteresis. When the input level increases by more than this hysteresis, LOS is de-asserted (ST asserted)

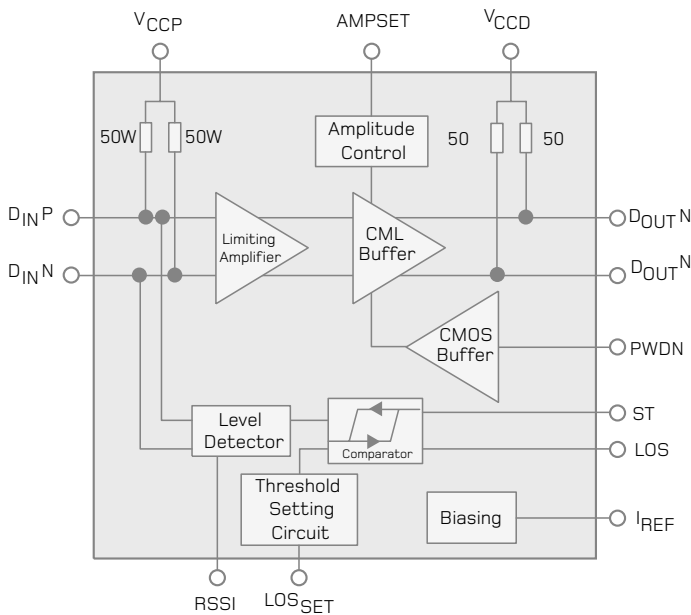
When asserted, the active high PWDN pin forces the outputs to a high state. This ensures that no data is propagated through the system. The loss of signal detection circuit can be used to automatically force the data outputs to a high state when the input signal falls below the threshold. The function is normally used to

allow data to propagate only when the signal is above the user's bit-error-rate requirement. It therefore inhibits the data outputs toggling due to noise when there is no signal present ("squelch"). In order to implement this function, LOS should be connected to the PWDN pin, thus forcing the data outputs to VCC when the signal falls below the threshold.

The M02140 contains an accurate on-chip bias circuit requiring an external 12.1 k-Ω 1% resistor, R_{REF} , from pin I_{REF} to ground to define an on-chip reference current.

The output circuit is basically a differential pair with a tail current of I_{TAIL} . The load of the differential pair is formed by the parallel combination of R_{OUT} and R_{LOAD} for high frequencies where the output AC-coupling capacitor can be considered as a short circuit ($50 \parallel 50 = 25\Omega$).

The required minimum voltage swing sets I_{TAIL} which determines the output power consumption. The minimum voltage swing depends on the application. Therefore, M02140 provides the user the flexibility to optimize the voltage swing and the output power consumption in his own application by setting I_{TAIL} using an external resistor (R_{AMPSET}).



M02140 Block Diagram

Product Features

Applications

- STM-64/OC-192 SDH/SONET
- SDH/SONET with single or double FEC
- 10G Ethernet
- 10G Fiber Channel
- XFP

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