M02040/43/49/50 Evaluation Module

User Guide

02049-EVMD-001-D
April, 2005

MINDSPEED™

Revision History

Revision	Level	Date	Description
D	Final	April 2005	Update for -14 (3.3V only) and -15 (3.3V/5V) versions of the parts.
C	Final	May 2004	Add peaking network description for 4.3 Gbps. Add user instructions to Fig. 3-1.
B	Final	April 2004	Update RAMPSET and RST values
A	Final	February 2004	Initial Release

1.0 Operation of Evaluation Module

1.1 Functional Description

The M02040/43/49/50 Evaluation Module has been designed to demonstrate the performance of the respective ICs, a highly integrated family of limiting amplifiers targeted for use in optical receivers operating up to 4.3 Gbps (M02043/49).

The evaluation module enables the user to investigate the full functionality of the device and facilitate programming of various features. The high speed data inputs and outputs are AC-coupled, with controlled impedance lines and good quality SMA connectors providing the interface to test equipment. The laminate (Nelco N4000-13) used for the design of this board, offers superior high frequency performance and ensures a good quality transmission medium for the signals delivered to and output from the board.

Features:

- Supports the -14 (3.3V only) and the -15 (3.3/5V) versions of the parts. Either +3.3V or +5V supply selected by a switch. No components require changing
- SMA connectors for all high-speed I/O connections with AC-coupling to the IC allowing direct connection of inputs and outputs to test equipment
- Operates with Differential input levels up to 1200 mVpp
- Signal Detected (SD) indication
- Two Analog Received Signal Strength Indicator outputs: $RSSI_{AVG}$ and $RSSI_{PP}$
- Versions with PECL outputs (M02040/50) include a regulator to supply the correct PECL termination voltage regardless of the supply voltage

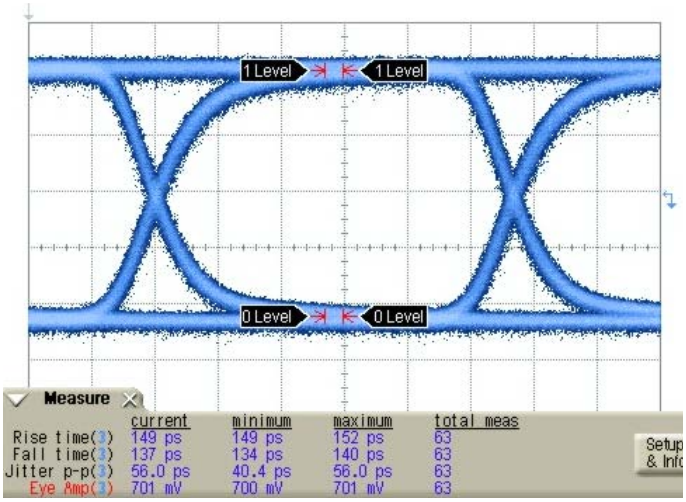
Programmability

- Programmable CML output levels (M02043/49)
- Programmable Rate Select (M02049/50) or DC Servo Disable (M02040)
- Loss of Signal threshold level adjustment
- Selectable data output power down/squelch operation (Jam)
- Selectable Signal Detect LED operation

Test Points Available

- Receive Signal Strength ($RSSI_{AVG}$ and $RSSI_{PP}$) levels
- Bandgap reference
- LOS Output
- Jam input
- LOS threshold setting voltage
- AMPSET voltage that defines CML output levels
- Regulated 3.3V output (5V operation)
- All control inputs

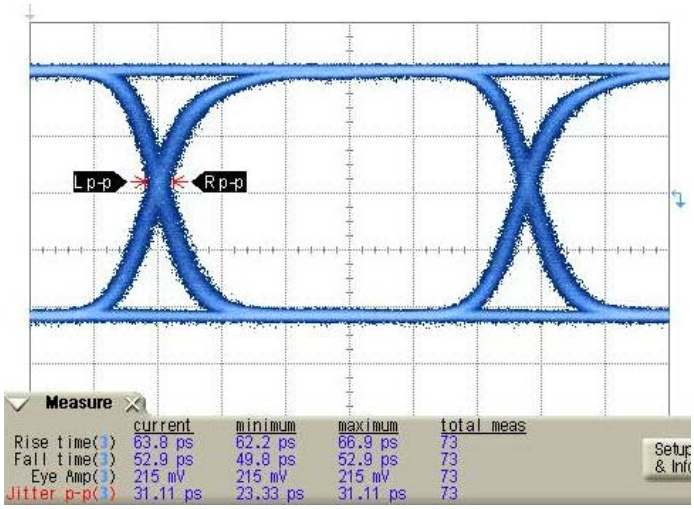
Figure 1-1. Typical 1.25 Gbps PECL Output (Low Rate Mode) Eye Diagram



10 mV_{PP} differential input
1.25 Gbps

160 mV/div
140 ps/div

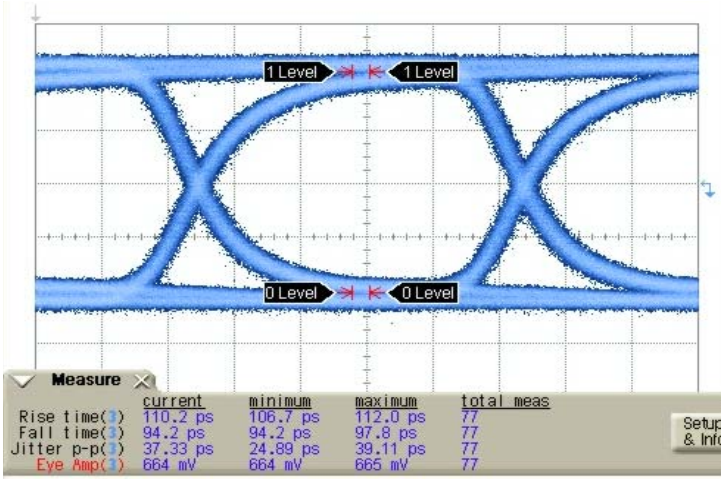
Figure 1-2. Typical 2.5 Gbps CML output (High Rate Mode) Eye Diagram



10 mV_{PP} differential input
2.5 Gbps

50 mV/div
70 ps/div

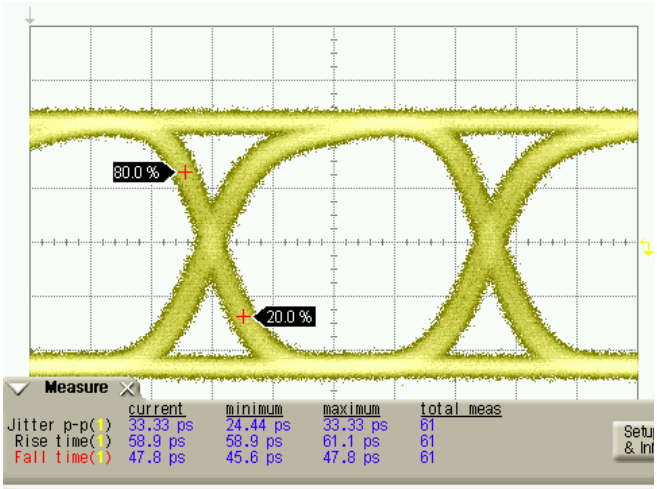
Figure 1-3. Typical 2.5 Gbps PECL output (High Rate Mode) Eye Diagram



10 mV_{PP} differential input
2.5 Gbps

160 mV/div
80 ps/div

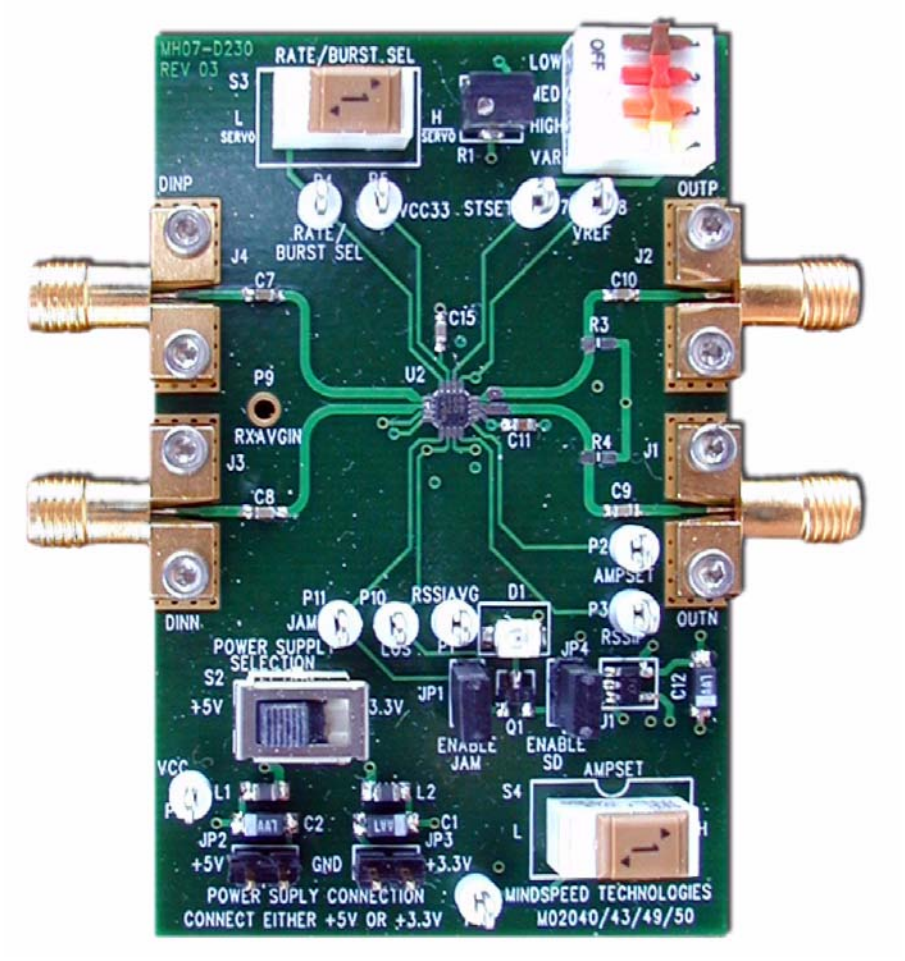
Figure 1-4. Typical 4.3 Gbps CML output (High Rate Mode) Eye Diagram



10 mV_{PP} differential input
4.3 Gbps

45 mV/div
50 ps/div

Figure 1-5. Evaluation Board



1.1.1 Power

A single positive 3.3V (± 7.5%) or 5V (± 7.5%) power supply is required to power this board. Power is applied via 2 pin header JP3 for 3.3V operation or JP2 for 5V operation. Indication of polarity on the printed circuit board is provided to enable correct connection. Switch S2 selects which external supply value is provided to the IC. If using 5V, then switch S2 needs to be in the 5V position, likewise for 3.3V.

NOTE: NOTE: This EVM supports both the 3.3V only version of the parts (-14) and the 3.3/5V version (-15). There are no other operational differences between the two versions. Both versions are available on the EVM. When fabricated with a -14 version, switch 2, the supply selection switch, will be hard-wired for 3.3V only operation.

NOTE: Switch 2, the supply selection switch, does not need to be set to the proper supply location prior to connecting the supply. However, it is important to not connect 5V to the 3.3V supply input (JP3) as this will damage the IC regulator output because 5V will be connected to the IC's 3.3V regulator output.

Using the M02043 or M02049 with low CML output levels selected and the LED off, the typical operating current of the EVM under nominal conditions of the EVM is 32 mA. For the M02040/50 EVM, typical operating current under nominal conditions is 55 mA.

1.1.2 I_{REF}

R2 is a 12.1 kΩ 1% resistor that is used to set an on-chip reference current. This current, typically 100 µA, is the main reference for determining the bias current for the rest of the device. P8 is provided to measure the voltage at the I_{REF} input, typically 1.2V. Direct capacitive loading of I_{REF} pin could cause instability and is not recommended.

1.1.3 Data Inputs

Data is applied via SMA Edge launched connectors J3 and J4. The module is designed to accommodate differential input signals up to 1200 mVpp (600 mVpp single-ended). Since the inputs are AC-coupled, the input common mode level is rejected.

1.1.4 CML Data Outputs (M02043 and M02049)

The differential data outputs are available at J1 and J2 and can be directly connected to 50Ω test equipment. The outputs are internally back terminated with 100Ω pull-ups to the positive supply. The outputs are Current Mode Logic (CML) compatible. The output swing can be selected using S4 and can be either 400 mVpp or 840 mVpp differential. The single ended output current (I_{EE}) in each mode is typically 6 mApp and 13 mApp.

Microstrip transmission lines have been used to provide good quality transmission from the device to the test equipment. Figure 1-2 and Figure 1-4 demonstrate the typical performance with 400 mV (differential) output swing selected.

The Single Ended Output Voltage Swing
= I_{OUTPUT} x (Rout || Rload)
Where:

I_{OUTPUT} = 6 mA or 13 mA
For lowest overall power consumption the low CML output swing should be selected.

Table 1-1. R_{AMPSET} Settings

Differential Voltage Swing (mVpp)	I_{OUTPUT} - Single Ended Output Current (mA)	RAMPSET (Ω)
400 mV	6	0
840 mV	13	750

1.1.5 PECL Data Outputs (M02040 and M02050)

The differential data PECL outputs are available at J1 and J2 and can be directly connected to 50Ω test equipment. U1 is a negative regulator which supplies V_{CC} - 2V to the output 50Ω PECL termination resistors R3 and R4. The PECL outputs are then AC-coupled to the output SMAs J1 and J2.

When terminated with the on-board PECL termination and connected to 50 Ω test equipment, the AC load on the PECL outputs requires more current than the standard PECL termination of 50Ω to V_{CC} - 2V. This will attenuate the output swing slightly and may lead to slower edge speeds so provision is made for removing the on-board 50Ω to V_{CC} - 2V termination and using a single discrete resistor to ground for the PECL DC termination. This is accomplished by installing 0Ω jumpers or opening R15 and R16.

To terminate the PECL outputs of the part with 50Ω to the V_{CC} - 2V regulator output, R15 = 0Ω and R16 is open. When using the ground referenced termination, R15 is open and R16 = 0Ω In addition, in this condition R4 and R5 should be 150Ω for 3.3V operation or 300Ω for 5V operation.

1.1.6 Peak to Peak Receive Signal Strength Indication ($RSSI_{PP}$)

Peak to Peak Receive Signal Strength Indication is provided by this device and can be monitored at P3.

This function provides an output voltage that is a logarithmic function of the input signal. The voltage developed at the $RSSI_{PP}$ pin is referenced to the ground.

The $RSSI_{PP}$ voltage is utilized by the loss of signal function (LOS). Internally this voltage is compared with a user selectable reference (R_ST_{SET}) to determine loss of signal. The typical characteristics of the $RSSI_{PP}$ function are presented in Figure 1-6 - Figure 1-8.

Figure 1-6. Typical $RSSI_{PP}$ Transfer Function (Full Input Range)

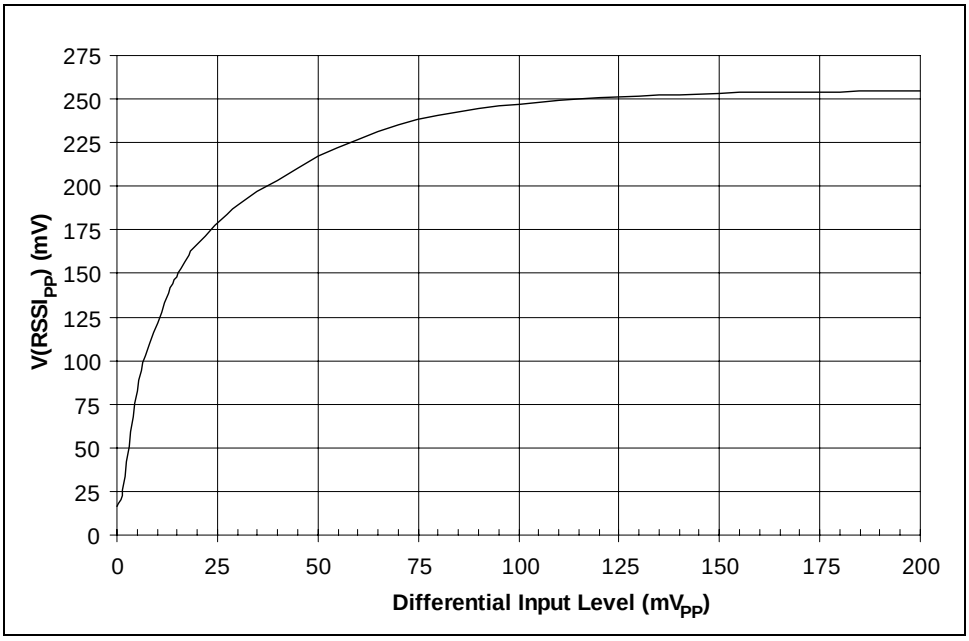


Figure 1-7. Typical $RSSI_{PP}$ Transfer Function (Low Input Level)

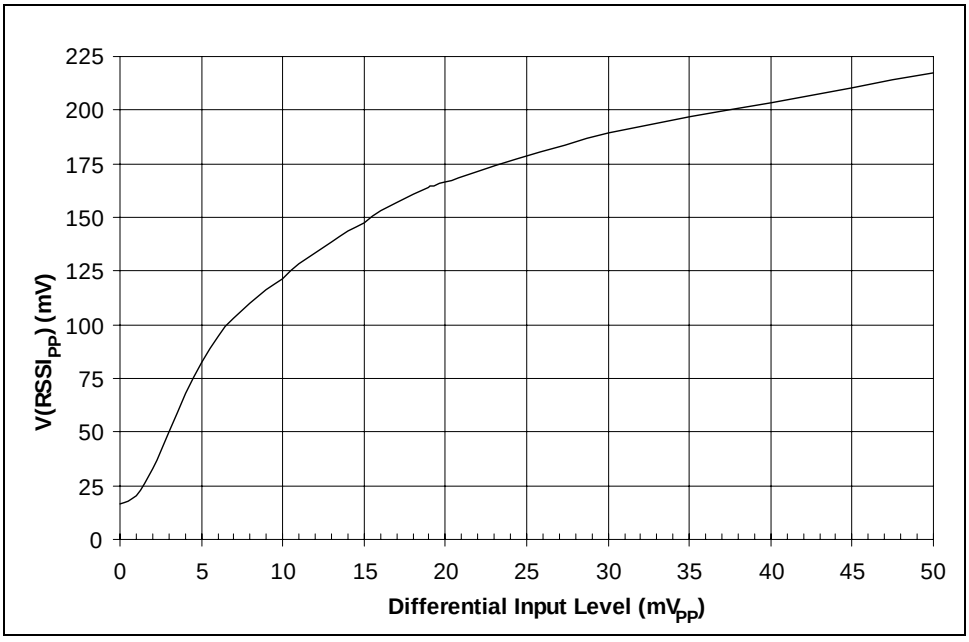
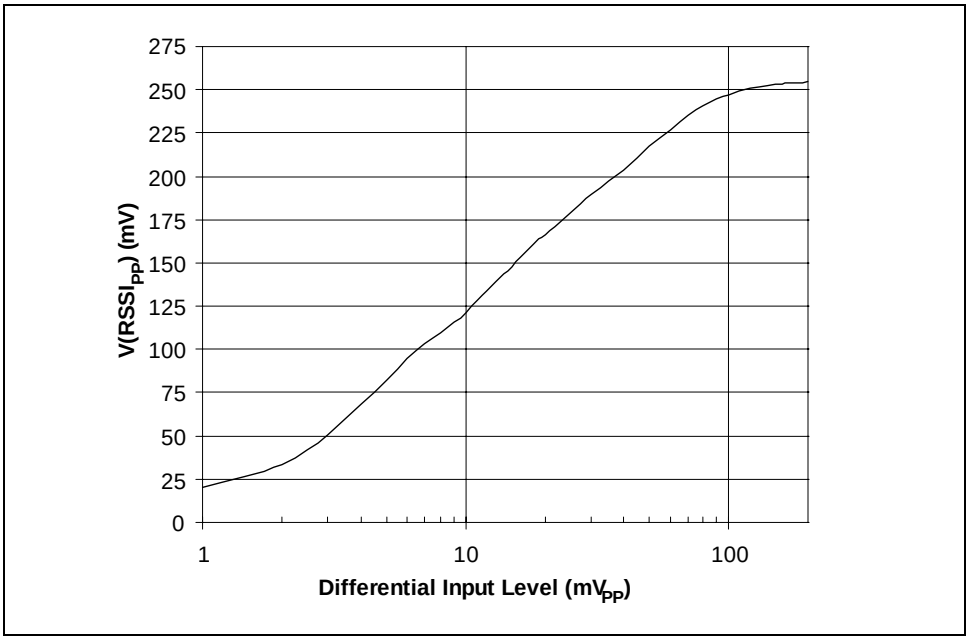


Figure 1-8. Typical $RSSI_{PP}$ Transfer Function (Log Scale)



1.1.7 Average Receive Signal Strength Indication ($RSSI_{AVG}$)

The $RSSI_{AVG}$ Receive Signal Strength Indication (P1) is a mirrored version of the $RxAVG_{IN}$ (P9) current from compatible TIAs or from a photodiode cathode. It sources rather than sinks the current making it compatible with DDMI type interfaces.

1.1.8 Loss of Signal Function (LOS)

Loss of signal threshold adjustment and status indication are provided. The evaluation module provides the option to either set the LOS threshold to one of three preset levels or to adjust the threshold over the full operating range. An external resistance, R_{ST}, connected between pin ST_{SET} and V_{CC3} (-15 versions) or V_{CC} (-14 versions) enables the user to program the LOS threshold level.

When the differential input voltage is lower than the programmed threshold at ST_{SET}, LOS is asserted and Status (ST) is de-asserted. Increasing the differential input level above the ST_{SET} threshold de-asserts LOS and asserts Status. Connecting header JP4 will illuminate LED D1 when the differential input signal is above the LOS threshold, i.e. "signal present", and turn the LED off when loss of signal has occurred.

The evaluation module includes a switch, STSET (S1), which allows the user to select one of three fixed LOS levels or to allow continuous adjustment of the LOS threshold via potentiometer R1. Resistors R8-R10 define the three preset levels.

Figure 1-9 - Figure 1-11 have been included to aid the selection of the appropriate resistance R_{ST} and desired LOS threshold setting level.

More detailed description of both the $RSSI_{PP}$ and LOS functions are included in the respective device data sheet.

Figure 1-9. LOS Characteristic (Extended Range)

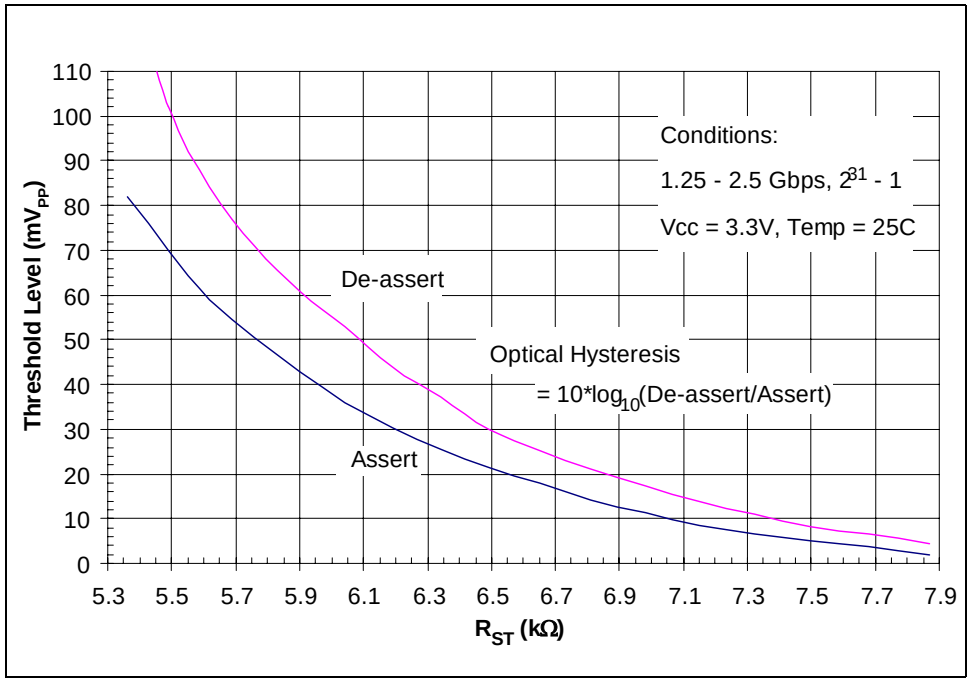


Figure 1-10. LOS Characteristic (Low Input Signal)

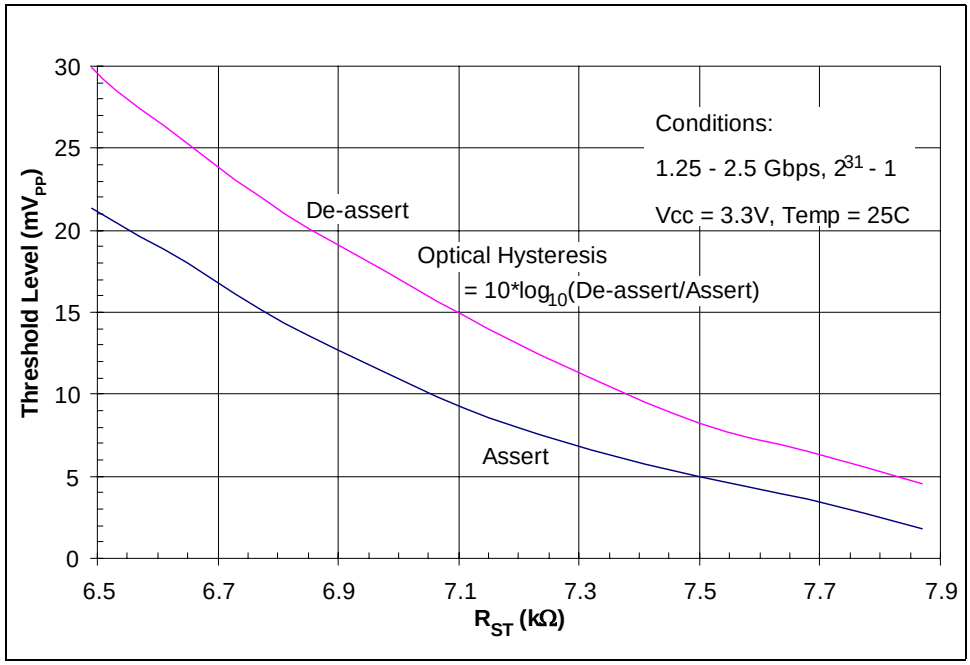
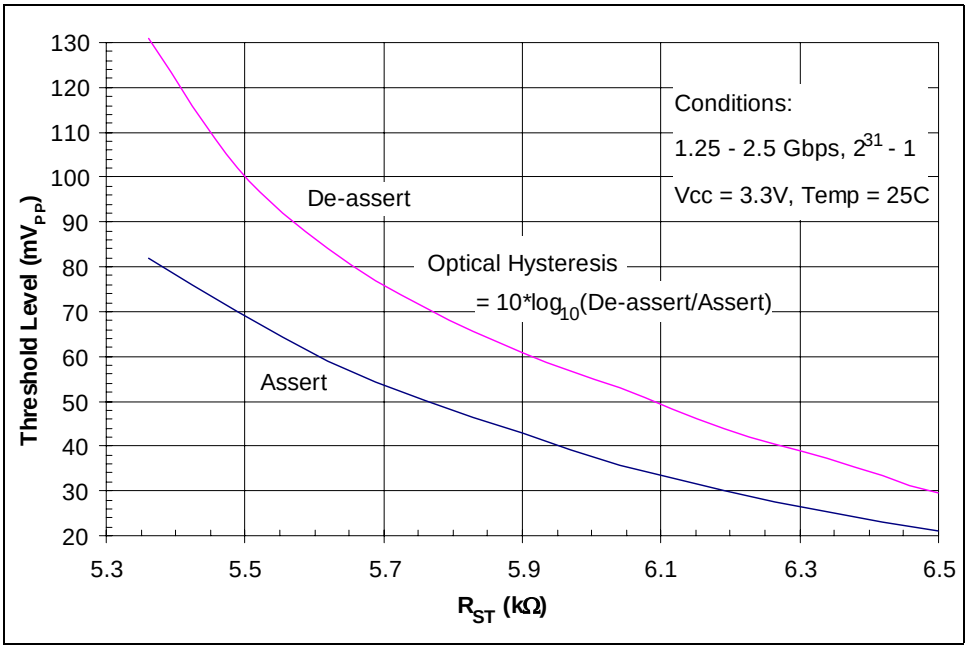


Figure 1-11. LOS Characteristic (High Input Signal)



1.1.9 JAM

JAM is a CMOS compatible input that can be used to inhibit the data outputs when forced to a logic high. If connected directly to the LOS output pin, then when LOS is asserted the data outputs will be forced to logic “one” state ensuring that no data is propagated through the system. Header JP1 (Enable_Jam) provides the flexibility to either connect LOS to JAM or leave unconnected.

2.0 EVM Bill of Materials

Table 2-1. Bill of Materials

Qty	Vendor	Part Number	Reference Designators	Description
3	PANASONIC	ECJ-3YF1A106Z	C1, C2, C12	CAP CERAMIC 10V 10UF +80/-20% Y5V 1206
6	KEMET ELECTRONICS	C0603C104K3RACTU	C3, C4, C5, C6, C7, C8	CAP CERAMIC 25V 0.1UF 10% X7R 0603
6	KEMET ELECTRONICS	C0603C103K5RACTU	C9, C10, C11, C13, C14	CAP CERAMIC 50V 0.01UF 10% X7R 0603
1	KEMET ELECTRONICS	C0603C101K5RACTU	C15	CAP CERAMIC 50V 100PF 10% X7R 0603
1	Kingbright	AA3528SRC	D1	3.5x2.8 mm SMD chip LED VF = 1.85V at ID = 20mA
4	Rosenberger	32K243-40ME3	J1, J2, J3, J4	SMA Edge Mounted Connector
4	SULLINS ELECTRONICS	PZC02SAAN	JP1, JP2, JP3, JP4	HEADER MALE 2 Pin 100 MIL STRAIGHT SINGLE ROW 1X2
2	Murata	BLM21RK601SN1	L1, L2	INDUCTOR CHIP FERRITE 600Ω at 100MHZ, 200MA, 0805
12	Keystone	5012	P1- P12	White THROUGH_HOLE PC TEST POINT, WITH EYE
1	Zetex, Inc.	ZXMP6A13FTA	Q1	60V P-CHANNEL ENHANCEMENT MODE MOSFET
1	BOURNS, INC.	3214W-1-502G	R1	RES ADJUSTABLE 5 KΩ 1/2W 10% 4MM SQUARE SMD TOP ADJUST
1	KOA	RK73H1JLTD1212F	R2	RES CHIP THICK FILM 12.1KΩ 1/10W 1% 0603
2	KOA	RK73H1JLTD1500F	R3, R4	RES CHIP THICK FILM 150Ω 1/10W 1% 0603
		Value for 3.3V PECL devices. Optionally 50Ω as described below		
2	KOA	RK73H1JLTD3000F	R3, R4	RES CHIP THICK FILM 300Ω 1/10W 1% 0603
		Value for 5V PECL devices. Optionally 50Ω as described below		

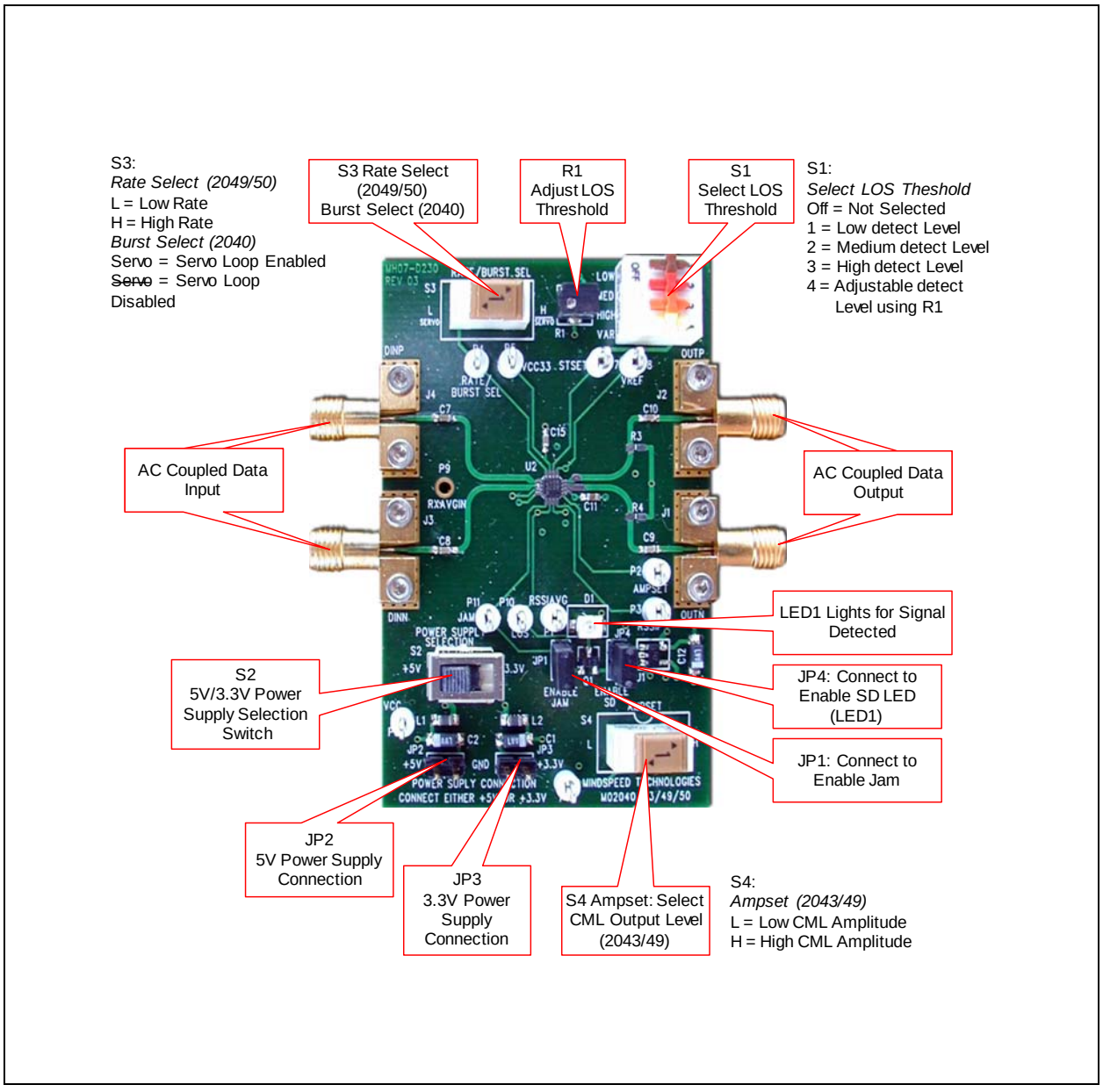
Table 2-1. Bill of Materials

Qty	Vendor	Part Number	Reference Designators	Description
2	KOA	RK73H1JLTD49R9F	R3, R4	RES CHIP THICK FILM 49.9Ω 1/10W 1% 0603
		When using the VCC-2V regulator U1 for PECL devices (3.3V or 5V)		
1	KOA	RK73H1JLTD7500F	R5 (CML devices)	RES CHIP THICK FILM 750Ω 1/10W 1% 0603
1	Yageo America	9C06031A0R00JLHFT	R5 (PECL devices)	RES 0.0Ω 1/10W 5% 0603 SMD
1	KOA	RK73H1JLTD4752F	R6	RES CHIP THICK FILM 4.75KΩ 1/10W 1% 0603
2	KOA	RK73H1JLTD1001F	R7, R12	RES CHIP THICK FILM 1.00KΩ 1/10W 1% 0603
1	KOA	RK73H1JLTD7502F	R8	RES CHIP THICK FILM 7.50KΩ 1/10W 1% 0603
1	KOA	RK73H1JLTD6812F	R9	RES CHIP THICK FILM 6.81KΩ 1/10W 1% 0603
2	KOA	RK73H1JLTD6192F	R10	RES CHIP THICK FILM 6.19KΩ 1/10W 1% 0603
1	KOA	RK73H1JLTD3012F	R11	RES CHIP THICK FILM 3.01KΩ 1/10W 1% 0603
2	KOA	RK73H1JLTD1002F	R13	RES CHIP THICK FILM 10.0KΩ 1/10W 1% 0603
1	KOA	RK73H1JLTD6652F	R14	RES CHIP THICK FILM 6.65KΩ 1/10W 1% 0603
1	Yageo America	9C06031A0R00JLHFT	R15	RES 0.0Ω 1/10W 5% 0603 SMD
		Typically open. Use zero Ω resistor when terminating PECL outputs using the VCC-2V regulator U1. In this case, R4 and R5 must each be 50Ω.		
1	Yageo America	9C06031A0R00JLHFT	R16	RES 0.0Ω 1/10W 5% 0603 SMD
		Only on PECL output devices when R4 and R5 are 150Ωs for 3.3V or 300Ω for 5V.		
1	ITW Erg Components	SDS-4-014	S1	SPST 4 position switch
1	C&K	ES21MCKE	S2	DPDT switch
1	ITW Erg Components	SDC-1-014	S3 (Not installed on PECL devices)	SPDT switch
1	ITW Erg Components	SDC-1-014	S4 (Not installed on 2040-xx device)	SPDT switch
1	Linear Technology	LT1964ES5-BYP	U1	200mA, Low Noise, Low Dropout Negative Regulator
1	Mindspeed Technologies	M0204x-1x	U2	Limiting Amplifier

3.0 Schematics and Layout

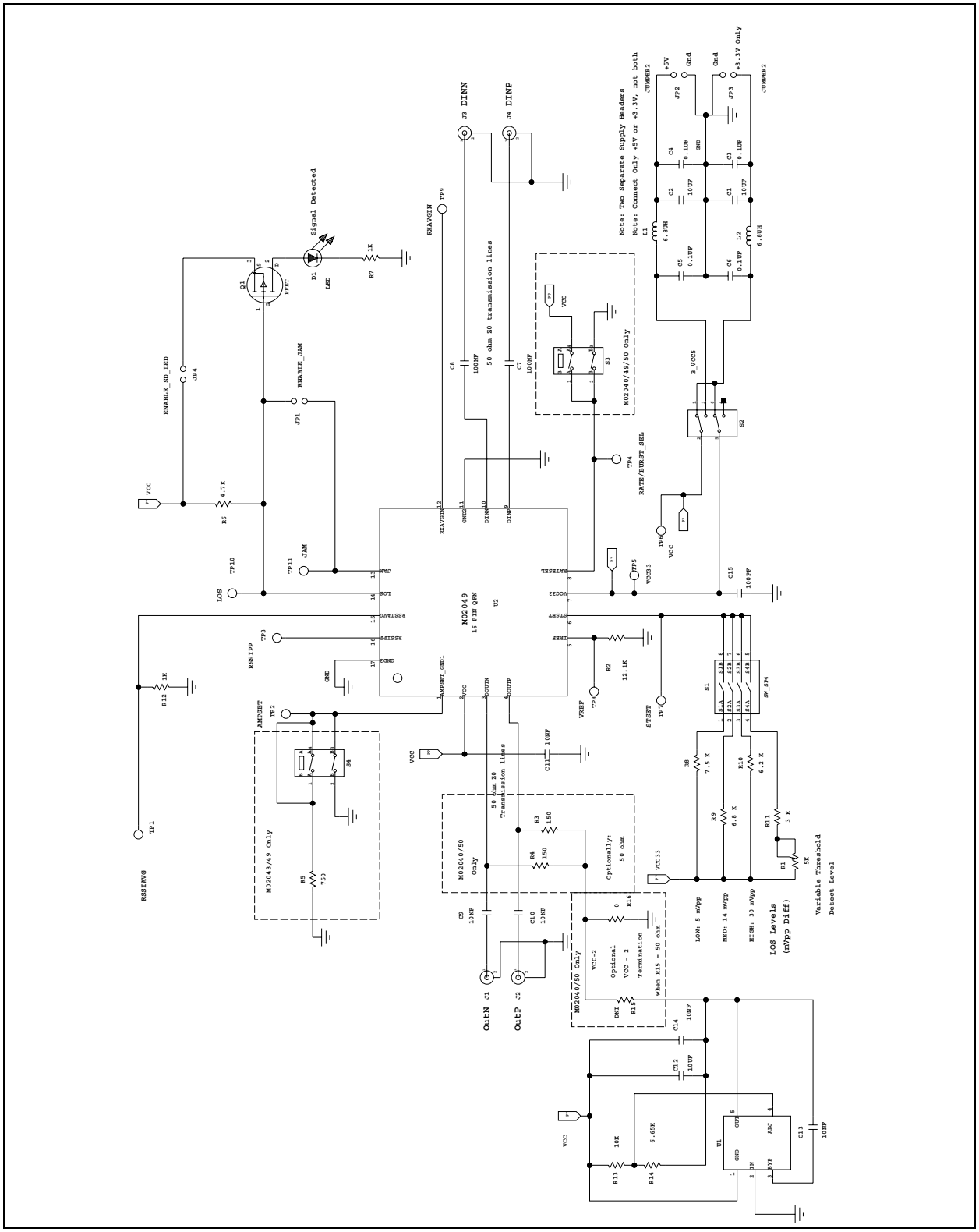
3.1 Board Layout

Figure 3-1. Board Layout



3.2 Schematics

Figure 3-2. Schematic Diagram



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