GaN Front End Module, 5 W
8.5 – 10.5 GHz

Features

Transmit
- · Saturated Output Power: 5 W
- · Power Added Efficiency: 37%
- · Large Signal Gain: 32 dB

Receive
- · NF: 2.5 dB
- · Small Signal Gain: 18 dB
- · P1dB: 15 dBm
- · OIP3: 26 dBm

Applications

- Military and Commercial Radar

Description

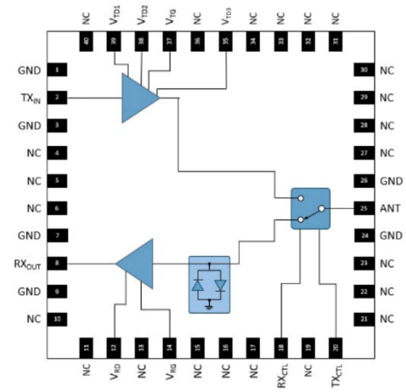
MACOM's WSM5000S is a packaged, multi-chip, front-end module utilizing both GaN and GaAs technologies. The WSM5000S operates from 8.5-10.5 GHz and supports both defense and commercial-related radar applications. In transmit mode, the WSM5000S achieves 5 W of saturated output power with 32 dB of large signal gain and typically 40% power-added efficiency under pulsed operation. In receive mode, the WSM5000S provides 16dB of small-signal gain and delivers an output P1dB of 15dBm along with noise figure of 2.5 dB and exceptional linearity.

Packaged in a 6x6 mm overmold QFN, the WSM5000S provides superior RF transmit and receive performance in a small footprint that will improve SWaP-C benchmarks in next-generation systems.

Ordering Information

Part Number	Package (MOQ/Mult)
WSM5000S	Tape & Reel (25/25)
WSM5000S-AMP	Sample Board (1/1)

Functional Schematic



Pin Configuration[1,2]

Pin #	Name
4-6, 10, 11, 13, 15-17, 19, 21-23, 27-34, 26, 40	No Connect
1, 3, 7, 9, 24, 26	GND
2	TX_{IN}
8	RX_{OUT}
12	V_{RD}
14	V_{RG}
18	RX_{CTL}
20	TX_{CTL}
25	ANT
35	V_{TD3}
37	V_{TG}
38	V_{TD2}
39	V_{TD1}

1. MACOM recommends connecting No Connection (N/C) pins to ground.
2. The exposed pad centered on the package bottom must be connected to RF, DC, and thermal ground.

RF Electrical Specifications: T_C = 25°C, Z_0 = 50 Ω

Mode	Parameter	Test Conditions	Frequency (GHz)	Units	Min.	Typ.	Max.
TX	Output Power	Bias = 28 V, 40 mA P_{IN} = 5 dBm Pulse: 100 µs, 10%	8.5 9.5 10.5	dBm	36.0 36.0 35.5	37 37 37	—
	Power Added Efficiency		8.5 9.5 10.5	%	29 30 27	36 40 37	—
	Large Signal Gain		8.5 9.5 10.5	dB	31.0 31.0 30.5	32 32 32	—
	Small Signal Gain	Bias = 28 V, 40 mA P_{IN} = -25 dBm CW	8.5 9.5 10.5	dB	—	37 36 34	—
	Input Return Loss		8.5 – 10.5	dB	—	-10	—
	Output Return Loss		8.5 – 10.5	dB	—	-9	—
RX	P1dB	Bias = 2 V, 90 mA CW	8.5 9.5 10.5	dBm	13.5 13.5 14.0	14.4 14.9 15.2	—
	Noise Figure		8.5 9.5 10.5	dB	—	2.5 2.4 2.6	—
	Small-Signal Gain	Bias = 2 V, 90 mA P_{IN} = -20 dBm CW	8.5 9.5 10.5	dB	—	19 18 17	—
	Input Return Loss		8.5 – 10.5	dB	—	-15	—
	Output Return Loss		8.5 – 10.5	dB	—	-15	—
	OIP3	P_{OUT}/Tone = 0 dBm, 10MHz	9.5	dBm	—	26	—
	Recovery Time	P1dB to Linear Gain	—	ns	—	22	—
	Switch Rise/Fall Time		—	ns	—	15	—

DC Electrical Specifications:

Mode	Parameter	Units	Min.	Typ.	Max.
TX	Drain Voltage	V	—	28	—
	Gate Voltage	V	—	-2	—
	Quiescent Drain Current	mA	—	40	—
	Saturated Drain Current	mA	—	500	—
RX	Drain Voltage	V	—	2	—
	Gate Voltage	V	—	-0.5	—
	Quiescent Drain Current	mA	—	90	—

Recommended Operating Conditions

Mode	Parameter	Symbol	Unit	Min.	Typ.	Max.
TX	Input Power	P_{IN}	dBm	—	5	10
	Drain Voltage	V_D	V	—	28	29
	Gate Voltage	V_G	V	-5	-2	-1
	Quiescent Drain Current	I_{DQ}	mA	—	40	—
RX	Input Power	P_{IN}	dBm	—	—	36
	Drain Voltage	V_D	V	1.8	2	3.5
	Gate Voltage	V_G	V	-1.5	-0.5	-0.4
	Quiescent Drain Current	I_{DQ}	mA	—	90	—
	Operating Temperature	T_C	°C	-40	—	+85

Absolute Maximum Ratings[3,4]

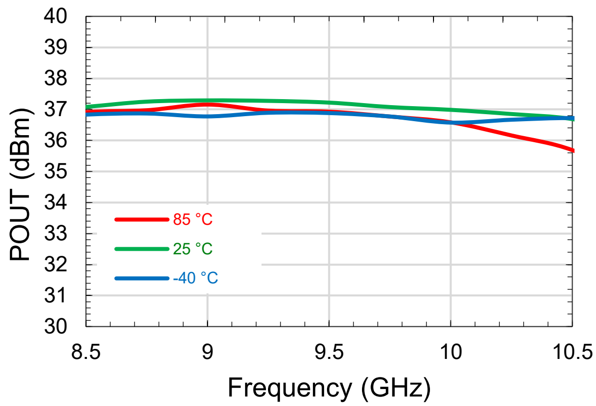
Mode	Parameter	Symbol	Unit	Min.	Max.
TX	Input Power	TX-P_{IN}	dBm	—	10
	Drain to Source Breakdown Voltage	V_{TDS}	V	—	84
	Drain Voltage	V_{TD}	V	—	28
	Gate Voltage	V_{TG}	V	-8	+2
	Drain Current	I_{TD}	A	—	1.14
	Gate Current	I_{TG}	mA	—	0.4
	Dissipated Power @ +85°	P_{DISS}	W	—	21.63
	VSWR	—	Ratio	—	5:1
	Junction Temperature (MTTF > 1E6 Hrs)	T_J	°C	—	+225°C
RX	Input Power	RX-P_{IN}	dBm		37
	Drain Voltage	V_{RD}	V		4
	Gate Voltage	V_{RG}	V	-2	0
	Junction Temperature (MTTF > 1E6 Hrs) (RX)	T_J	°C		+125°C
	Storage Temperature	T_{STG}	°C	-55	+150
	Mounting Temperature (30 seconds)	T_M	°C	—	+260

3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. MACOM does not recommend sustained operation near these survivability limits.

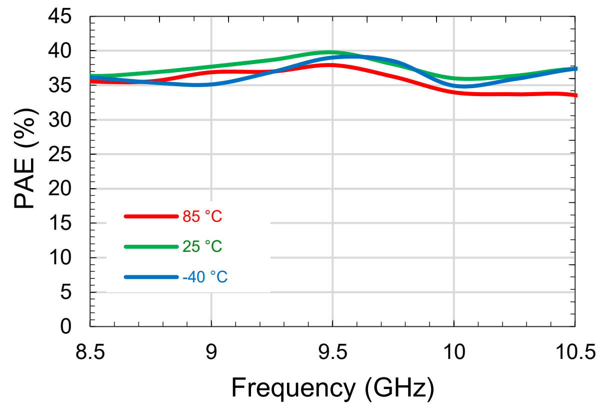
Typical Performance Curves – Large Signal over Temperature – Transmit:

V_D = 28 V, I_{DQ} = 40 mA, PW = 100 µs, DC = 10%, P_{IN} = 5 dBm

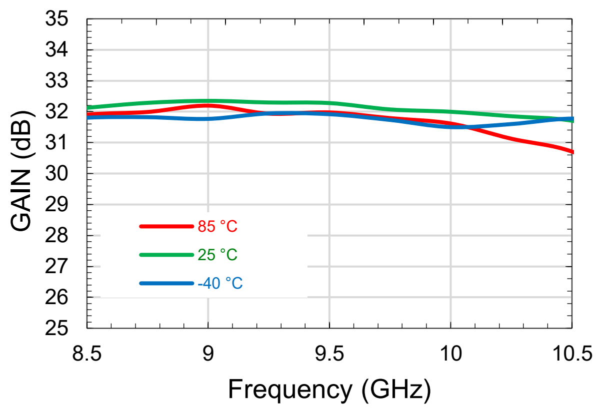
Output Power vs. Frequency



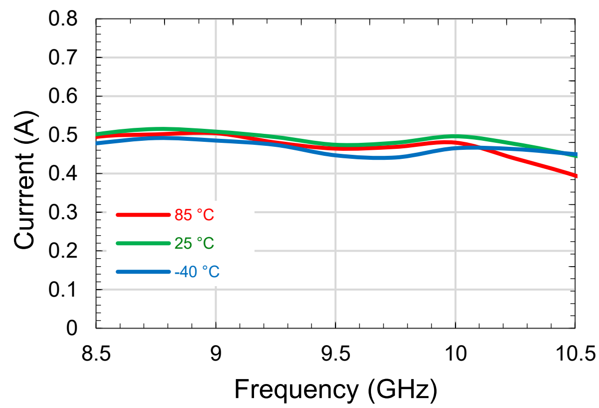
Power Added Efficiency vs. Frequency



Large Signal Gain vs. Frequency



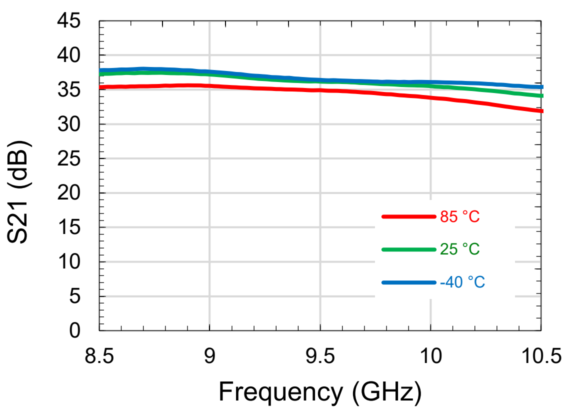
Drain Current vs. Frequency



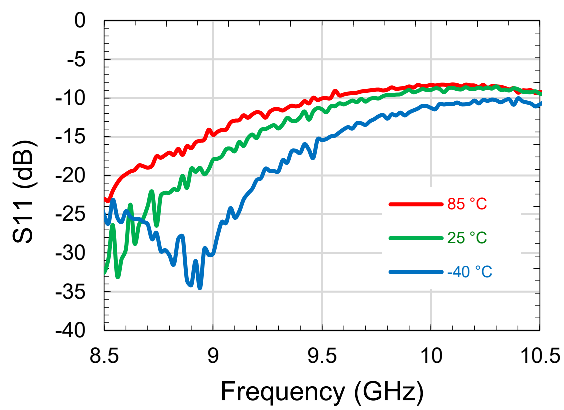
Typical Performance Curves – Small Signal over Temperature – Transmit:

I_D = 28V, I_{DQ} = 40 mA, CW, P_{IN} = -25 dBm

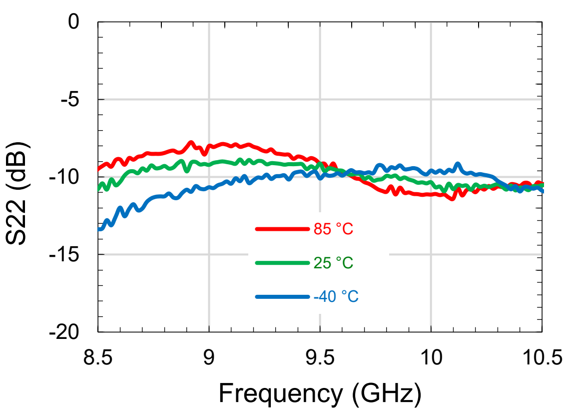
S21 vs. Frequency



S11 vs. Frequency



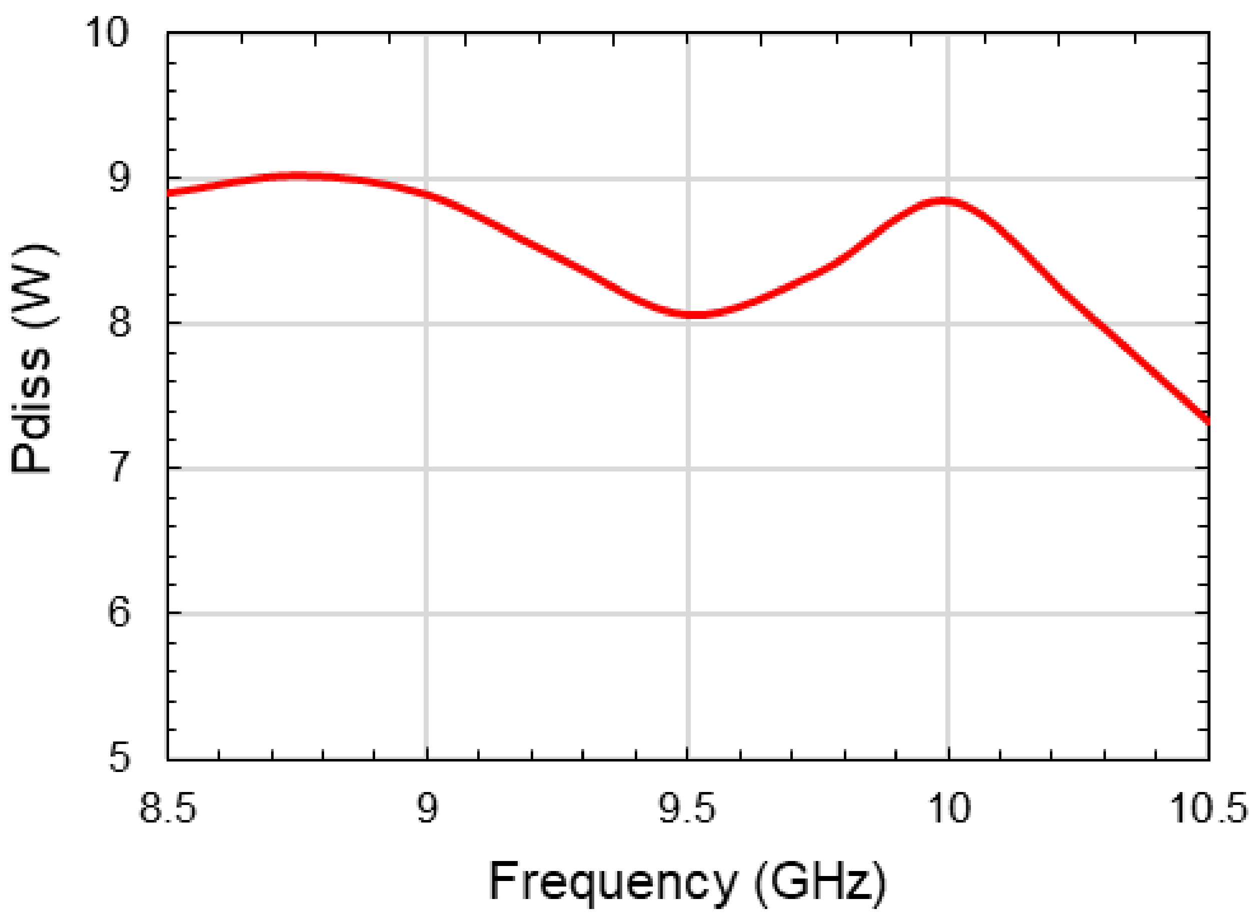
S22 vs. Frequency



Thermal Characteristics (Transmit)

Parameter	Operating Conditions	Value
Operating Junction Temperature (T_J)	Freq = 9.5 GHz, V_D = 28 V, I_{DQ} = 40 mA, I_{DRIVE} = 0.46 A, P_{IN} = 5 dBm, P_{OUT} = 36.0 dBm, P_{DISS} = 8.1 W, T_{CASE} = 85°C, 100 µs, 10%	135ºC
Thermal Resistance, Junction to Case ($R_{\theta JC}$)		6.2ºC/W

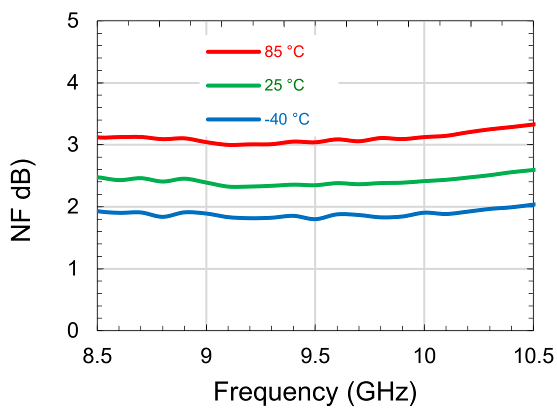
Power Dissipation vs. Frequency (T_C = 85°C)



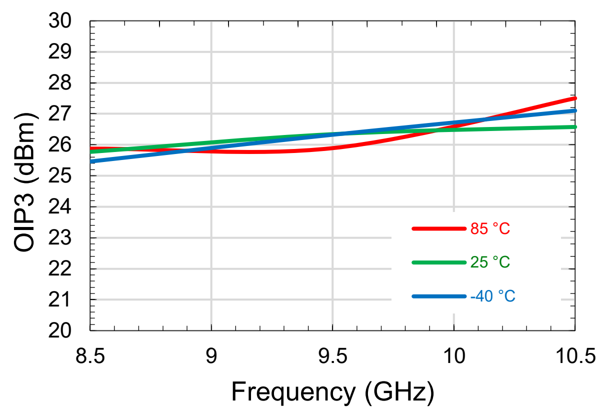
Typical Performance Curves – NF, OIP3, and P1dB over Temperature – Receive:

V_D = 2 V, I_{DQ} = 90 mA, CW, P_{IN} = -25 dBm

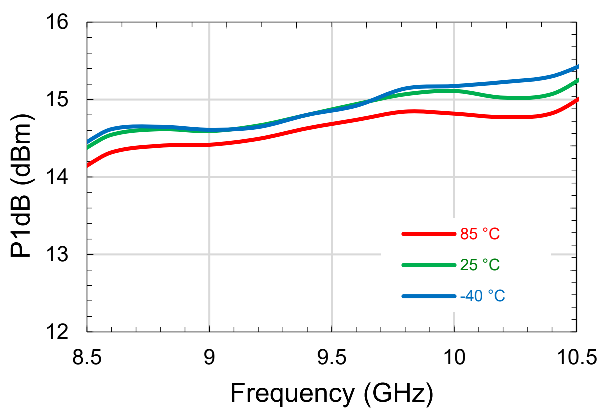
NF vs. Frequency



OIP3 vs. Frequency



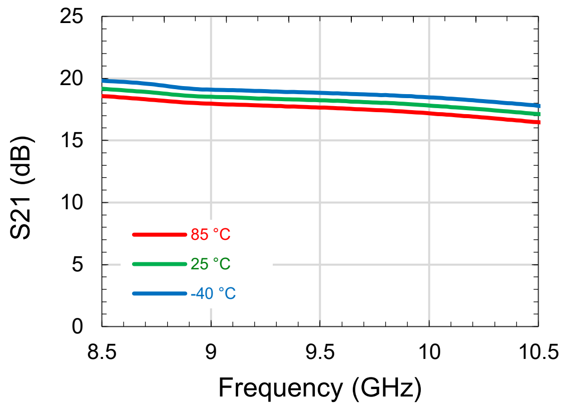
P1dB vs. Frequency



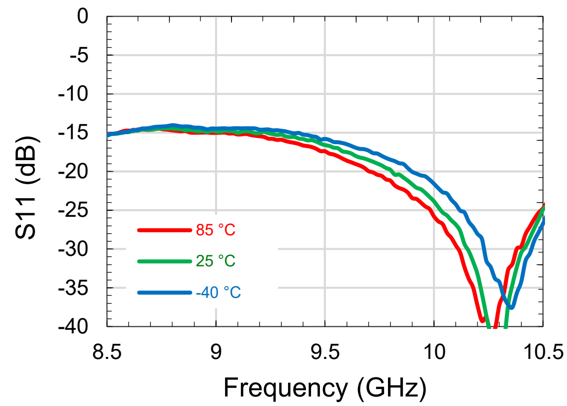
Typical Performance Curves – Small Signal over Temperature – Receive:

V_D = 2 V, I_{DQ} = 90 mA, CW, P_{IN} = -25 dBm

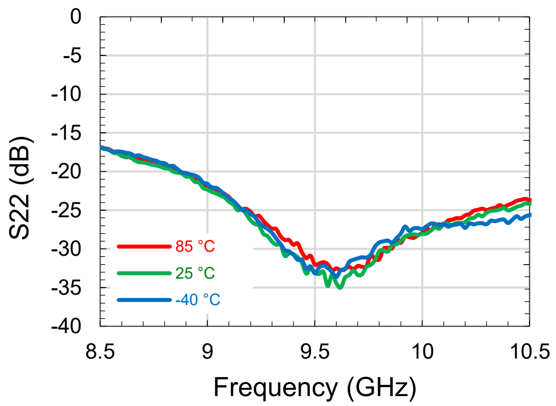
S21 vs. Frequency



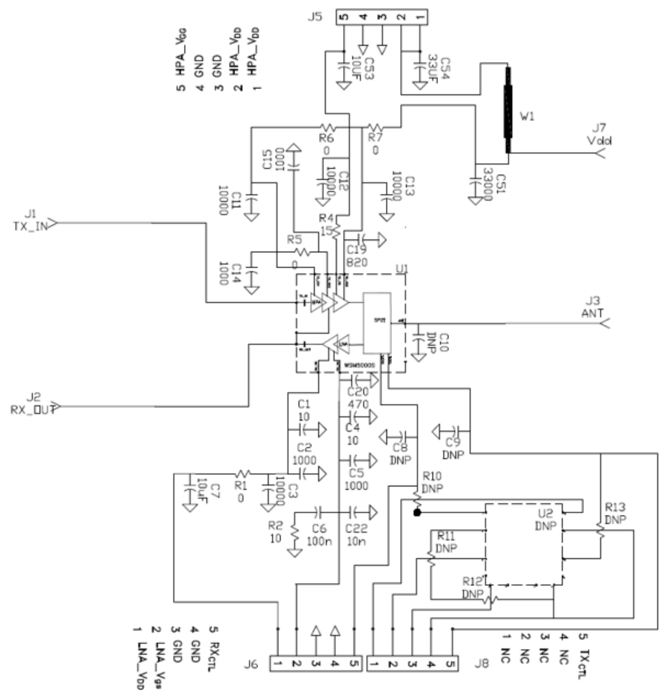
S11 vs. Frequency



S22 vs. Frequency



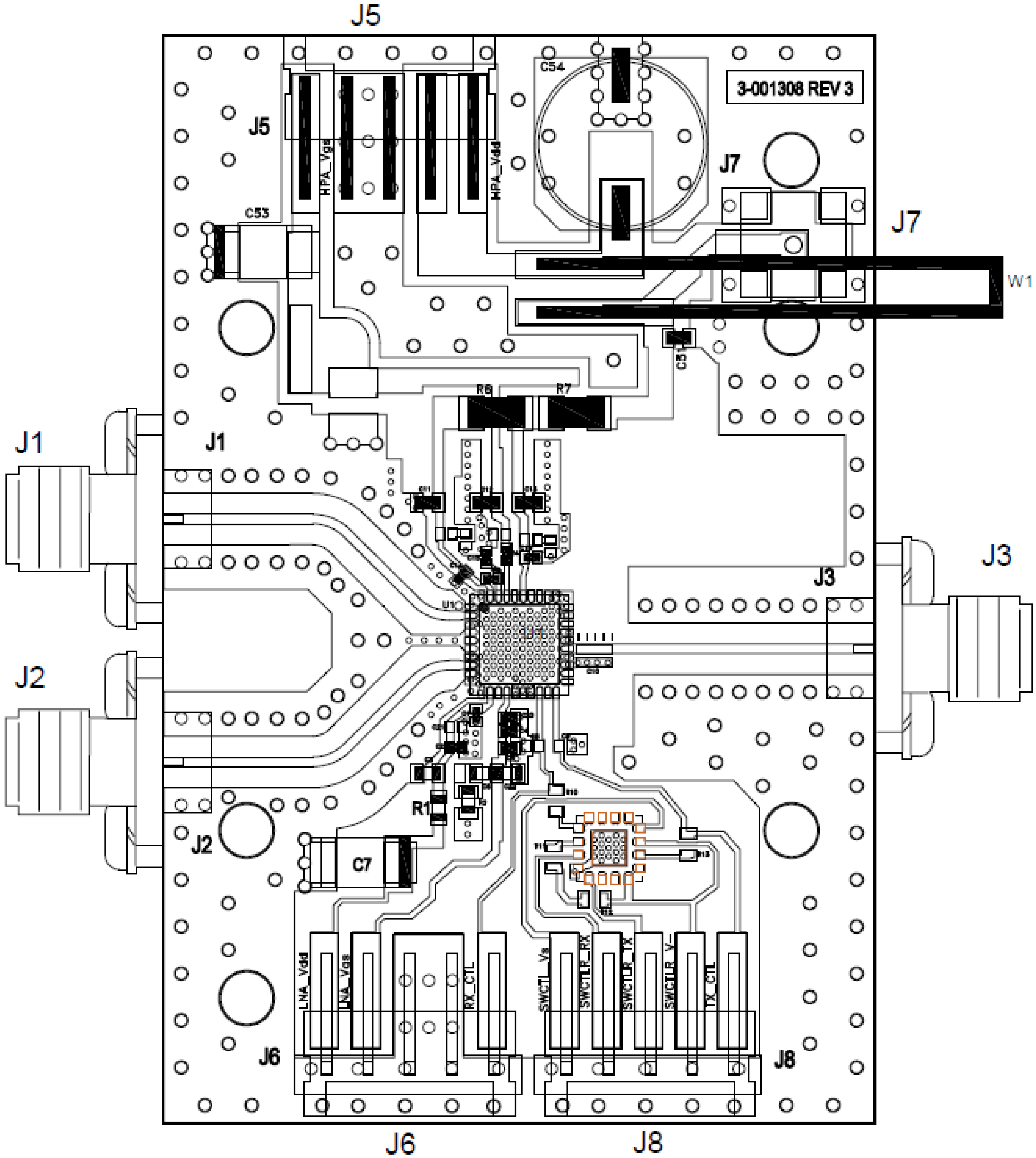
Evaluation Board Schematic (WSM5000S-AMP1)



Parts List

Part	Value	Qty
C1,C4	CAP,SMT,0402,10pF,+/-5%,50V	2
C2,C5,C14,C15	Capacitor,1000PF 100V 10% X7R 0402	4
C3,C22	Capacitor,10000pF,5%,50V,0603,COG	2
C6	Capacitor, 0.1uF, 10%, 0603 Murata	1
C11,C12,C13	CAP CER 10000PF 100V 5% X7R 0603	3
C7,C53	CAP, 10UF, 16V, TANTALUM	2
C19	Capacitor,0402,50V,COG,5%,820pF,SMT	1
C20	CAPACITOR,CER,SMT,470PF,50V,5%	1
C51	3300pF, 250V, 5%, Ceramic Cap, TDK	1
C54	CAP, 33UF, +/-20%, G CASE	1
R1	RES, SMT, 0603, 0 OHM, +/-1% TOL	1
R2	Resistor,0603,1%,1/16W,10 Ohms,SMT	1
R4	Resistor,0402,5%,1/16W,15ohm,SMT	1
R5	Chip Resistor Panasonic 0 ohm 5% 0402	1
R6,R7	Resistor, 0 ohm, 1/16W, 1206 SMD	2
W1	WIRE,22 AWG, 19STRAND, BLACK	1
J1,J2,J3	SMA Connector, PSF-S00-000	3
J7	CONN, SMB, STRAIGHT JACK RECEPTACLE, SMT	1
J5,J6,J8	Connector Header Thru Hole,Right Angle	3
	PCB Substrate, WSM5000S-AMP1	1
	Baseplate, 2.6X1.7x0.25	1
	SCREW, 2-56, SOC HD, 3/16" SS	1
	Washer, Split Lock, No. 2, OD .172	1
U1	WSM5000S	1

Evaluation Board Assembly Drawing (WSM5000S-AMP1)



Bias, Control and Handling

TX Bias On Sequence

1. Ensure RF is turned off
2. Apply pinch-off voltage of -5 V to the gate (V_G)
3. Apply nominal drain voltage (V_D)
4. Adjust Vg to obtain desired quiescent drain current (I_{DQ})
5. Apply RF

TX Bias Off Sequence

1. Turn RF off
2. Apply pinch-off to the gate (V_G = -5V)
3. Turn off drain voltage (V_D)
4. Turn off gate voltage (V_G)

Note: RX bias on and off sequencing is the same procedure as above except for replacing -5V on the gate with -2V.

Switch Control Voltage

RX_{CTL}	TX_{CTL}	ANT - RX_{OUT}	TX_{IN} - ANT
-28V	0V	On	Off
0V	-28V	Off	On

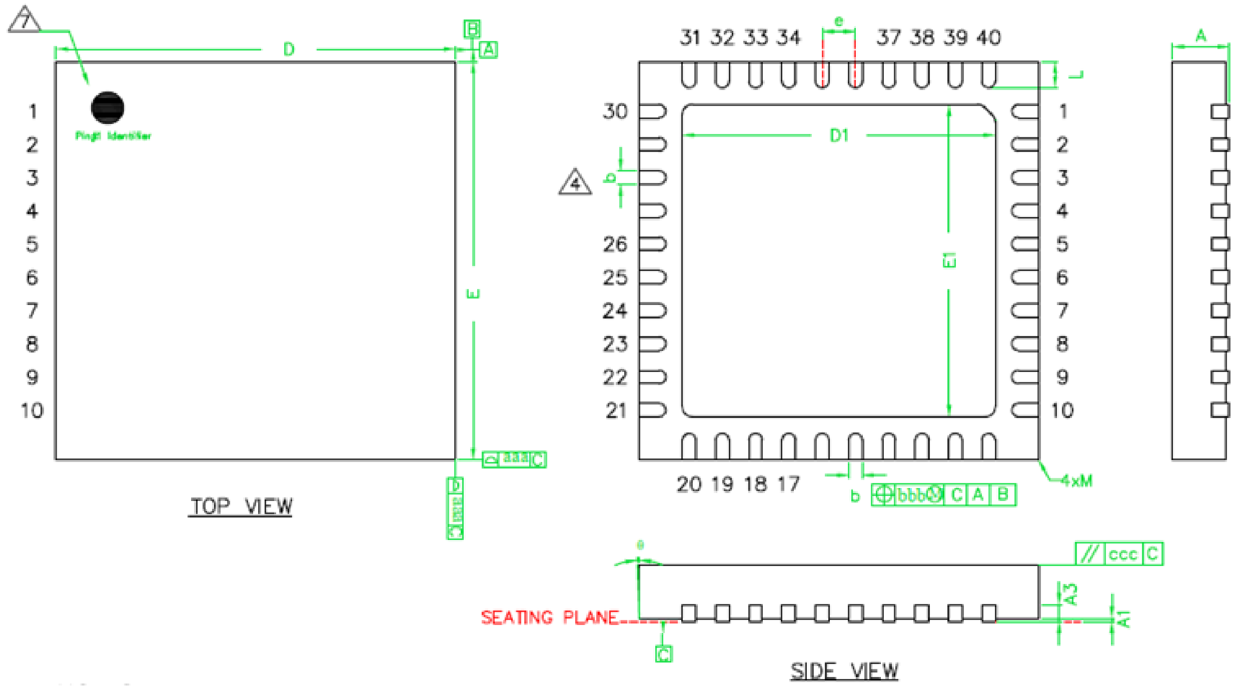
Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM class 1B and CDM class C3 devices.

Mechanical Information



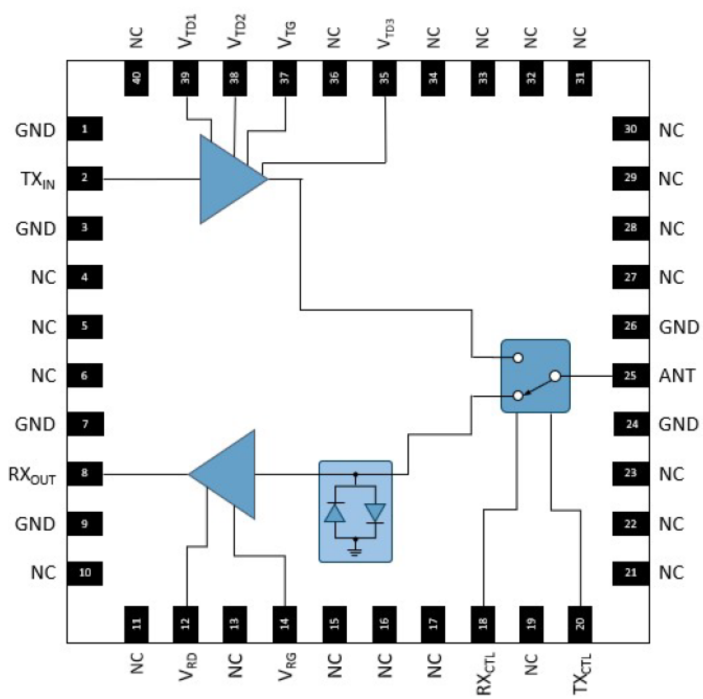
NOTES :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M. – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
5. MAX. PACKAGE WARPAGE IS 0.05 mm.
6. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
7. PIN #1 ID ON TOP WILL BE LASER MARKED.
8. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. THIS DRAWING CONFORMS TO JEDEC REGISTERED OUTLINE MO-220
10. ALL PLATED SURFACES ARE TIN 0.010 mm +/– 0.005mm.

SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3	----	0.20REF.	----
b	0.15	0.20	0.25
D	5.90	6.00	6.10
D1	----	4.7BSC	----
E	5.90	6.00	6.10
E1	----	4.7BSC	----
e	----	0.50BSC	----
L	0.30	0.40	0.50
θ	0	----	12
aaa	----	0.25	----
bbb	----	0.10	----
ccc	----	0.10	----
M	----	----	0.05

Pin Description

Pin #	Name	Description
4-6, 10, 11, 13, 15-17, 19, 21-23, 27-34, 26, 40	No Connect	No internal connection.
1, 3, 7, 9, 24, 26	GND	RF and DC ground.
2	TX_{IN}	TX input, DC blocked.
8	RX_{OUT}	RX output, DC blocked.
12	V_{RD}	Drain voltage supply for LNA in RX path.
14	V_{RG}	Gate voltage supply for LNA in RX path.
18	RX_{CTL}	Switch control voltage for RX path.
20	TX_{CTL}	Switch control voltage for TX path.
25	ANT	Antenna (common) port, DC blocked.
35	V_{TD3}	Drain voltage supply for power amplifier stage 3 in TX path.
37	V_{TG}	Gate voltage supply for power amplifier in TX path.
38	V_{TD2}	Drain voltage supply for power amplifier stage 2 in TX path.
39	V_{TD1}	Drain voltage supply for power amplifier stage 1 in TX path.



Revision History

Rev	Date	Change Description
V1A	2/21/2024	Advanced data sheet.
V1P	4/7/2025	Preliminary data sheet.
V1	12/19/2025	Production release.