

# PXAE213708NB

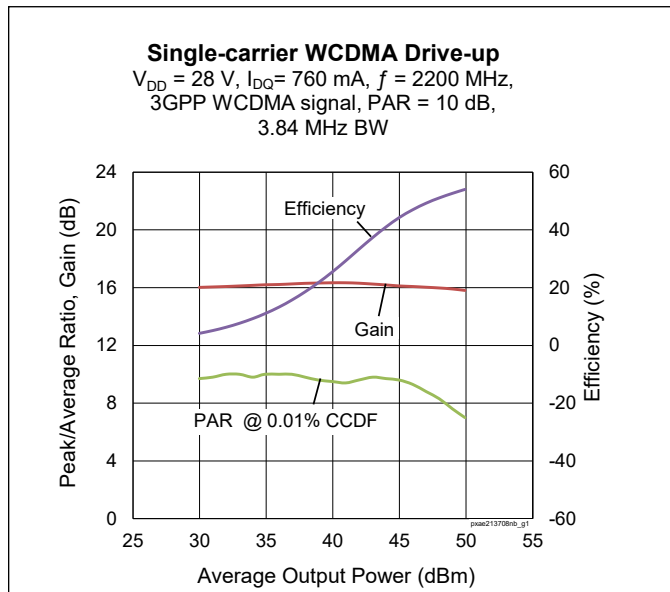
Thermally-Enhanced High Power RF LDMOS FET  
400 W, 48 V, 2110 – 2200 MHz



Package Type: PG-HB2SOF-8-1

## Description

The PXAE213708NB is a 400-watt ( $P_{3dB}$ ) LDMOS Doherty transistor intended for use in multi-standard cellular power amplifier applications in the 2110 to 2200 MHz frequency band. Features include input and output matching, high gain and thermally-enhanced package with earless flange. Manufactured with an advanced LDMOS process, this device provides excellent thermal performance and superior reliability.



## Features

- Broadband internal input and output matching
- Asymmetrical Doherty design
  - Main:  $P_{3dB} = 160\text{ W Typ}$
  - Peak:  $P_{3dB} = 290\text{ W Typ}$
- Typical Pulsed CW performance, 2200 MHz, 28 V, doherty configuration, 10  $\mu\text{s}$ , 10% duty cycle, class AB
  - Output power at  $P_{3dB} = 400\text{ W}$
  - Efficiency = 60%
  - Gain = 13.3 dB
- Capable of handling 10:1 VSWR @ 28 V, 54 W (1C WCDMA) output power
- Human Body Model Class 2 (per ANSI/ESDA/JEDEC JS-001)
- Integrated ESD protection
- Low thermal resistance
- Pb-free and RoHS compliant

## RF Characteristics

### Single-carrier WCDMA Specifications (tested in the Doherty production test circuit)

$V_{DD} = 28\text{ V}$ ,  $I_{DQ} = 700\text{ mA}$ ,  $P_{OUT} = 54\text{ W avg}$ ,  $V_{GS(PEAK)} = 1.5\text{ V}$ ,  $f = 2200\text{ MHz}$ , 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Gain	$G_{ps}$	15	16	—	dB
Drain Efficiency	$\eta_D$	48.5	52	—	%
Adjacent Channel Power Ratio	ACPR	—	-28	-25	dBc
Output PAR @ 0.01% CCDF	OPAR	7.5	8	—	dB

All published data at  $T_{CASE} = 25^\circ\text{C}$  unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!



## DC Characteristics

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-source Breakdown Voltage	$V_{BR(DSS)}$	65	—	—	V	$V_{GS} = 0\text{ V}, I_{DS} = 10\text{ mA}$
Drain Leakage Current (main) (peak)	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 28\text{ V}, V_{GS} = 0\text{ V}$
		—	—	10		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$
Gate Leakage Current	$I_{GSS}$	—	—	1	$\mu\text{A}$	$V_{GS} = 10\text{ V}, V_{DS} = 0\text{ V}$
On-State Resistance (main) (peak)	$R_{DS(on)}$	—	0.08	—	W	$V_{GS} = 10\text{ V}, V_{DS} = 0.1\text{ V}$
		—	0.05	—		
Operating Gate Voltage (main) (peak)	$V_{GS}$	2.85	3.05	3.35	V	$V_{DS} = 28\text{ V}, I_{DQ} = 760\text{ mA}$
		—	1.5	—		$V_{DS} = 28\text{ V}, I_{DQ} = 0\text{ mA}$

## Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source Voltage	$V_{DSS}$	65	V
Gate-source Voltage	$V_{GS}$	-6 to +10	
Operating Voltage	$V_{DD}$	0 to +32	
Junction Temperature	$T_J$	225	$^{\circ}\text{C}$
Storage Temperature Range	$T_{STG}$	-65 to +150	

1. Operation above the maximum values listed here may cause permanent damage. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the component. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For reliable continuous operation, the device should be operated within the operating voltage range ( $V_{DD}$ ) specified above.
2. Product's qualification were performed at 225 °C. Operation at  $T_J$  (275 °C) reduces median time to failure.

## Thermal Characteristics

Parameter	Symbol	Value	Unit	Conditions
Thermal Resistance (main)	$R_{\theta JC}$	0.60	$^{\circ}\text{C}/\text{W}$	$T_{CASE} = 70^{\circ}\text{C}, 54\text{ W CW}$
Thermal Resistance (peak)		0.22		$T_{CASE} = 70^{\circ}\text{C}, 282\text{ W CW}$

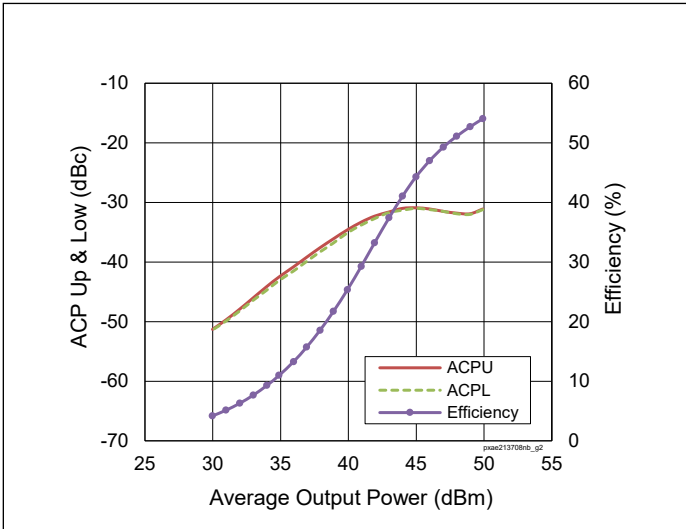
## Moisture Sensivity Level

Level	Test Signal	Package Temperature	Unit
3	IPC/JEDEC J-STD-020	260	$^{\circ}\text{C}$

## Ordering Information

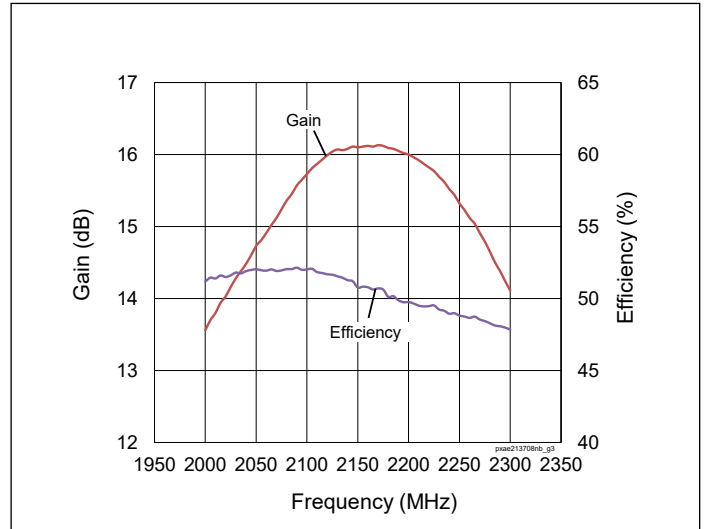
Type and Version	Order Code	Package Description	Shipping
PXAE213708NB V1 R2	PXAE213708NB-V1-R2	PG-HB2SOF-8-1	Tape & Reel, 250 pcs

**Typical Performance** (data taken in test fixture)



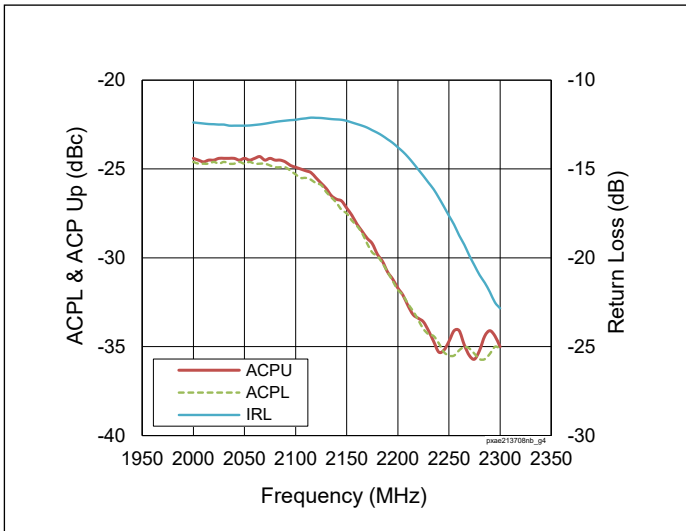
**Figure 1.** Single-carrier WCDMA Drive-up

$V_{DD} = 28\text{ V}$ ,  $I_{DQ(MAIN)} = 760\text{ mA}$ ,  $f = 2200\text{ MHz}$ ,  
 3GPP WCDMA signal, PAR = 10 dB,  
 BW = 3.84 MHz



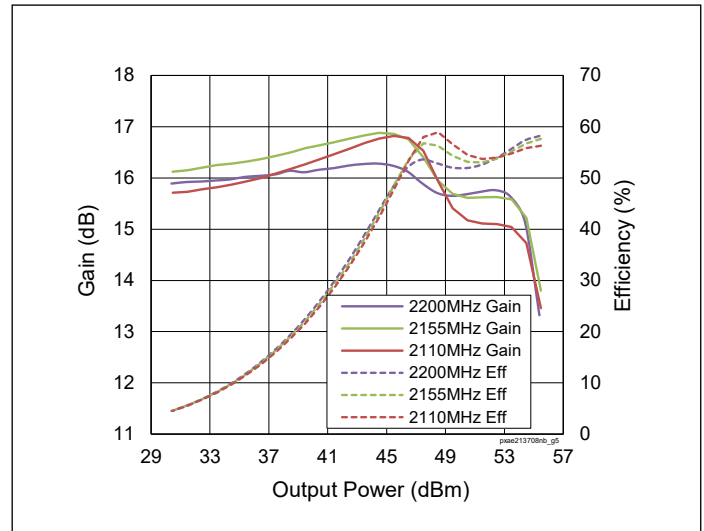
**Figure 2.** Single-carrier WCDMA Broadband

$V_{DD} = 28\text{ V}$ ,  $I_{DQ} = 760\text{ mA}$ ,  $P_{OUT} = 47.32\text{ dBm}$ ,  
 3GPP WCDMA signal, PAR = 10 dB



**Figure 3.** Single-carrier WCDMA Broadband

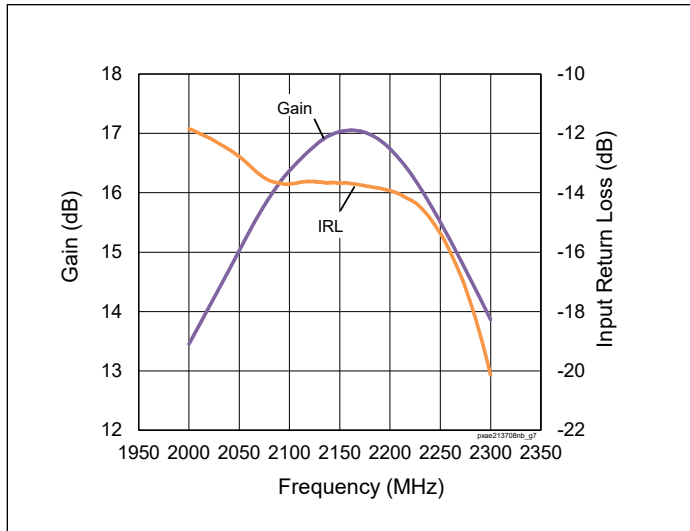
$V_{DD} = 28\text{ V}$ ,  $I_{DQ} = 760\text{ mA}$ ,  $P_{OUT} = 47.32\text{ dBm}$ ,  
 3GPP WCDMA signal, PAR = 10 dB



**Figure 4.** CW Performance

$V_{DD} = 28\text{ V}$ ,  $I_{DQ} = 760\text{ mA}$

**Typical Performance** (cont.)



**Figure 5.** Small Signal CW Gain & Input Return Loss

$V_{DD} = 28\text{ V}$ ,  $I_{DQ} = 760\text{ mA}$

**Load Pull Performance**

**Main side load pull performance** – pulsed CW signal: 10  $\mu\text{sec}$ , 10% duty cycle, 28 V,  $I_{DQ} = 850\text{ mA}$ , class AB

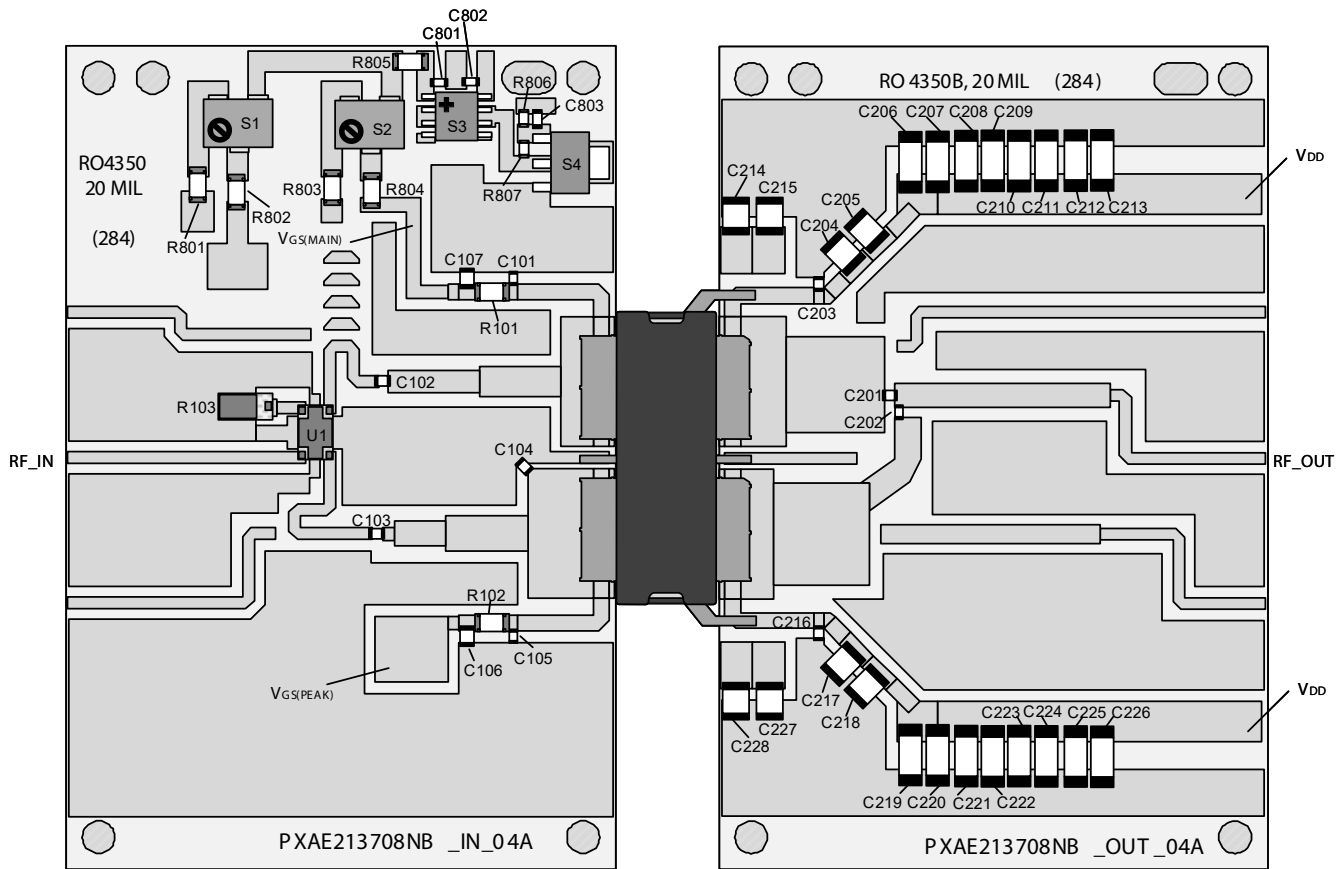
		<b>P<sub>3dB</sub></b>									
		<b>Max Output Power</b>					<b>Max Drain Efficiency</b>				
Freq [MHz]	Z <sub>s</sub> [Ω]	Z <sub>l</sub> [Ω]	Gain [dB]	P <sub>OUT</sub> [dBm]	P <sub>OUT</sub> [W]	η <sub>D</sub> [%]	Z <sub>l</sub> [Ω]	Gain [dB]	P <sub>OUT</sub> [dBm]	P <sub>OUT</sub> [W]	η <sub>D</sub> [%]
2110	6.88-j10.14	1.45-j3.46	16.35	52.75	188.4	56.72	2.75-j2.93	17.79	51.61	144.9	65.59
2155	10.79-j12.22	1.43-j3.59	16.36	52.82	191.4	57.65	2.78-j2.65	18.02	51.22	132.4	66.44
2200	17.44-j10.37	1.26-j3.83	16.25	52.99	199.1	57.69	2.35-j2.75	18.14	51.32	135.5	67.40

**Peak side load pull performance** – pulsed CW signal: 10  $\mu\text{sec}$ , 10% duty cycle, 28 V,  $I_{DQ} = 10\text{ mA}$ , class B

		<b>P<sub>3dB</sub></b>									
		<b>Max Output Power</b>					<b>Max Drain Efficiency</b>				
Freq [MHz]	Z <sub>s</sub> [Ω]	Z <sub>l</sub> [Ω]	Gain [dB]	P <sub>OUT</sub> [dBm]	P <sub>OUT</sub> [W]	η <sub>D</sub> [%]	Z <sub>l</sub> [Ω]	Gain [dB]	P <sub>OUT</sub> [dBm]	P <sub>OUT</sub> [W]	η <sub>D</sub> [%]
2110	2.39-j6.39	3.90-j5.38	14.77	54.79	301.3	52.77	3.65-j2.94	15.59	53.90	245.5	58.76
2155	4.53-j7.79	3.94-j5.41	14.74	54.86	306.2	53.59	3.31-j2.66	15.65	53.71	235.0	61.20
2200	7.76-j6.76	3.90-j5.30	17.93	54.90	309.0	54.90	2.93-j2.88	15.82	53.66	232.3	63.25

**Reference Circuit, 2110 – 2200 MHz**

Test Circuit Part Number	LTA/PXAE213708NB-V1
PCB Information	Rogers 4350, 0.508 mm [0.020"] thick, 2 oz. copper, $\epsilon_r = 3.66$

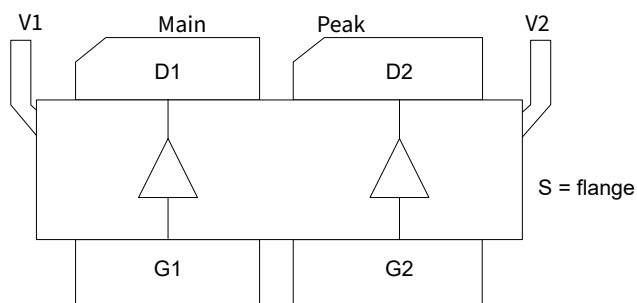


Reference circuit assembly diagram (not to scale)

## Components Information

Component	Description	Manufacturer	P/N
<b>Input</b>			
C101, C102, C103, C105	Capacitor, 33 pF	ATC	ATC800A330JT250XT
C104	Capacitor, 0.7 pF	ATC	ATC800A0R7BT250XT
C106, C107	Capacitor, 0.1 $\mu$ F	Murata Electronics North America	GCM21BR71H104KA37K
R101, R102	Resistor, 2.49 ohms	Vishay Dale	CRCW12062R49FKEA
R103	Resistor, 50 ohms	Richardson	C8A50Z4A
U1	Hybrid Coupler	Anaren	X3C20F1-02S
C801, C802, C803	Capacitor, 1000 pF	Murata Electronics North America	GRM188R71H102KA01J
R801, R802, R804, R805	Resistor, 10 ohms	Panasonic Electronic Components	ERJ-8GEYJ100V
R803	Resistor, 5.6 ohms	Panasonic Electronic Components	ERJ-8RQJ5R6V
R806	Resistor, 1.3K ohms	Panasonic Electronic Components	ERJ-3GEYJ132V
R807	Resistor, 1.2K ohms	Panasonic Electronic Components	ERJ-3GEYJ122V
S1, S2	Resistor, 2K ohms	Bourns Inc.	3224W-1-202E
S3	Voltage Regulator	Texas Instruments	LM78L05ACM
S4	Transistor	Diodes Incorporated	BCP5616TA
<b>Output</b>			
C201	Capacitor, 4.7 pF	ATC	ATC800A7R7BT250XT
C202, C203, C216	Capacitor, 33 pF	ATC	ATC800A330JT250XT
C204, C205, C214, C215, C217, C218, C227, C228	Capacitor, 100 V, 10 $\mu$ F	Murata Electronics North America	GRM32EC72A106KE05L
C206, C207, C208, C209, C210, C211, C212, C213, C219, C220, C221, C222, C223, C224, C225, C226	Capacitor, 100 V, 10 $\mu$ F	TDK Corporation	C5750X7S2A106M230KB

## Pinout Diagram (top view)

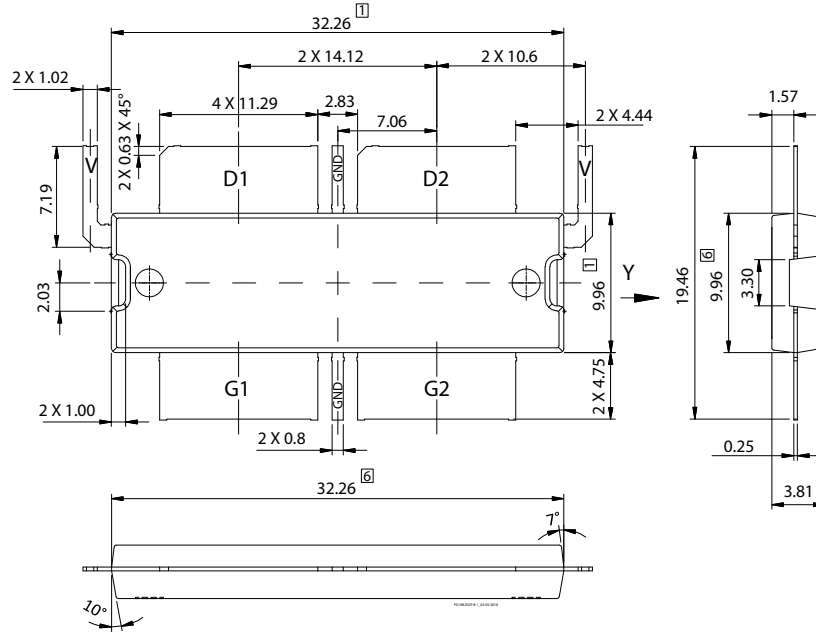


Pin	Description
D1	Drain Device 1 (Main)
D2	Drain Device 2 (Peak)
G1	Gate Device 1(Main)
G2	Gate Device 2 (Peak)
GND	Ground
V1, V2	Drain video decoupling, no DC bias

Lead connections for PXAE213708NB

**Package Outline Specifications – Package PG-HB2SOF-8-1**

Top and Side View



Bottom View

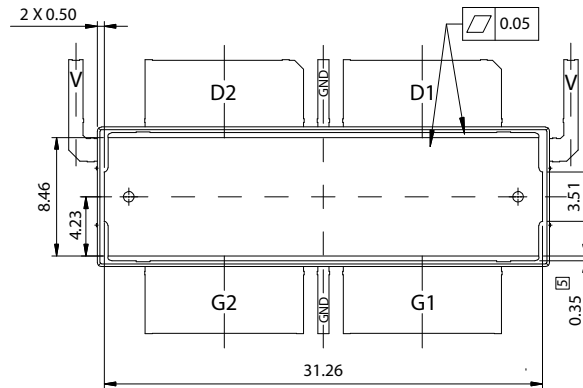


Diagram Notes—unless otherwise specified:

1. Mold/Dam Bar/Metal protusion of 0.30mm max per side not included.
2. Fillets and radii: all radii are 0.3 mm max unless specified otherwise
3. Interpret dimensions and tolerances per ISO 8015
4. Dimensions are mm
5. Exposed metal surface are tin plated, may not be covered by mold compound
6. Does not include mold/dam bar/metal protusion.
7. All tolerances  $\pm 0.1$ mm unless specified otherwise
9. All metal surfaces pre-plated, except area of cut
9. Lead thickness: 0.25 mm
10. Pins: D1, D2 – drain; G1, G2 – gate; GND – ground; V – Drain video decoupling, no DC bias

## Notes & Disclaimer

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