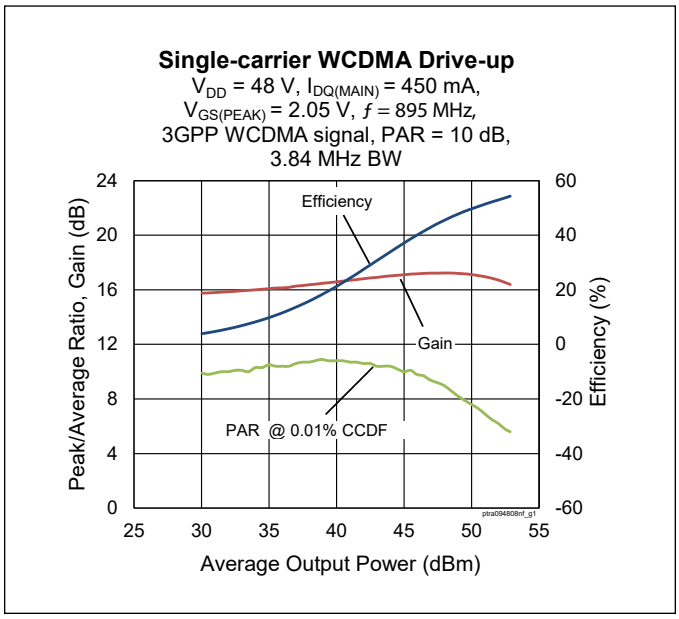
PTRA094808NF

Thermally-Enhanced High Power RF LDMOS FET
480 W, 48 V, 859 – 960 MHz

Package Types: PG-HBSOF-6-2
PN: PTRA094808NF

Description

The PTRA094808NF is a 480-watt LDMOS FET intended for use in multi-standard cellular power amplifier applications in the 859 to 960 MHz frequency band. Features include input and output matching, high gain and thermally-enhanced package with earless flange. Manufactured with an advanced LDMOS process, this device provides excellent thermal performance and superior reliability.



Features

- Broadband internal input and output matching
- Asymmetrical design
  - Main: P_{1dB} = 210 W Typ
  - Peak: P_{1dB} = 340 W Typ
- Typical Pulsed CW performance, 896 MHz, 48 V, Doherty configuration
  - Output power at P_{1dB} = 300 W
  - Output power at P_{3dB} = 420 W
  - Efficiency = 53%
  - Gain = 17.5 dB
- Capable of handling 10:1 VSWR @ 48 V, 100 W (CW) output power
- Integrated ESD protection
- Human Body Model class 1C (per ANSI/ESDA/JEDEC JS-001)
- Low thermal resistance
- Pb-free and RoHS compliant

RF Characteristics

Single-carrier WCDMA Specifications (tested in the Doherty production test fixture)
V_{DD} = 48 V, I_{DQ} = 450 mA, $V_{GS(PEAK)}$ = 2.05 V, P_{OUT} = 87 W avg, ƒ = 895 MHz, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Linear Gain	G_{ps}	16.5	17.5	—	dB
Drain Efficiency	η_D	48.5	52.5	—	%
Adjacent Channel Power Ratio	ACPR	—	–30.5	–26.5	dBc
Output PAR @ 0.01% CCDF	OPAR	7.1	7.5	—	dB

Note:
All published data at T_{CASE} = 25°C unless otherwise indicated
ESD: Electrostatic discharge sensitive device—observe handling precautions!

RoHS compliant

DC Characteristics (each side)

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-Source Breakdown Voltage	$V_{BR(DSS)}$	105	—	—	V	V_{GS} = 0 V, I_{DS} = 10 mA
Drain Leakage Current	I_{DSS}	—	—	1	µA	V_{DS} = 48 V, V_{GS} = 0 V
		—	—	10		V_{DS} = 105 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}	—	—	1		V_{GS} = 14 V, V_{DS} = 0 V
On-State Resistance (main)	$R_{DS(on)}$	—	0.08	—	Ω	V_{GS} = 10 V, V_{DS} = 0.1 V
On-State Resistance (peak)		—	0.05	—		
Operating Gate Voltage (main)	V_{GS}	3	3.5	4	V	V_{DS} = 48 V, I_{DQ} = 0.45 A
Operating Gate Voltage (peak)		—	2.05	—		V_{DS} = 48 V, I_{DQ} = 0 A

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source Voltage	V_{DSS}	105	V
Gate-source Voltage	V_{GS}	–6 to +12	
Operating Voltage	V_{DD}	0 to +55	
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	

1. Operation above the maximum values listed here may cause permanent damage. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the component. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For reliable continuous operation, the device should be operated within the operating voltage range (V_{DD}) specified above.
2. Parameters values can be affected by end application and product usage. Values may change over time.

Thermal Characteristics

Characteristics	Symbol	Value	Unit	Conditions
Thermal Resistance (Main)	$R_{\theta JC}$	0.51	°C/W	T_{CASE} = 70°C, 87.1 W CW

Moisture Sensitivity Level

Level	Test Signal	Package Temperature	Unit
3	IPC/JEDEC J-STD-020	260	°C

Ordering Information

Type and Version	Order Code	Package and Description	Shipping
PTRA094808NF V1 R5	PTRA094808NF-V1-R5	PG-HBSOF-6-2	Tape & Reel, 500 pcs

Typical RF Performance (data taken in production test fixture)

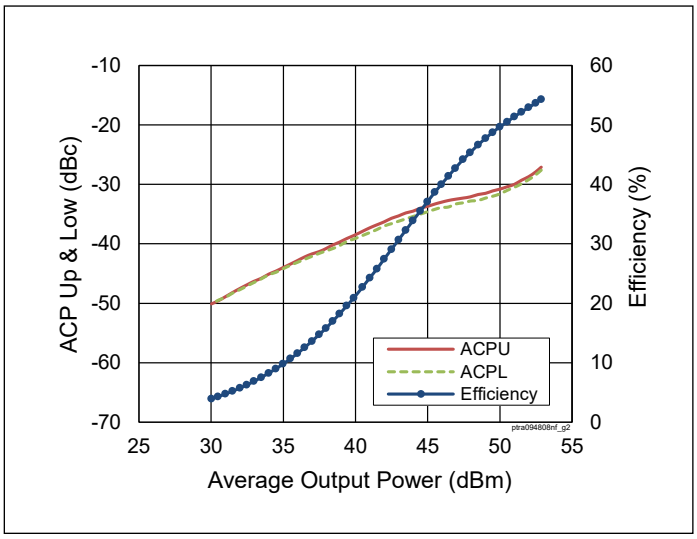


Figure 1. Single-carrier WCDMA Drive-up

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 450 mA,
$V_{GS(PEAK)}$ = 2.05 V, f = 895MHz,
3GPP WCDMA signal, PAR = 10 dB,
BW = 3.84 MHz

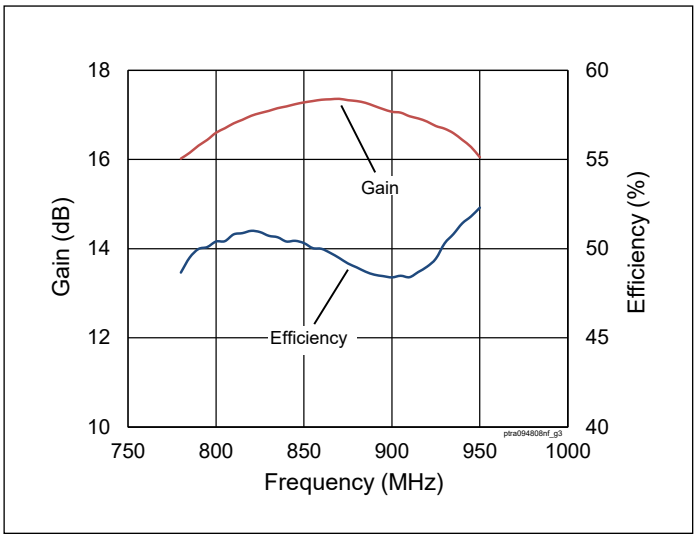


Figure 2. Single-carrier WCDMA Broadband Performance

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 450 mA,
$V_{GS(PEAK)}$ = 2.05 V, P_{OUT} = 49.4 dBm,
3GPP WCDMA signal, PAR = 10 dB

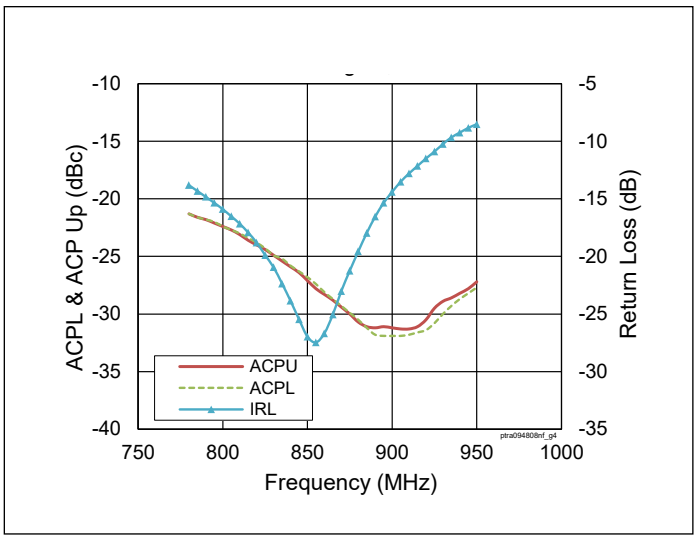


Figure 3. Single-carrier WCDMA Broadband Performance

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 450 mA,
$V_{GS(PEAK)}$ = 2.05 V, P_{OUT} = 49.4 dBm,
3GPP WCDMA signal, PAR = 10 dB

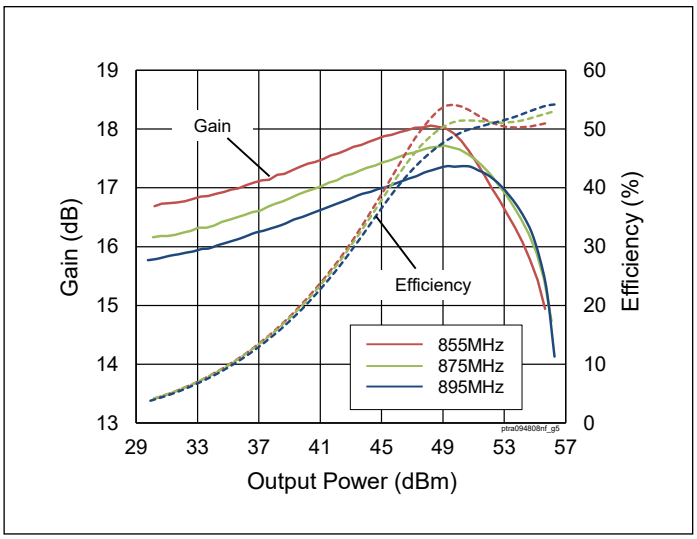


Figure 4. CW Performance

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 450 mA,
$V_{GS(PEAK)}$ = 2.05 V

Typical Performance (cont.)

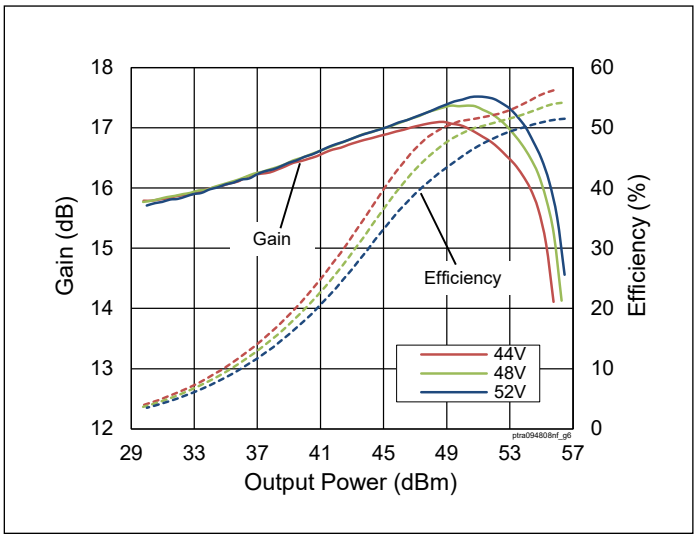


Figure 5. CW Performance at various V_{DD}

$I_{DQ(MAIN)}$ = 450 mA, $V_{GS(PEAK)}$ = 2.05 V,
f = 895 MHz

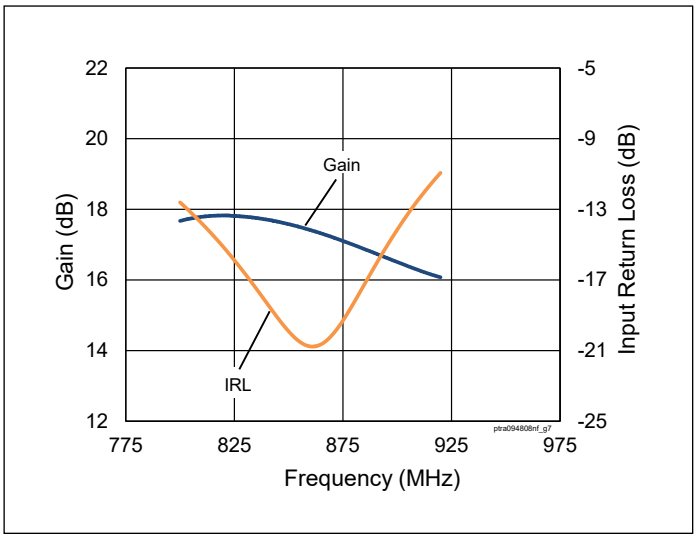


Figure 6. CW Performance Small Signal Gain & Input Return Loss

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 450 mA,
$V_{GS(PEAK)}$ = 2.05 V

Load Pull Performance

Main Side Load Pull Performance – Pulsed CW signal: 10 µsec, 10% duty cycle, V_{DD} = 48 V, I_{DQ} = 350 mA, class AB

		P_{1dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{1dB} [dBm]	P_{1dB} [W]	ηD [%]	Zl [Ω]	Gain [dB]	P_{1dB} [dBm]	P_{1dB} [W]	ηD [%]
865	1.4-j4.1	1.93-j1.35	20.25	53.40	219	57.4	4.16-j0.34	22.1	51.50	141	67.2
880	1.6-j4.65	1.67-j1.24	19.8	53.40	219	54.6	4.0-j0.5	22.1	51.50	141	67.7
895	2.0-j4.33	1.87-j1.62	20	53.37	217	56.7	4.08-j0.33	22	51.37	137	67.6

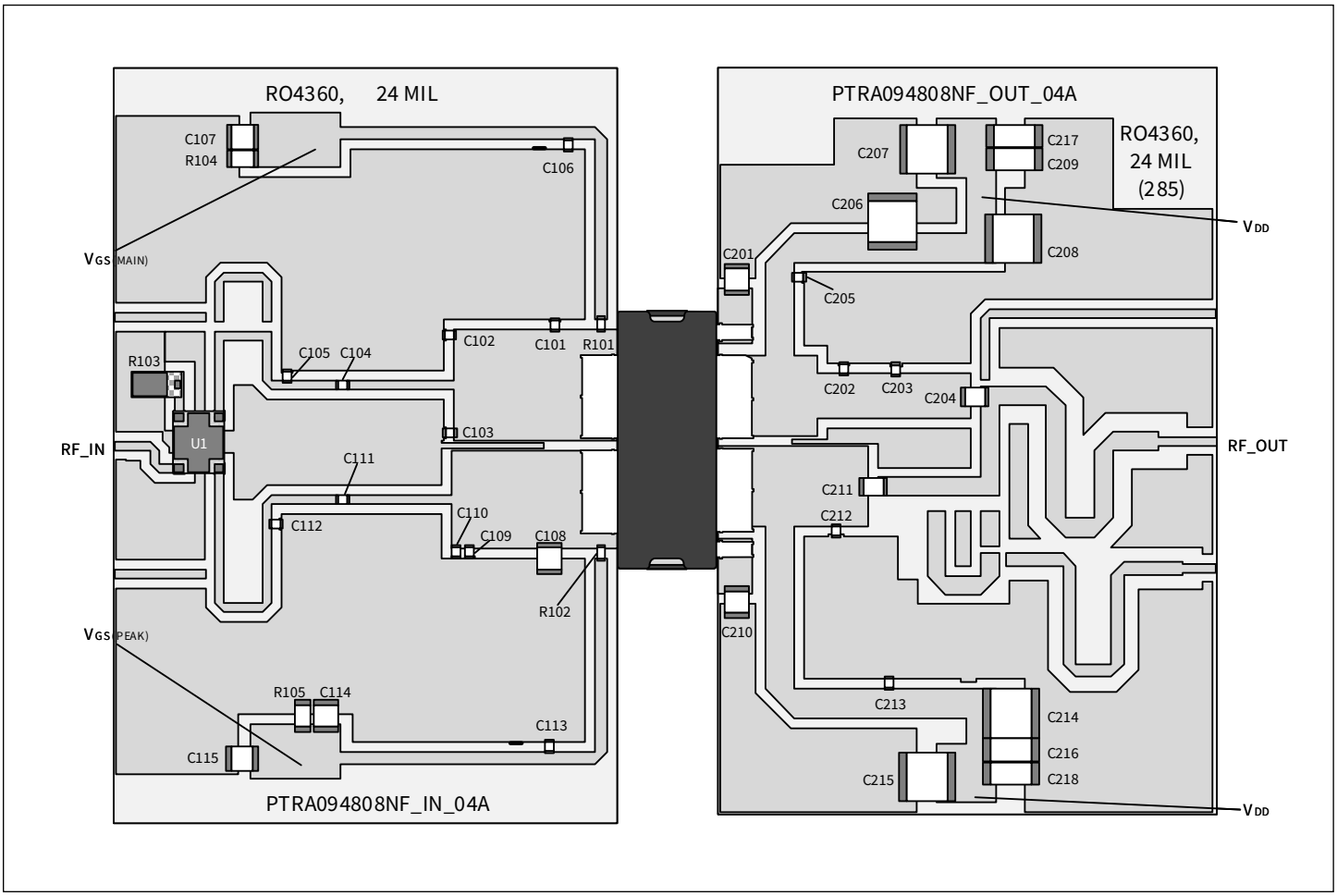
		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]
865	1.4-j4.1	2.09-1.87	18.4	54.30	270	61.8	3.8+0	20	52.62	182	69.1
880	1.6-j4.65	1.87-1.73	18	54.20	263	58.7	3.56+0.05	19.85	52.67	184	69.5
895	2.0-j4.33	1.81-1.78	17.9	54.20	263	59.1	3.33+0.04	19.73	52.65	184	69.43

Peak Side Load Pull Performance – Pulsed CW signal: 10 µsec, 10% duty cycle, V_{DD} = 48 V, $V_{GS(PEAK)}$ = 2 V, class C

		P_{1dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{1dB} [dBm]	P_{1dB} [W]	ηD [%]	Zl [Ω]	Gain [dB]	P_{1dB} [dBm]	P_{1dB} [W]	ηD [%]
865	1.57-j3.71	1.17-j1.97	16	55.80	380	58.8	1.01-j0.55	17.1	53.17	207	71.1
880	1.58-j3.55	1.15-j3.55	16	55.70	372	59.0	1.08-j0.83	17	53.70	234	70.9
895	1.82-3.82	1.14-j2.05	16	55.84	384	60.9	1.11-j1.04	16.9	54.10	257	71.1

		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]
865	1.57-j3.71	1.2-1.97	14	56.68	466	61.9	1.17-0.93	15.1	55.12	325	71.2
880	1.58-j3.55	1.32-2.11	13.8	56.46	443	60.6	1.15-1.05	15	55.00	316	70.7
895	1.82-3.82	1.19-2.09	13.9	56.59	456	62.4	1.05-1.04	14.8	54.72	296	71.0

Evaluation Board, 869 – 894 MHz



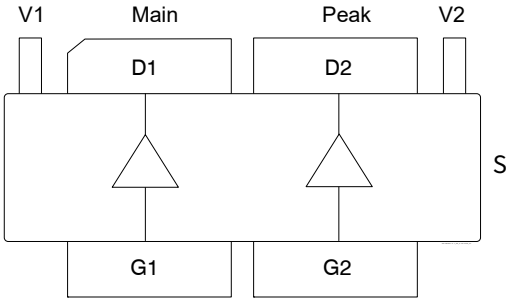
Reference circuit assembly diagram (not to scale)

Evaluation Board Part Number	LTA/PTRA094808NF-V1
PCB Information	Rogers 4360, 0.609 mm [0.024”] thick, 2 oz. copper, ε_r = 6.15

Components Information

Component	Description	Manufacturer	P/N
Input			
C101	Capacitor, 6.8 pF	ATC	ATC600F6R8BT250T
C102	Capacitor, 2.7 pF	ATC	ATC600F2R7BT250T
C103, C105	Capacitor, 1.8 pF	ATC	ATC600F1R8BT250T
C104, C111	Capacitor, 33 pF	ATC	ATC600F330JT250T
C106, C113	Capacitor, 68 pF	ATC	ATC600F680JT250T
C107, C114, C115	Capacitor, 10 µF	Taiyo Yuden	UMK325C7106MM-T
C108	Capacitor, 8.2 pF	ATC	ATC100B8R2BT500XB
C109	Capacitor, 2.0 pF	ATC	ATC600F2R0BT250T
C110	Capacitor, 1.0 pF	ATC	ATC600F1R0BT250T
C112	Capacitor, 3.3 pF	ATC	ATC600F3R3BT250T
R101, R102	Resistor, 5.6 Ω	Panasonic Electronic Components	ERJ-8RQJ5R6V
R103	Resistor, 50 Ω	Anaren	C16A50Z4
R104, R105	Resistor, 1,000 Ω	Panasonic Electronic Components	ERJ-8GEYJ102V
U1	Hybrid coupler	CEMAX	CMX09Q02
Output			
C201, C210	Capacitor, 10 µF	Taiyo Yuden	UMK325C7106MM
C202	Capacitor, 10 pF	ATC	ATC600F100JT250T
C203	Capacitor, 1.5 pF	ATC	ATC600F1R5CT250T
C204	Capacitor, 20 pF	ATC	ATC100B200JT500XB
C205	Capacitor, 68 pF	ATC	ATC600F680JT250T
C206, C207, C208, C209, C214, C215, C216, C217, C218	Capacitor, 10 µF, 100 V	TDK Corporation	C5750X7S2A106M230KB
C211	Capacitor, 47 pF	ATC	ATC100B470JT500XB
C212	Capacitor, 12 pF	ATC	ATC600F120JT250T
C213	Capacitor, 47 pF	ATC	ATC600F470JT250T

Pinout Diagram (top view)



Pin	Description
D1	Drain Device 1 (Main)
D2	Drain Device 2 (Peak)
G1	Gate Device 1 (Main)
G2	Gate Device 2 (Peak)
S	Source (flange)
V1	Drain video decoupling, no DC bias
V2	NC or connected to ground

Package Outline Specifications – Package PG-HBSOF-6-2

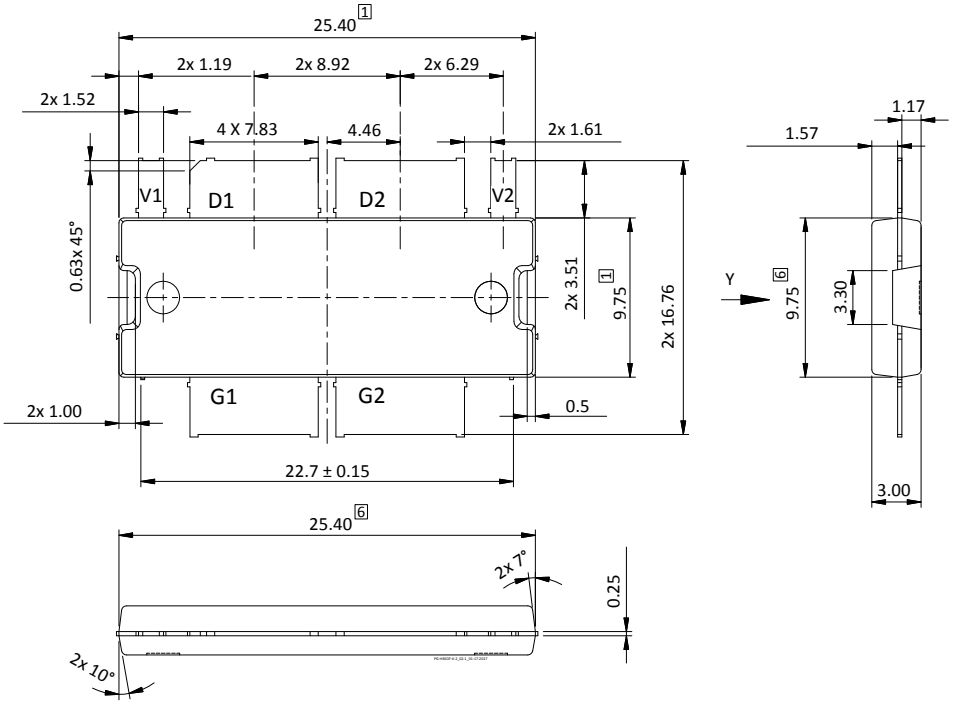
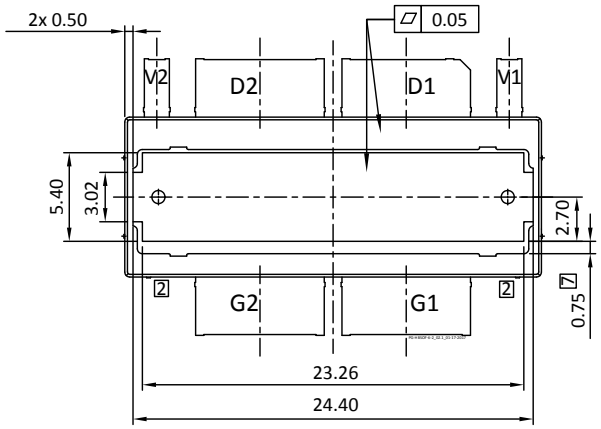


Diagram Notes—unless otherwise specified:

1. Mold/dam bar/metal protrusion of 0.30 mm max per side not included.
2. Metal protrusions are connected to source and shall not exceed 0.10 mm max.
3. Fillets and radii: all radii are 0.3 mm max.
4. Interpret dimensions and tolerances per ISO 8015.
5. Dimensions are mm.
6. Does not include mold/dam bar and metal protrusion.
7. Exposed metal surface is tin-plated, may not be covered by mold compound.
8. All tolerances ± 0.1 mm unless specified otherwise.
9. All metal surfaces are tin-plated, except area of cut.
10. Lead thickness: 0.25 mm.
11. Pins: D1, D2 = drain; G1, G2 = gate; S = source; V1 = drain video decoupling, no DC Bias, V2 = NC or connected to GRD

Package Outline Specifications – Package PG-HBSOF-6-2 (bottom view)



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