

## Features

- Supports up to 40 W Power
- Low Insertion Loss:
  - 0.10 dB to 2.7 GHz
  - 0.25 dB to 6.0 GHz
- High Isolation:
  - 26 dB to 6.0 GHz
- RoHS\* Compliant

## Applications

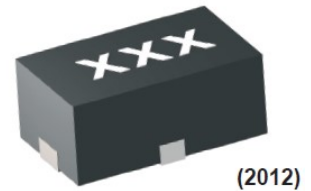
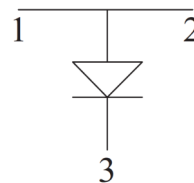
- Wireless Telecommunications Infrastructure
- Test Instrument Applications

## Description

A broadband, high linearity, medium power shunt switch element in a 1.9 x 1.1 mm DFN package.

This device is designed for wireless telecommunications infrastructure and test instrument applications. It is also suited for other applications in 0.05 ~ 6 GHz.

## Pin Out / Schematic



## Ordering Information

Part Number	Package
MSWSH-040-30	3000 piece reel

## Electrical Specifications: $T_A = +25^\circ\text{C}$

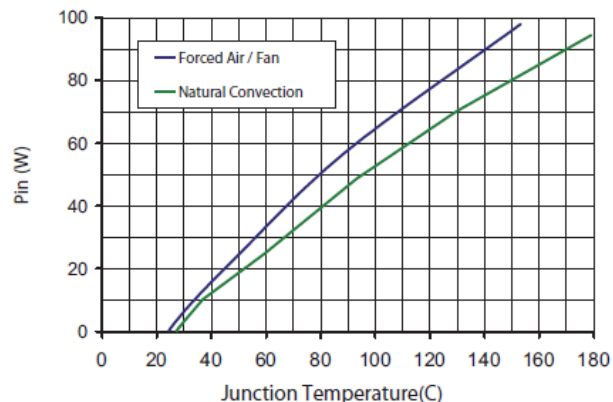
Parameter	Test Conditions	Units	Min.	Typ.	Max.
Breakdown Voltage ( $V_B$ )	$I_R = 10 \mu\text{A}$	V	500	—	—
Total Capacitance ( $C_T$ )	$V_R = -50 \text{ V}$ , 1 MHz	pF	—	0.42	—
Series Resistance ( $R_S$ )	$I_F = 100 \text{ mA}$ , 500 MHz	$\Omega$	—	0.36	—
I-Region (W)	I-Layer	mm	—	40	—
Insertion Loss ( $I_L$ )	$V_R = 10 \text{ V}$ 2.7 GHz <6.0 GHz	dB	—	0.10 0.30	0.30 0.50
Isolation ( $I_{SO}$ )	$I_F = 100 \text{ mA}$ 2.7 GHz <6.0 GHz	dB	29 24	32 26	—
Input / Output Return Loss ( $R_L$ )	$V_R = 10 \text{ V}$ 2.7 GHz <6.0 GHz	dB	18 13	22 15	—
Minority Carrier Lifetime ( $T_L$ )	$I_F = 10 \text{ mA}$ , $I_R = 6 \text{ mA}$ , @ 50%	ns	—	600	—

\* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

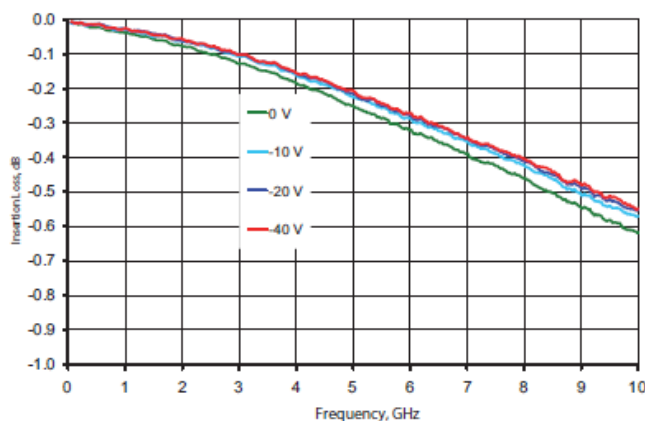
## Absolute Maximum Ratings

Parameter	Absolute Maximum
Breakdown Voltage	500 V
Forward Current	500 mA
Thermal Resistance	10°C/W
Junction Temperature	+175°C
Storage Temperature	-65°C to +150°C
Assembly Temperature	+260°C Per JEDEC STD-J-20C

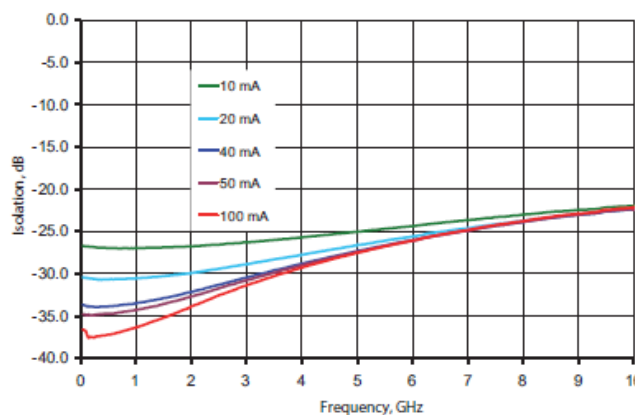
**Junction Temperature vs. Power  
Mounted on Heatsink, +25°C, 1.3 GHz**



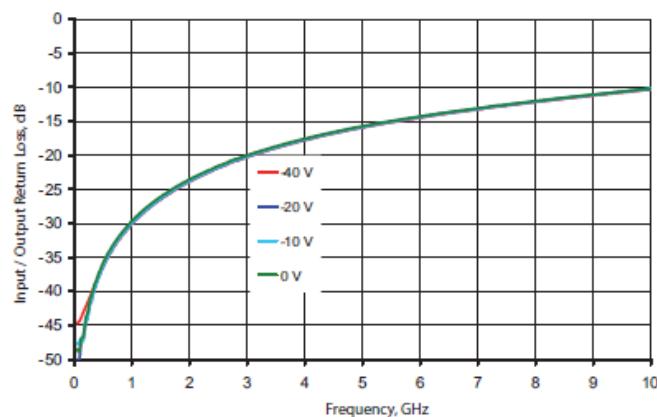
**Insertion Loss**



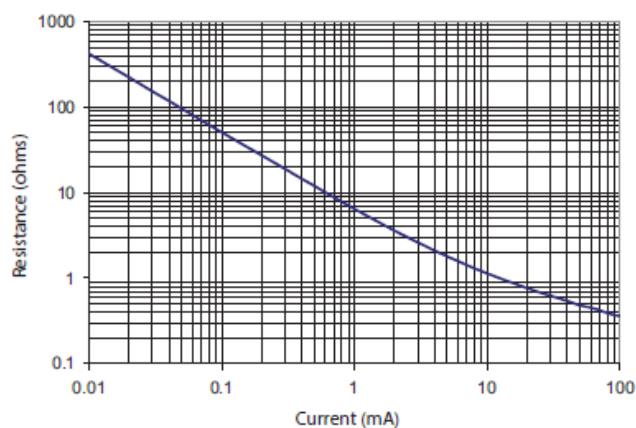
**Isolation**



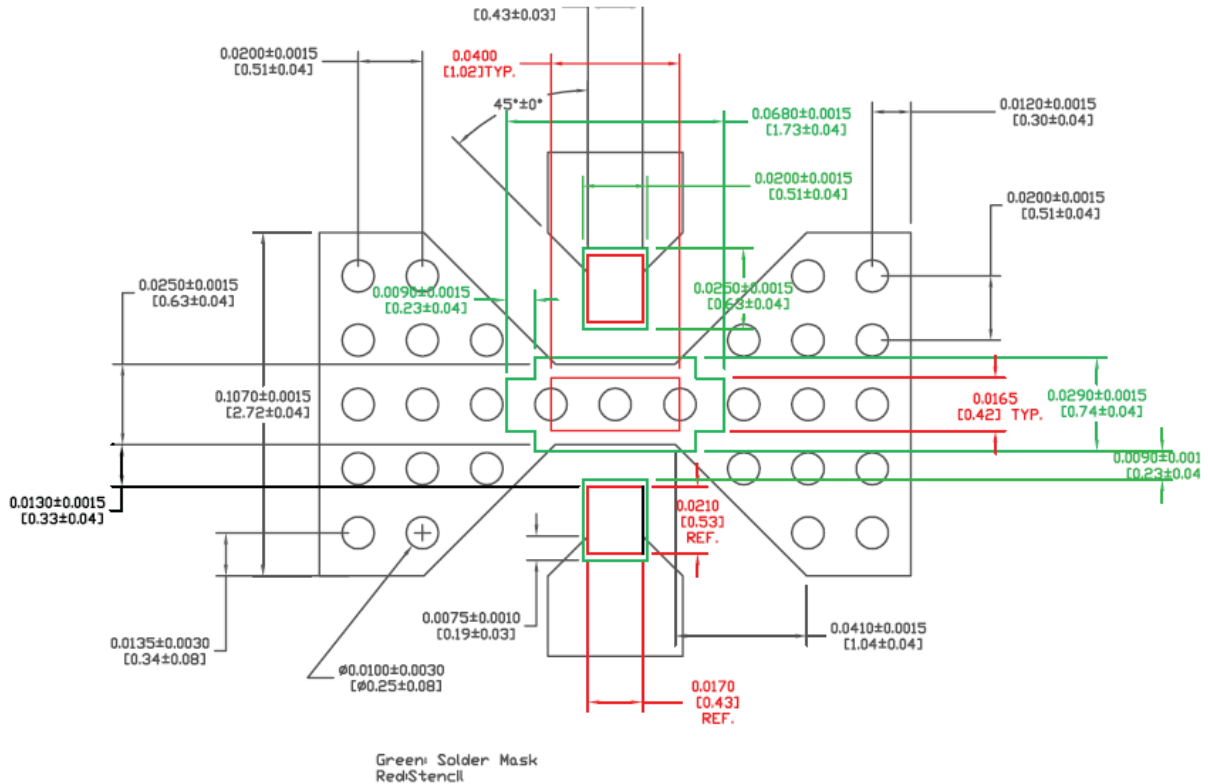
**Input Return Loss**



**Series Resistance vs. Bias, 500 MHz**



### Printed Circuit Board Layout

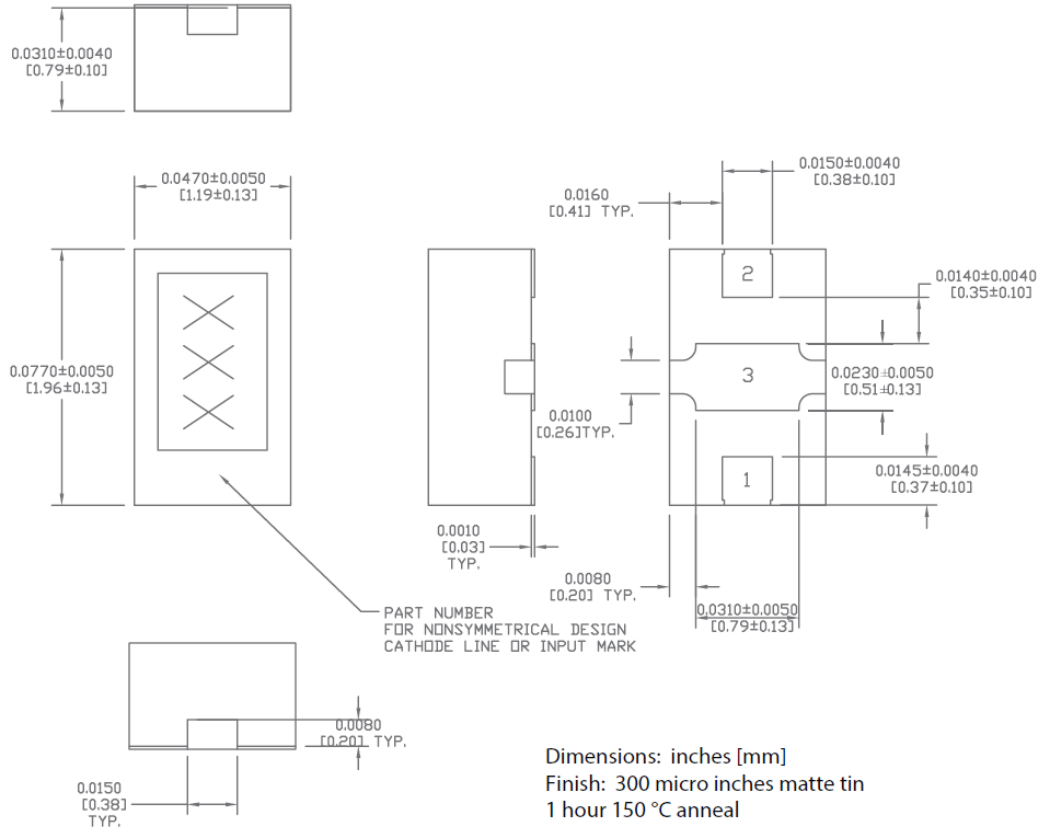


NOTE: If possible, use copper filled vias underneath pin 3 for better thermals; otherwise, use vias that are plated through, filled and plated over.

Solder mask should provide a 60 um clearance between copper pad and soldermask. Rounded pkg pads should have matching rounded solder mask openings.

Use circles or squares for the thermal land stencil such that only get 50% to 80% solder paste coverage.

## Outline (2012)



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