The RF Line NPN Silicon Power Transistor
100W(PEP), 30MHz, 28V

Designed primarily for application as a high-power linear amplifier from 2.0
 to 30 MHz.

- Specified 12.5 V, 30 MHz characteristics —
  Output power = 100 W (PEP)
  Minimum gain = 10 dB
  Efficiency = 40%
- Intermodulation distortion @ 100 W (PEP) — IMD = –30 dB (min.)
- 100% tested for load mismatch at all phase angles with 30:1 VSWR

MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collector-Emitter Voltage</td>
<td>V_{CEO}</td>
<td>20</td>
<td>Vdc</td>
</tr>
<tr>
<td>Collector-Base Voltage</td>
<td>V_{CBO}</td>
<td>45</td>
<td>Vdc</td>
</tr>
<tr>
<td>Emitter-Base Voltage</td>
<td>V_{EBO}</td>
<td>3.0</td>
<td>Vdc</td>
</tr>
<tr>
<td>Collector Current — Continuous</td>
<td>I_C</td>
<td>20</td>
<td>Adc</td>
</tr>
<tr>
<td>Withstand Current — 10 s</td>
<td></td>
<td>30</td>
<td>Adc</td>
</tr>
<tr>
<td>Total Device Dissipation @ T_C = 26°C</td>
<td>P_D</td>
<td>290</td>
<td>Watts</td>
</tr>
<tr>
<td>Derate above 25°C</td>
<td></td>
<td>1.66</td>
<td>W/°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td></td>
<td>–65 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

THERMAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Resistance, Junction to Case</td>
<td>R_{JVC}</td>
<td>0.5</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)</td>
<td>V_{BRICEO}</td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>Vdc</td>
</tr>
<tr>
<td>Collector-Emitter Breakdown Voltage (I_C = 200 mAdc, V_{BE} = 0)</td>
<td>V_{BRICES}</td>
<td>45</td>
<td>—</td>
<td>—</td>
<td>Vdc</td>
</tr>
<tr>
<td>Collector-Base Breakdown Voltage (I_C = 200 mAdc, I_E = 0)</td>
<td>V_{BRICBO}</td>
<td>45</td>
<td>—</td>
<td>—</td>
<td>Vdc</td>
</tr>
<tr>
<td>Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)</td>
<td>V_{BRIEBO}</td>
<td>3.0</td>
<td>—</td>
<td>—</td>
<td>Vdc</td>
</tr>
<tr>
<td>Collector Cutoff Current (V_{CE} = 16 Vdc, V_{BE} = 0, T_C = 25°C)</td>
<td>I_{CES}</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>mAdc</td>
</tr>
</tbody>
</table>

(continued)
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ELECTRICAL CHARACTERISTICS – continued (T_C = 25°C unless otherwise noted.)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Current Gain</td>
<td>hFE</td>
<td>10</td>
<td>70</td>
<td>—</td>
<td>—</td>
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</tbody>
</table>

DYNAMIC CHARACTERISTICS

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Capacitance (V_CE = 12.5 Vdc, I_E = 0, f = 1.0 MHz)</td>
<td>C_OB</td>
<td>—</td>
<td>560</td>
<td>600</td>
<td>pF</td>
</tr>
</tbody>
</table>

FUNCTIONAL TESTS

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Common–Emitter Amplifier Power Gain (V_CC = 12.5 Vdc, P_out = 100 W, I_C(max) = 10 Adc, I_CQ = 150 mA, f = 30, 30.001 MHz)</td>
<td>G_FE</td>
<td>10</td>
<td>12</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Collector Efficiency (V_CC = 12.5 Vdc, P_out = 100 W, I_C(max) = 10 Adc, I_CQ = 150 mA, f = 30, 30.001 MHz)</td>
<td>η</td>
<td>40</td>
<td>—</td>
<td>—</td>
<td>%</td>
</tr>
<tr>
<td>Intermodulation Distortion (I) (V_CE = 12.5 Vdc, P_out = 100 W, I_C = 10 Adc, I_CQ = 150 mA, f = 30, 30.001 MHz)</td>
<td>IMD</td>
<td>—</td>
<td>−33</td>
<td>−30</td>
<td>dB</td>
</tr>
</tbody>
</table>

NOTE:
1. To proposed EIA method of measurement. Reference peak envelope power.

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Figure 1. 30 MHz Test Circuit Schematic
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Figure 2. Output Power versus Input Power

Figure 3. Output Power versus Supply Voltage

Figure 4. Power Gain versus Frequency

Figure 5. Intermodulation Distortion versus Output Power

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Figure 6. DC Safe Operating Area

Figure 7. Series Equivalent Impedance
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Figure 8. Output Capacitance versus Frequency

Figure 9. Output Resistance versus Frequency

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