MRF175LU

The RF MOSFET Line
100W, 400MHz, 28V

Designed for broadband commercial and military applications using single ended circuits at frequencies to 400 MHz. The high power, high gain and broadband performance of each device makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

N-Channel enhancement mode
- Guaranteed performance
- MRF175LU @ 28 V, 400 MHz ("U" Suffix)
  Output power — 100 W
  Power gain — 10 dB typ
  Efficiency — 55% typ
- 100% ruggedness tested at rated output power
- Low thermal resistance
- Low Crss — 20 pF Typ @ Vds = 28 V

MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-Source Voltage</td>
<td>V_DSS</td>
<td>65</td>
<td>Vdc</td>
</tr>
<tr>
<td>Gate-Source Voltage</td>
<td>V_GS</td>
<td>≥40</td>
<td>Vdc</td>
</tr>
<tr>
<td>Drain Current — Continuous</td>
<td>I_D</td>
<td>13</td>
<td>Adc</td>
</tr>
<tr>
<td>Total Device Dissipation @ T_C = 25°C</td>
<td>P_D</td>
<td>270</td>
<td>Watts</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.54</td>
<td>W/C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>T_S</td>
<td>-65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td>T_J</td>
<td>200</td>
<td>°C</td>
</tr>
</tbody>
</table>

THERMAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Resistance, Junction to Case</td>
<td>R_JUC</td>
<td>0.65</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

OFF CHARACTERISTICS

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-Source Breakdown Voltage (V_GS = 0, I_D = 50 mA)</td>
<td>V_DBDSS</td>
<td>65</td>
<td>—</td>
<td>—</td>
<td>Vdc</td>
</tr>
<tr>
<td>Zero Gate Voltage Drain Current (V_DS = 28 V, V_GS = 0)</td>
<td>I_DSS</td>
<td>—</td>
<td>—</td>
<td>2.5</td>
<td>mA</td>
</tr>
<tr>
<td>Gate–Body Leakage Current (V_GS = 20 V, V_DS = 0)</td>
<td>I_GSS</td>
<td>—</td>
<td>—</td>
<td>1.0</td>
<td>μA</td>
</tr>
</tbody>
</table>

(continued)
### ELECTRICAL CHARACTERISTICS — continued  (T_C = 25°C unless otherwise noted)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ON CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)</td>
<td>V_{GS(min)}</td>
<td>1.0</td>
<td>3.0</td>
<td>6.0</td>
<td>Vdc</td>
</tr>
<tr>
<td>Drain-Source On-Voltage (V_{GS} = 10 V, I_D = 5.0 A)</td>
<td>V_{DS(on)}</td>
<td>0.1</td>
<td>0.9</td>
<td>1.5</td>
<td>Vdc</td>
</tr>
<tr>
<td>Forward Transconductance (V_{DS} = 10 V, I_D = 2.5 A)</td>
<td>g_m</td>
<td>2.0</td>
<td>3.0</td>
<td>—</td>
<td>mhos</td>
</tr>
</tbody>
</table>

### DYNAMIC CHARACTERISTICS

- **Input Capacitance** (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)  
  \( C_{iss} \)
  - 180 pF

- **Output Capacitance** (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)  
  \( C_{oss} \)
  - 200 pF

- **Reverse Transfer Capacitance** (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)  
  \( C_{tss} \)
  - 20 pF

### FUNCTIONAL CHARACTERISTICS — MRF175LU (Figure 2)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
</table>
| Common Source Power Gain  
  (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 400 MHz, I_{DQ} = 100 mA) | G_{dc} | 8.0 | 10  | —   | dB   |
| Drain Efficiency  
  (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 400 MHz, I_{DQ} = 100 mA) | \( \eta \) | 50  | 55  | —   | %    |
| Electrical Ruggedness  
  (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 400 MHz, I_{DQ} = 100 mA,  
  VSWR 30:1 at all Phase Angles) | \( \psi \) | No Degradation in Output Power |

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**Figure 2. 400 MHz Test Circuit**

- C1, C8 — 270 pF ATC Chip Cap
- C2, C4, C5, C7 — 1.0–20 pF Trimmer Cap
- C3 — 15 pF Mini Unilco Cap
- C6 — 33 pF Mini Unilco Cap
- C9, C12 — 0.1 µF Ceramic Cap
- C11, C14 — 680 pF Feed Thru Cap
- C13 — 50 µF Tantalum Cap
- L1 — Hairpin Inductor #18 Wire
- L2 — 12 Turns #18 Wire 0.450” ID
- L3 — Ferroxcube VK200 20/4B
- R1 — 10 k 1/4 W Resistor
- R2 — 1 k 1/4 W Resistor
- R3 — 1.5 k 1/4 W Resistor
- Z1 — Microstrip Line 0.350” x 0.250”
- Z2 — Microstrip Line 1” x 0.250”
- Z3 — Microstrip Line 0.550” x 0.250”
- Board Material — 0.062” Teflon — fiberglass, \( r_t = 2.56 \), 1 oz. copper clad both sides
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Rev. V1

TYPICAL CHARACTERISTICS

Figure 3. Common Source Unity Current Gain Frequency versus Drain Current

Figure 4. DC Safe Operating Area

Figure 5. Drain Current versus Gate Voltage (Transfer Characteristics)

Figure 6. Gate–Source Voltage versus Case Temperature

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Figure 7. Capacitance versus Drain–Source Voltage

Figure 9. Output Power versus Supply Voltage

Figure 10. Power Gain versus Frequency

Figure 11. Output Power versus Input Power

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INPUT AND OUTPUT IMPEDANCE

Figure 12.

<table>
<thead>
<tr>
<th>f (MHz)</th>
<th>( Z_0 ) Ohms</th>
<th>( Z_{0L}^* ) Ohms</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>2.80 - j4.00</td>
<td>3.65 - j1.30</td>
</tr>
<tr>
<td>100</td>
<td>1.40 - j2.80</td>
<td>2.90 - j1.50</td>
</tr>
<tr>
<td>150</td>
<td>1.10 - j1.90</td>
<td>2.10 - j1.40</td>
</tr>
<tr>
<td>175</td>
<td>1.00 - j1.25</td>
<td>1.80 - j1.20</td>
</tr>
<tr>
<td>225</td>
<td>0.95 - j0.65</td>
<td>1.50 - j0.80</td>
</tr>
<tr>
<td>300</td>
<td>0.95 + j0.20</td>
<td>1.35 - j0.30</td>
</tr>
<tr>
<td>400</td>
<td>1.05 + j1.15</td>
<td>1.45 + j0.55</td>
</tr>
</tbody>
</table>

\( Z_{0L}^* \) = CONJUGATE OF THE OPTIMUM LOAD IMPEDANCE INTO WHICH THE DEVICE OUTPUT OPERATES AT A GIVEN OUTPUT POWER, VOLTAGE AND FREQUENCY.
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RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.

\[
\begin{align*}
C_{gs} & = C_{gd} + C_{gs} \\
C_{oss} & = C_{gs} + C_{ds} \\
C_{iss} & = C_{ds} \\
C_{rss} & = C_{ds}
\end{align*}
\]

The C_{iss} given in the electrical characteristics table was measured using method 2 above. It should be noted that: C_{iss}, C_{oss}, C_{rss} are measured at zero drain current and are provided for general information about the device. They are not RF design parameters and no attempt should be made to use them as such.

LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain, data presented in Figure 3 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to fr for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, V_{DSS(on)}, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, V_{DSS(on)} has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^10 ohms — resulting in a leakage current of a few nanoamperes. Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, V_{GS(th)}.

Gate Voltage Rating — Never exceed the gate voltage rating (or any of the maximum ratings on the front page). Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of this device are essentially capacitors. Circuits that leave the gate open–circuit or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate–to–source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

HANDLING CONSIDERATIONS

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with grounded equipment.

DESIGN CONSIDERATIONS

The MRF175L is a RF power N–channel enhancement mode field–effect transistor (FETs) designed for HF, VHF andUHF power amplifier applications. M/A-COM RF MOSFETs feature a vertical structure with a planar design. M/A-
COM Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal.

**DC BIAS**

The MRF175L is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I\text{DQ}) is not critical for many applications. The MRF175L was characterized at I\text{DQ} = 100 mA, each side, which is the suggested minimum value of I\text{DQ}. For special applications such as linear amplification, I\text{DQ} may have to be selected to optimize the critical parameters. The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias system.

**GAIN CONTROL**

Power output of the MRF175L may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.