MRF174

The RF MOSFET Line
125W, 200MHz

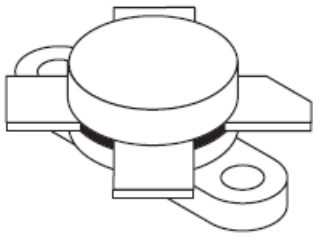
Rev. V1

Designed primarily for wideband large–signal output and driver stages up to 200 MHz frequency range.

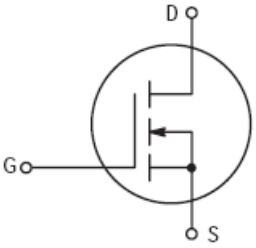
N–Channel enhancement mode MOSFET

- Guaranteed performance at 150 MHz, 28 Vdc
  Output power = 125 W
  Minimum gain = 9.0 dB
- Efficiency = 50% (min.)
- Excellent thermal stability, ideally suited for Class A operation
- Facilitates manual gain control, ALC and modulation techniques
- 100% tested for load mismatch at all phase angles with 30:1 VSWR
- Low noise figure — 3.0 dB typ. at 2.0 A, 150 MHz

Product Image



CASE 211–11, STYLE 2



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	13	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

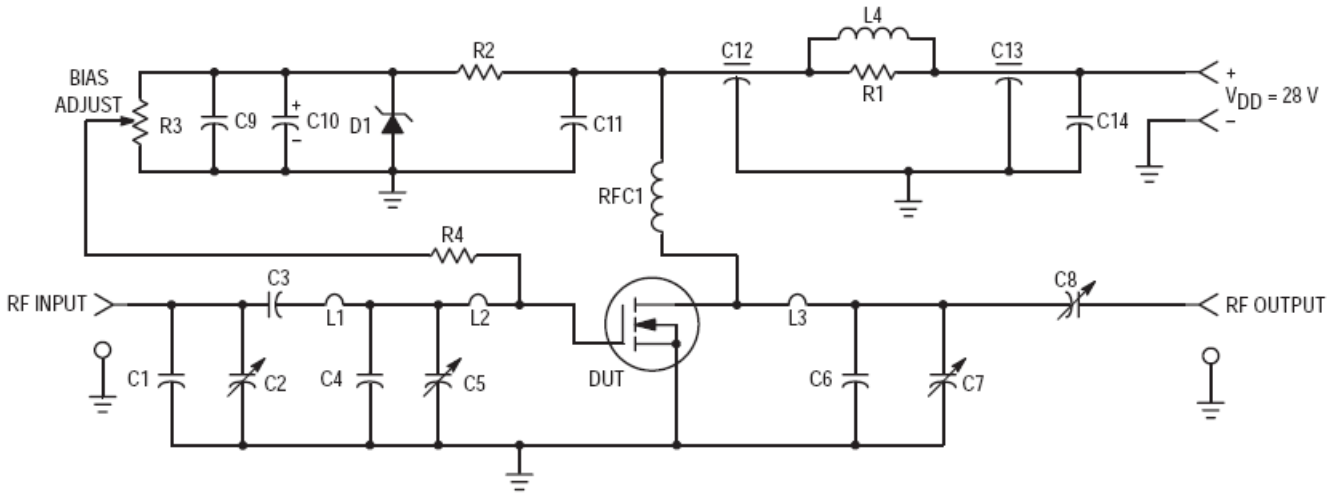
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 50 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	10	mAdc
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	µAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 3.0 A)	gfs	1.75	2.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	175	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	190	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	40	—	pF
FUNCTIONAL CHARACTERISTICS (Figure 1)					
Noise Figure (V_{DD} = 28 Vdc, I_D = 2.0 A, f = 150 MHz)	NF	—	3.0	—	dB
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 125 W, f = 150 MHz, I_{DQ} = 100 mA)	G_{ps}	9.0	11.8	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 125 W, f = 150 MHz, I_{DQ} = 100 mA)	η	50	60	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 125 W, f = 150 MHz, I_{DQ} = 100 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			



C1 — 15 pF Unelco
C2 — Arco 462, 5.0–80 pF
C3 — 100 pF Unelco
C4 — 25 pF Unelco
C6 — 40 pF Unelco
C7 — Arco 461, 2.7–30 pF
C5, C8 — Arco 463, 9.0–180 pF
C9, C11, C14 — 0.1 µF Erie Redcap
C10 — 50 µF, 50 V
C12, C13 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener

L1 — #16 AWG, 1–1/4 Turns, 0.213″ ID
L2 — #16 AWG, Hairpin 0.25″ / 0.062″
L3 — #14 AWG, Hairpin 0.47″ / 0.2″
L4 — 10 Turns #16 AWG Enameled Wire on R1
RFC1 — 18 Turns #16 AWG Enameled Wire, 0.3″ ID
R1 — 10 Ω, 2.0 W
R2 — 1.8 kΩ, 1/2 W
R3 — 10 kΩ, 10 Turn Bourns
R4 — 10 kΩ, 1/4 W

Figure 1. 150 MHz Test Circuit

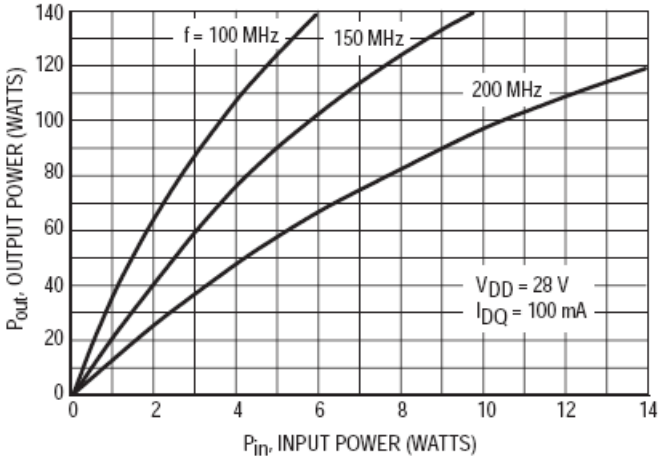


Figure 2. Output Power versus Input Power

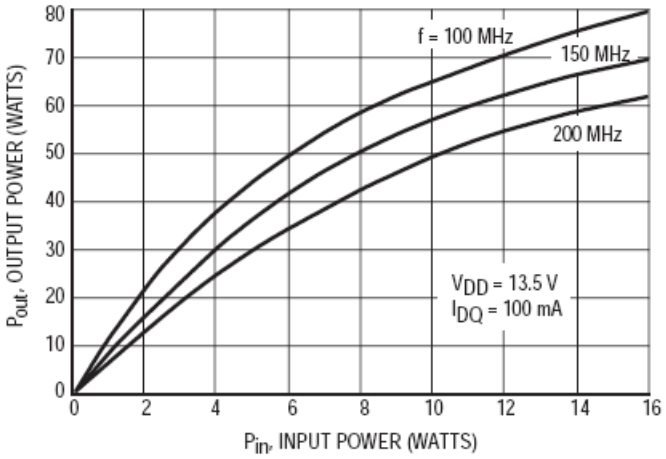


Figure 3. Output Power versus Input Power

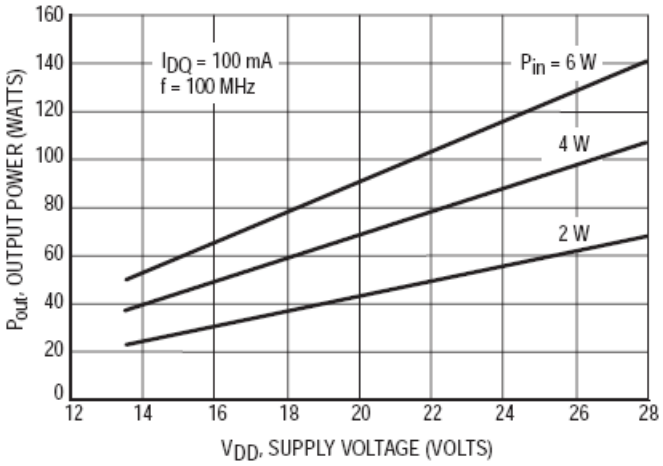


Figure 4. Output Power versus Supply Voltage

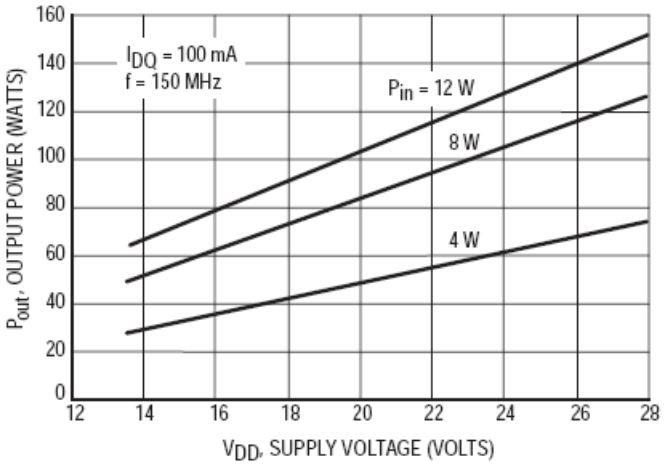


Figure 5. Output Power versus Supply Voltage

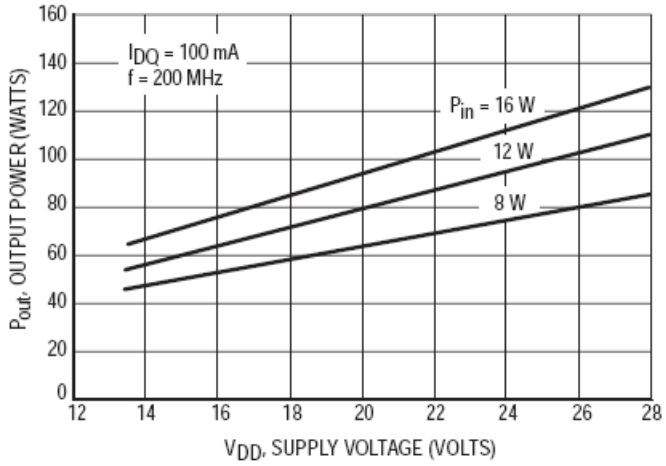


Figure 6. Output Power versus Supply Voltage

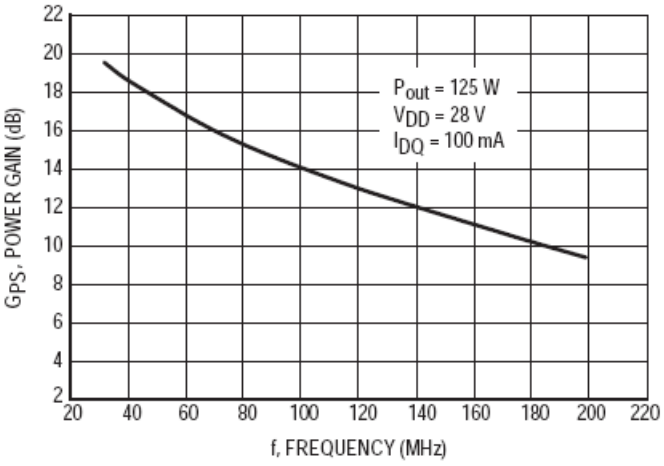


Figure 7. Power Gain versus Frequency

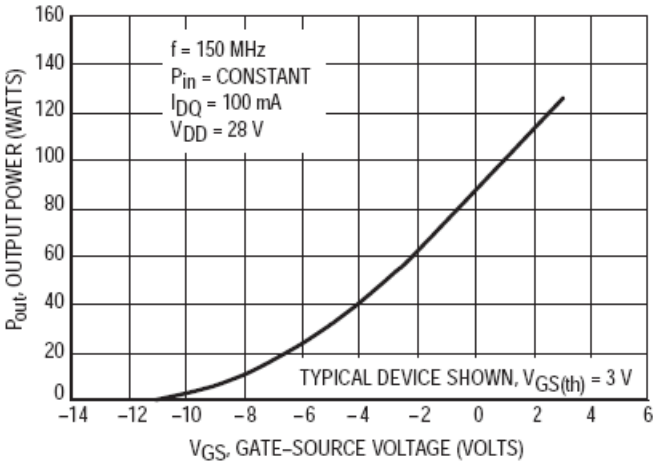


Figure 8. Output Power versus Gate Voltage

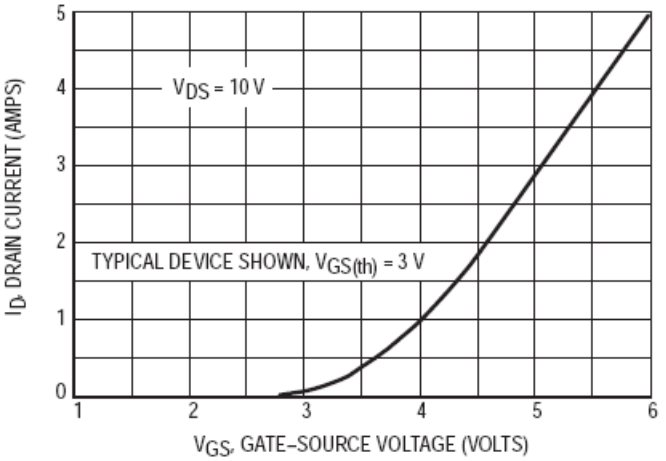


Figure 9. Drain Current versus Gate Voltage (Transfer Characteristics)

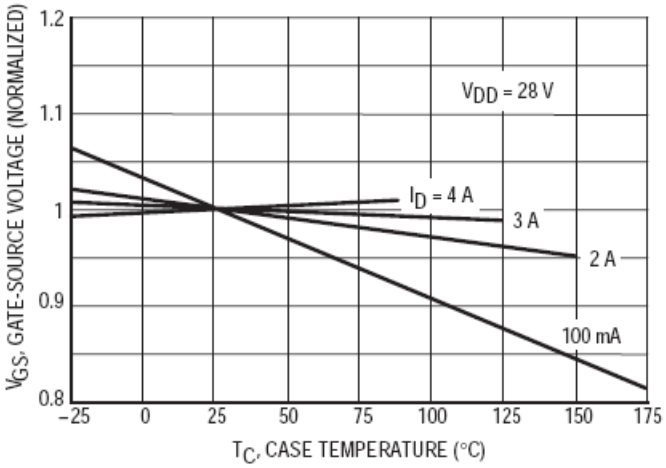


Figure 10. Gate–Source Voltage versus

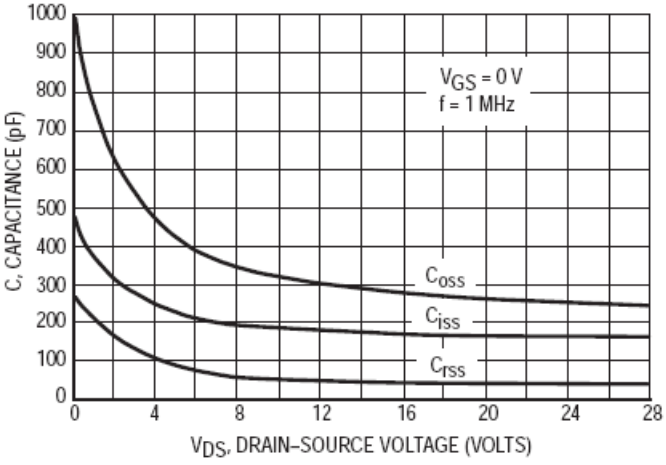


Figure 11. Capacitance versus Drain Voltage

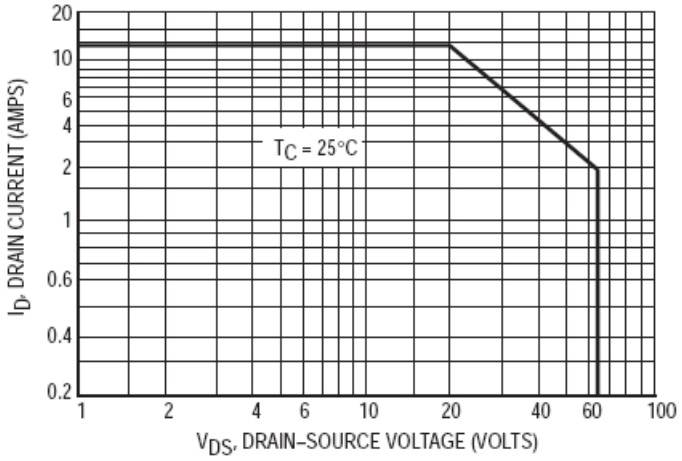


Figure 12. DC Safe Operating Area

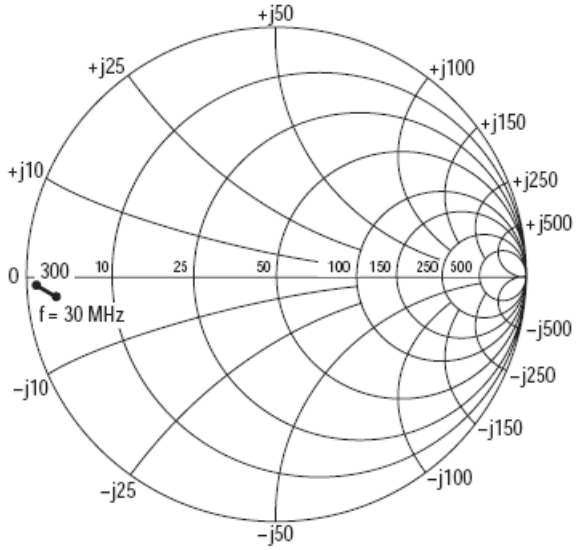


Figure 13. S_{11}, Input Reflection Coefficient versus Frequency
V_{DS} = 28 V, I_D = 3.0 A

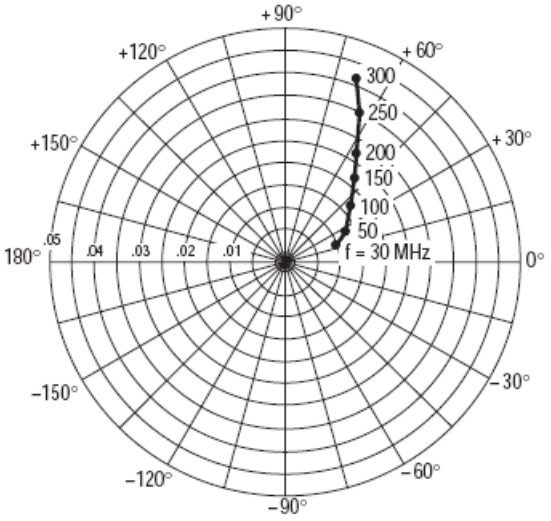


Figure 14. S_{12}, Reverse Transmission Coefficient versus Frequency
V_{DS} = 28 V, I_D = 3.0 A

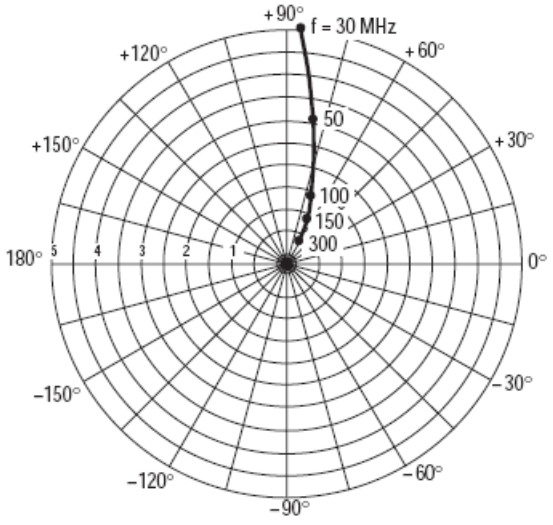


Figure 15. S_{21}, Forward Transmission Coefficient versus Frequency
V_{DS} = 28 V, I_D = 3.0 A

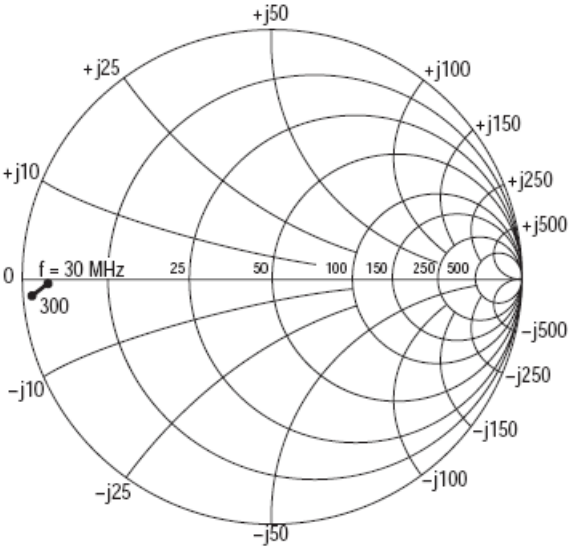
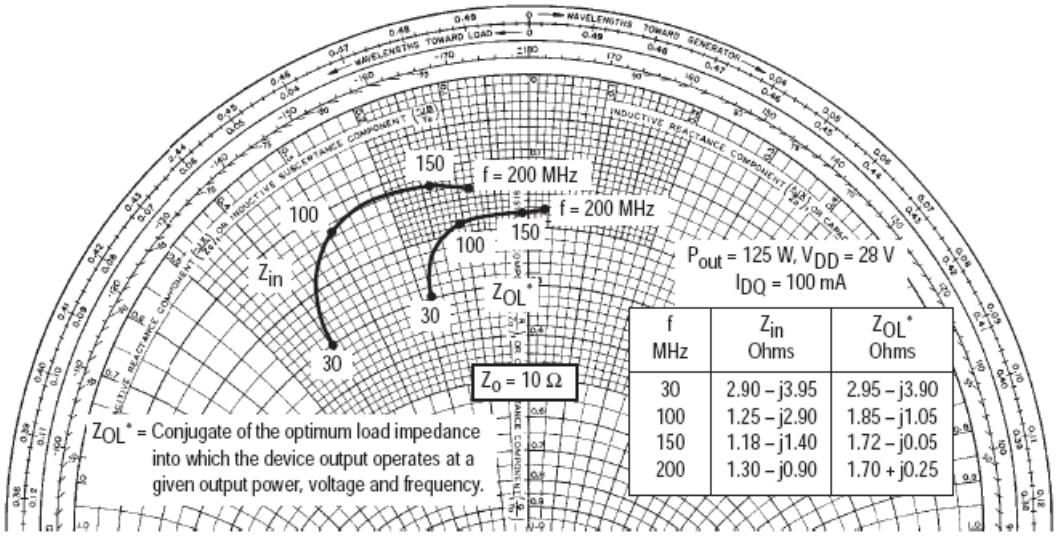


Figure 16. S_{22}, Output Reflection Coefficient versus Frequency
V_{DS} = 28 V, I_D = 3.0 A



f MHz	Z_{in} Ohms	Z_{OL}^* Ohms
30	2.90 – j3.95	2.95 – j3.90
100	1.25 – j2.90	1.85 – j1.05
150	1.18 – j1.40	1.72 – j0.05
200	1.30 – j0.90	1.70 + j0.25

Figure 17. Series Equivalent Input/Output Impedance, Z_{in}, Z_{OL}^*

DESIGN CONSIDERATIONS

The MRF174 is a RF MOSFET power N–channel enhancement mode field–effect transistor (FET) designed for UHF power amplifier applications. M/A-COM RF MOSFETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V–groove power FETs.

M/A-COM Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF174 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (IDQ) is not critical for many applications. The MRF174 was characterized at IDQ = 100 mA, which is the suggested minimum value of IDQ. For special applications such as linear amplification, IDQ may have to be selected to optimize the critical parameters.

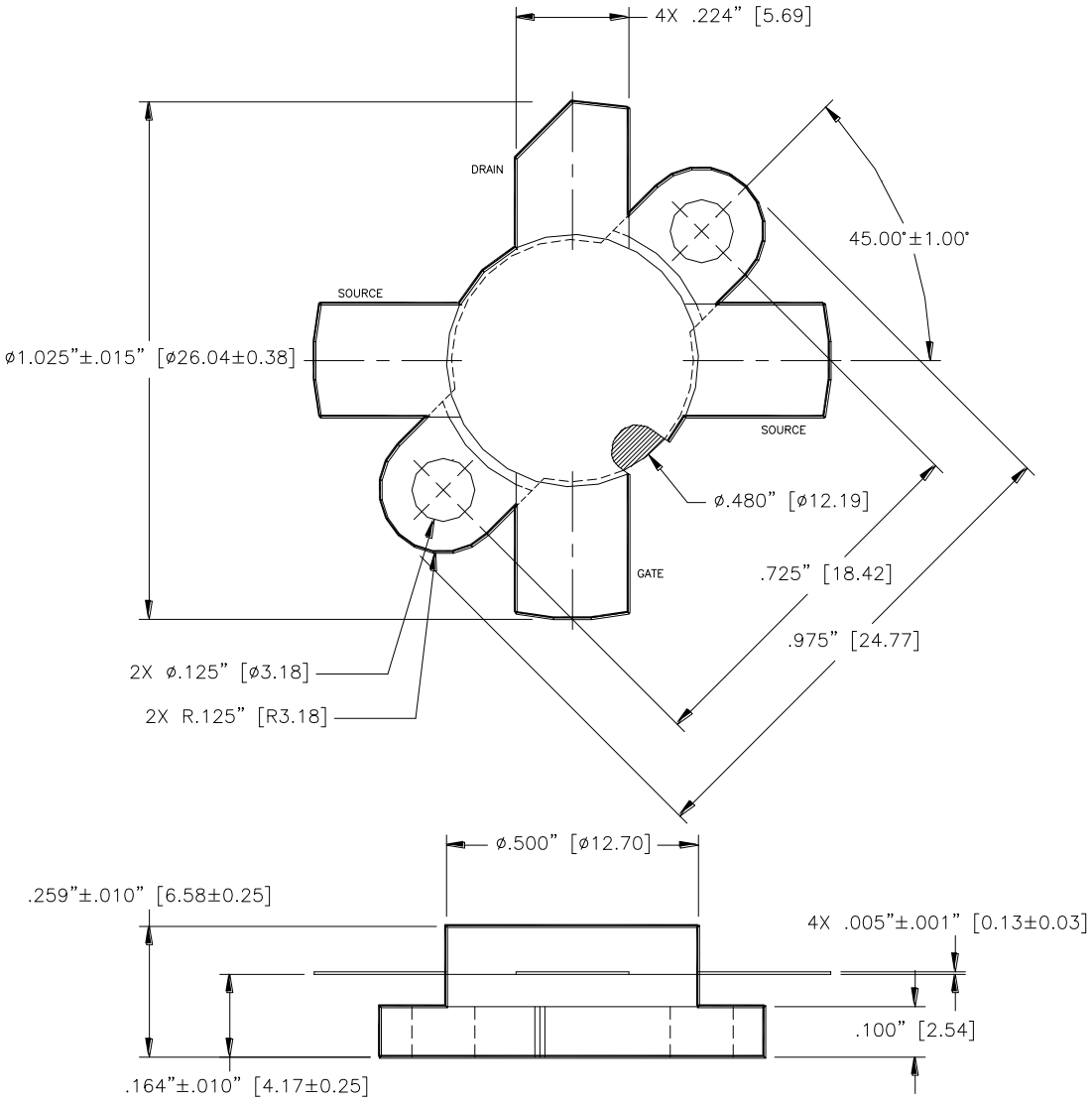
The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF174 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.
(see Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar VHF transistors are suitable for MRF174. See M/A-COM Application Note AN721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of RF MOSFETs helps ease the task of broadband network design. Both small–signal scattering parameters and large–signal impedances are provided. While the s–parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF MOS power FETs.



Unless otherwise noted, tolerances are inches ±.005" [millimeters ±0.13mm]