Designed for power amplifier applications in industrial, commercial and amateur radio equipment to 175MHz.

- Superior high order IMD
  - IMD(d3) (30W PEP): –35 dB (Typ.)
  - IMD(d11) (30W PEP): –60 dB (Typ.)

- Specified 50V, 30MHz characteristics:
  - Output power: 30W
  - Gain: 18dB (Typ.)
  - Efficiency: 40% (Typ.)

- 100% tested for load mismatch at all phase angles with 30:1 VSWR
- Lower reverse transfer capacitance (3.0 pF typ.)

## MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain–Source Voltage</td>
<td>V_DSS</td>
<td>120</td>
<td>Vdc</td>
</tr>
<tr>
<td>Drain–Gate Voltage</td>
<td>V_DGO</td>
<td>120</td>
<td>Vdc</td>
</tr>
<tr>
<td>Gate–Source Voltage</td>
<td>V_GS</td>
<td>±40</td>
<td>Vdc</td>
</tr>
<tr>
<td>Drain Current — Continuous</td>
<td>I_D</td>
<td>6.0</td>
<td>Adc</td>
</tr>
<tr>
<td>Total Device Dissipation @ T_C = 25°C</td>
<td>P_D</td>
<td>115</td>
<td>Watts</td>
</tr>
<tr>
<td>Derate above 25°C</td>
<td></td>
<td>0.86</td>
<td>W/°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>T_stg</td>
<td>–65 to +160</td>
<td>°C</td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td>T_J</td>
<td>200</td>
<td>°C</td>
</tr>
</tbody>
</table>

## THERMAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Resistance, Junction to Case</td>
<td>R_WJC</td>
<td>1.52</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

NOTE – CAUTION – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.
**MRF148A**

**Linear RF Power FET**
**30W, to 175MHz, 50V**

**Revised: V1**

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### ELECTRICAL CHARACTERISTICS  
(T<sub>C</sub> = 25°C unless otherwise noted.)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>OFF CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Drain–Source Breakdown Voltage (V&lt;sub&gt;GS&lt;/sub&gt; = 0, I&lt;sub&gt;D&lt;/sub&gt; = 10 mA)</td>
<td>V&lt;sub&gt;(BR)&lt;/sub&gt;DSS</td>
<td>125</td>
<td>—</td>
<td>—</td>
<td>V&lt;sub&gt;dc&lt;/sub&gt;</td>
</tr>
<tr>
<td>Zero Gate Voltage Drain Current (V&lt;sub&gt;GS&lt;/sub&gt; = 50 V, V&lt;sub&gt;DS&lt;/sub&gt; = 0)</td>
<td>I&lt;sub&gt;DSS&lt;/sub&gt;</td>
<td>—</td>
<td>—</td>
<td>1.0</td>
<td>mA&lt;sub&gt;dc&lt;/sub&gt;</td>
</tr>
<tr>
<td>Gate–Body Leakage Current (V&lt;sub&gt;GS&lt;/sub&gt; = 20 V, V&lt;sub&gt;DS&lt;/sub&gt; = 0)</td>
<td>I&lt;sub&gt;GSS&lt;/sub&gt;</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>nA&lt;sub&gt;dc&lt;/sub&gt;</td>
</tr>
<tr>
<td><strong>ON CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate Threshold Voltage (V&lt;sub&gt;DS&lt;/sub&gt; = 10 V, I&lt;sub&gt;D&lt;/sub&gt; = 10 mA)</td>
<td>V&lt;sub&gt;G&lt;/sub&gt;(&lt;i&gt;θ&lt;/i&gt;)</td>
<td>1.0</td>
<td>2.5</td>
<td>5.0</td>
<td>V&lt;sub&gt;dc&lt;/sub&gt;</td>
</tr>
<tr>
<td>Drain–Source On–Voltage (V&lt;sub&gt;GS&lt;/sub&gt; = 10 V, I&lt;sub&gt;D&lt;/sub&gt; = 2.5 A)</td>
<td>V&lt;sub&gt;DS(on)&lt;/sub&gt;</td>
<td>1.0</td>
<td>3.0</td>
<td>5.0</td>
<td>V&lt;sub&gt;dc&lt;/sub&gt;</td>
</tr>
<tr>
<td>Forward Transconductance (V&lt;sub&gt;DS&lt;/sub&gt; = 10 V, I&lt;sub&gt;D&lt;/sub&gt; = 2.5 A)</td>
<td>g&lt;sub&gt;fs&lt;/sub&gt;</td>
<td>0.8</td>
<td>1.2</td>
<td>—</td>
<td>mhos</td>
</tr>
</tbody>
</table>

### DYNAMIC CHARACTERISTICS

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Capacitance (V&lt;sub&gt;GS&lt;/sub&gt; = 50 V, V&lt;sub&gt;DS&lt;/sub&gt; = 0, f = 1.0 MHz)</td>
<td>C&lt;sub&gt;iss&lt;/sub&gt;</td>
<td>—</td>
<td>62</td>
<td>—</td>
<td>pF</td>
</tr>
<tr>
<td>Output Capacitance (V&lt;sub&gt;DS&lt;/sub&gt; = 50 V, V&lt;sub&gt;GS&lt;/sub&gt; = 0, f = 1.0 MHz)</td>
<td>C&lt;sub&gt;oss&lt;/sub&gt;</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>pF</td>
</tr>
<tr>
<td>Reverse Transfer Capacitance (V&lt;sub&gt;DS&lt;/sub&gt; = 50 V, V&lt;sub&gt;GS&lt;/sub&gt; = 0, f = 1.0 MHz)</td>
<td>C&lt;sub&gt;rss&lt;/sub&gt;</td>
<td>—</td>
<td>3.0</td>
<td>—</td>
<td>pF</td>
</tr>
</tbody>
</table>

### FUNCTIONAL TESTS (SSB)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
</table>
| Common Source Amplifier Power Gain  
  (V<sub>DP</sub> = 50 V, P<sub>out</sub> = 30 W (PEP), I<sub>DQ</sub> = 100 mA)  
  (30 MHz) | G<sub>ps</sub> | — | 18 | — | dB |
| Drain Efficiency  
  (V<sub>DP</sub> = 50 V, f = 30 MHz, I<sub>DQ</sub> = 100 mA)  
  (30 W PEP) | η | — | 40 | — | % |
| Intermodulation Distortion  
  (V<sub>DP</sub> = 50 V, P<sub>out</sub> = 30 W (PEP),  
  f = 30, 30.001 MHz, I<sub>DQ</sub> = 100 mA)  
  (30 W CW) | IMD<sub>(d3)</sub> | — | −35 | — | dB |
| IMD<sub>(d11)</sub> | — | −60 | — | dB |
| Load Mismatch  
  (V<sub>DP</sub> = 50 V, P<sub>out</sub> = 30 W (PEP), f = 30, 30.001 MHz,  
  I<sub>DQ</sub> = 100 mA, VSWR 3:1 at all Phase Angles) | Ψ | No Degradation in Output Power |

### CLASS A PERFORMANCE

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
</table>
| Intermodulation Distortion (1) and Power Gain  
  (V<sub>DP</sub> = 50 V, P<sub>out</sub> = 10 W (PEP), f<sub>1</sub> = 30 MHz,  
  I<sub>DQ</sub> = 100 mA) | G<sub>P</sub> | 20 | — | — | dB |
| IMD<sub>(d3)</sub> | — | 50 | — | dB |
| IMD<sub>(d13)</sub> | — | 70 | — | dB |

**NOTE:**
Linear RF Power FET
30W, to 175MHz, 50V

C1, C2, C3, C4, C5, C6 — 0.1 μF Ceramic Chip or Equivalent
C7 — 10 μF, 100 V Electrolytic
C8 — 100 pF Dipped Mica
L1 — VK200 20/4dB Ferrite Choke or Equivalent (3.0 μH)
L2 — Ferrite Bead(s), 2.0 μH
R1, R2 — 200 Ω, 1/2 W Carbon
R3 — 4.7 Ω, 1/2 W Carbon
R4 — 470 Ω, 1.0 W Carbon
T1 — 4:1 Impedance Transformer
T2 — 1:2 Impedance Transformer

Figure 1. 2.0 to 50 MHz Broadband Test Circuit

Figure 2. Power Gain versus Frequency

Figure 3. Output Power versus Input Power
MRF148A

Linear RF Power FET
30W, to 175MHz, 50V

Rev. V1

Figure 4. IMD versus P_out

Figure 5. Common Source Unity Gain Frequency versus Drain Current

Figure 6. 150 MHz Test Circuit

C1 — 91 pF Unelco Type MCM 01/010
C2, C4 — 0.1 µF Elna Red Cap
C3 — Allen Bradley 680 pF Feed Thru
C5 — 1.0 µF, 50 Vdc Electrolytic
C6 — 15 pF Unelco Type J101
C7 — 24 pF Unelco Type MCM 01/010
L1 — 2 Turns #18 AWG, 5/16” ID
L2 — 4 Turns #18 AWG, 5/16” ID
R1 — 1.0 Ohm, 1/4 W Carbon
R2 — 2000 Ohm, 1/4 W Carbon
RFC1 — VK200 21/4B
T1 — 4:1 Transformer, 1.75” Subminiature Coaxial Cable

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Linear RF Power FET
30W, to 175MHz, 50V

Figure 7. Gate Voltage versus Drain Current

Figure 8. DC Safe Operating Area (SOA)

Figure 9. Impedance Coordinates — 50 Ohm Characteristic Impedance
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal-oxide gate structure determines the capacitances from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during the fabrication of the RF MOSFET results in a junction capacitance from drain-to-source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower.

However, neither method represents the actual operating conditions in RF applications.

Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, V_{DS(on)}, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, V_{DS(on)} has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^6 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage, V_{GS(th)}.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open—circuited or floating should be avoided. These conditions can result in turn—on of the devices due to voltage build—up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate—to—source. If gate protection is required, an external zener diode is recommended.
Equivalent Transistor Parameter Terminology

Collector .......................... Drain
Emitter ............................ Source
Base ................................. Gate
$V_{BR(CES)}$ .......................... $V_{BR(DSS)}$
$V_{CB(O)}$ ............................. $V_{DGO}$
$I_C$ ................................. $I_D$
$I_{CES}$ .............................. $I_{GSS}$
$I_{EBO}$ ............................... $I_{GSS}$
$V_{BE(on)}$ ........................... $V_{GS(th)}$
$V_{CE(sat)}$ ........................... $V_{DS(on)}$
$C_{gb}$ ............................... $C_{oss}$
$C_{be}$ ............................... $C_{oss}$
$R_{ne}$ ............................... $S_{ds}$

$$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C} \quad \text{and} \quad f_{DS(on)} = \frac{V_{DS(on)}}{I_D}$$

Package Dimensions

CASE 211-07
ISSUE N
MRF148A

Linear RF Power FET
30W, to 175MHz, 50V

Rev. V1

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