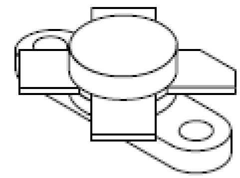
MRF148A

Linear RF Power FET
30W, to 175MHz, 50V

Rev. V1

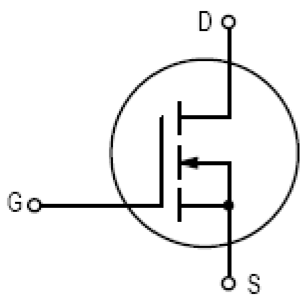
Product Image



CASE 211–07, STYLE 2

Designed for power amplifier applications in industrial, commercial and amateur radio equipment to 175MHz.

- Superior high order IMD
  IMD(d3) (30W PEP): –35 dB (Typ.)
  IMD(d11) (30W PEP): –60 dB (Typ.)
- Specified 50V, 30MHz characteristics:
  Output power: 30W
  Gain: 18dB (Typ.)
  Efficiency: 40% (Typ.)
- 100% tested for load mismatch at all phase angles with 30:1 VSWR
- Lower reverse transfer capacitance (3.0 pF typ.)



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	120	Vdc
Drain–Gate Voltage	V_{DGO}	120	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	6.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.66	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	°C/W

NOTE – CAUTION – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 10 mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 V, V_{GS} = 0)	I_{DSS}	—	—	1.0	mAdc
Gate–Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 10 mA)	$V_{GS(th)}$	1.0	2.5	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 2.5 A)	$V_{DS(on)}$	1.0	3.0	5.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2.5 A)	g_{fs}	0.8	1.2	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	62	—	pF
Output Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	35	—	pF
Reverse Transfer Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	3.0	—	pF
FUNCTIONAL TESTS (SSB)					
Common Source Amplifier Power Gain (30 MHz) (V_{DD} = 50 V, P_{out} = 30 W (PEP), I_{DQ} = 100 mA) (175 MHz)	G_{ps}	— —	18 15	— —	dB
Drain Efficiency (30 W PEP) (V_{DD} = 50 V, f = 30 MHz, I_{DQ} = 100 mA) (30 W CW)	η	— —	40 50	— —	%
Intermodulation Distortion (V_{DD} = 50 V, P_{out} = 30 W (PEP), f = 30; 30.001 MHz, I_{DQ} = 100 mA)	$IMD_{(d3)}$ $IMD_{(d11)}$	— —	−35 −60	— —	dB
Load Mismatch (V_{DD} = 50 V, P_{out} = 30 W (PEP), f = 30; 30.001 MHz, I_{DQ} = 100 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			
CLASS A PERFORMANCE					
Intermodulation Distortion (1) and Power Gain (V_{DD} = 50 V, P_{out} = 10 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 1.0 A)	G_{PS} $IMD_{(d3)}$ $IMD_{(d9-13)}$	— — —	20 −50 −70	— — —	dB

NOTE:
1. To MIL–STD–1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.

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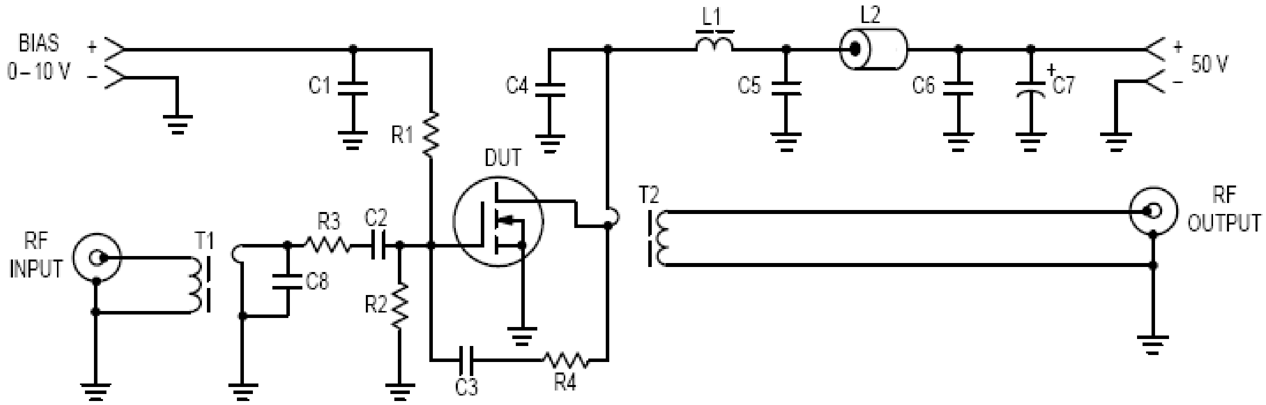

C1, C2, C3, C4, C5, C6 — 0.1 µF Ceramic Chip or Equivalent
C7 — 10 µF, 100 V Electrolytic
C8 — 100 pF Dipped Mica
L1 — VK200 20/4B Ferrite Choke or Equivalent (3.0 µH)
L2 — Ferrite Bead(s), 2.0 µH

R1, R2 — 200 Ω, 1/2 W Carbon
R3 — 4.7 Ω, 1/2 W Carbon
R4 — 470 Ω, 1.0 W Carbon
T1 — 4:1 Impedance Transformer
T2 — 1:2 Impedance Transformer

Figure 1. 2.0 to 50 MHz Broadband Test Circuit

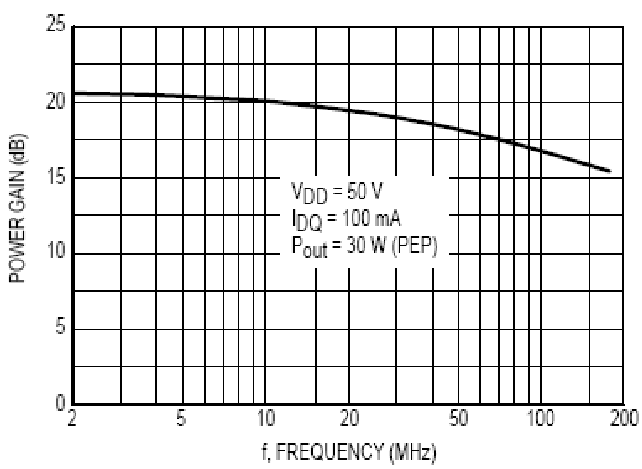

Figure 2. Power Gain versus Frequency

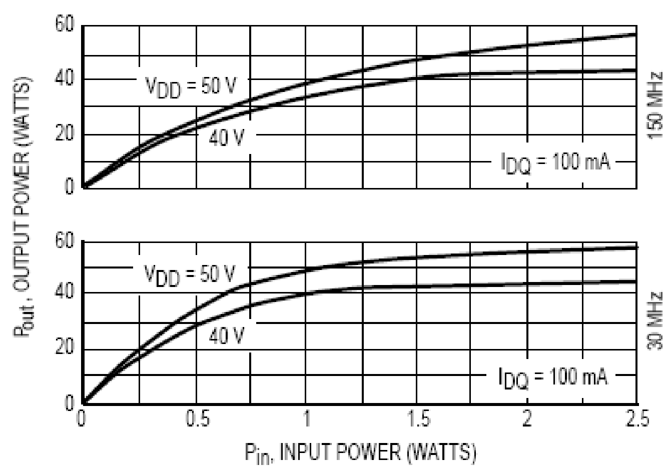

Figure 3. Output Power versus Input Power

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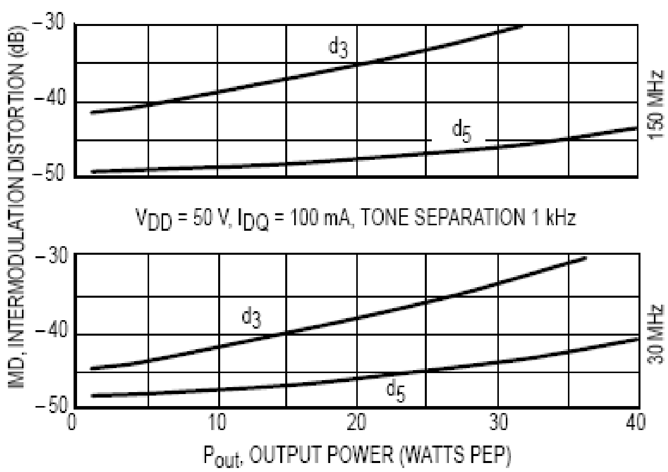


Figure 4. IMD versus P_{out}

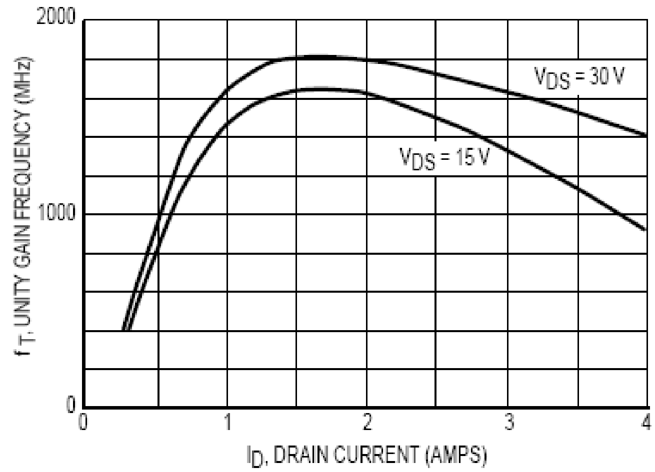
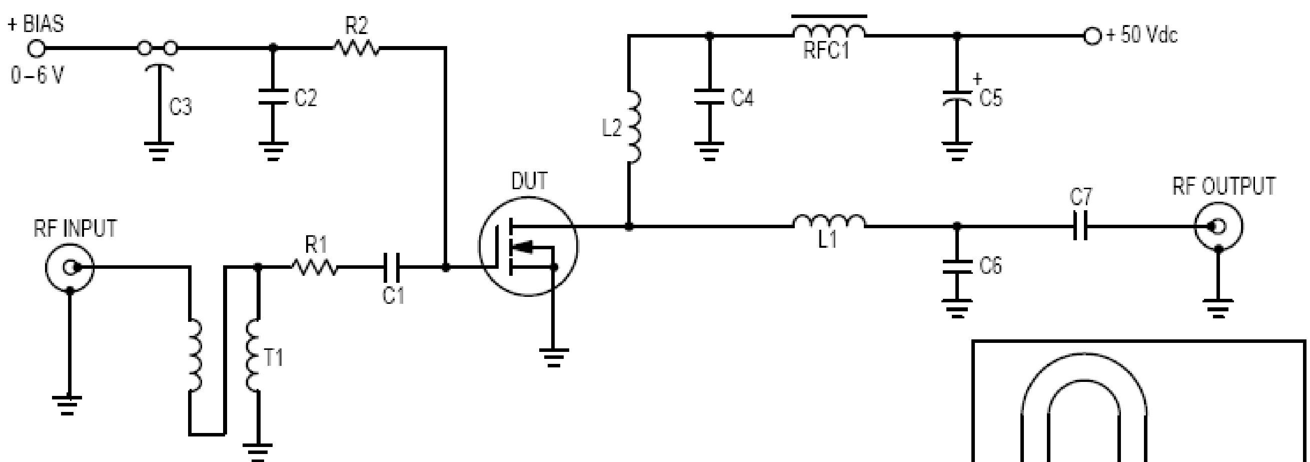


Figure 5. Common Source Unity Gain Frequency versus Drain Current



C1 — 91 pF Unelco Type MCM 01/010
C2, C4 — 0.1 µF Erie Red Cap
C3 — Allen Bradley 680 pF Feed Thru
C5 — 1.0 µF, 50 Vdc Electrolytic
C6 — 15 pF Unelco Type J101
C7 — 24 pF Unelco Type MCM 01/010
L1 — 2 Turns #18 AWG, 5/16″ ID
L2 — 4 Turns #18 AWG, 5/16″ ID
R1 — 1.0 Ohm, 1/4 W Carbon
R2 — 2000 Ohm, 1/4 W Carbon
RFC1 — VK200 21/4B
T1 — 4:1 Transformer, 1.75″ Subminiature Coaxial Cable

Figure 6. 150 MHz Test Circuit

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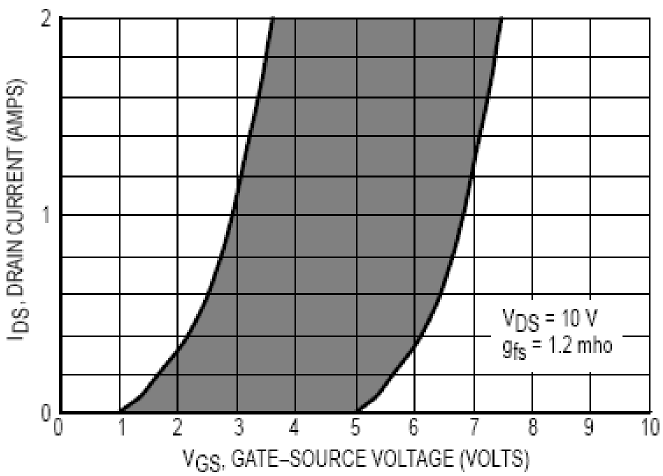


Figure 7. Gate Voltage versus Drain Current

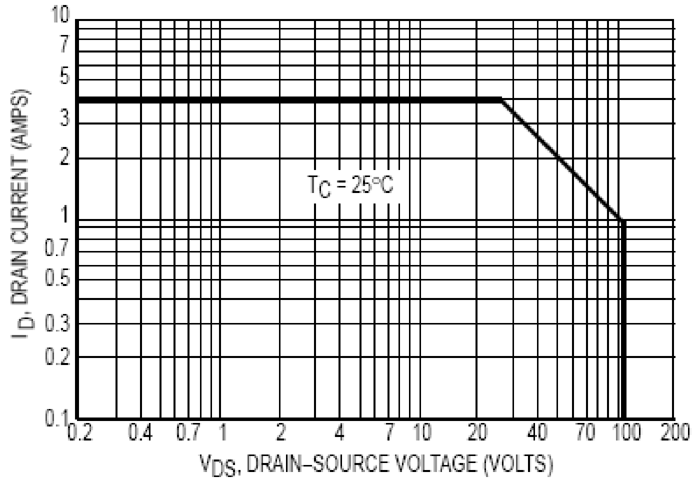
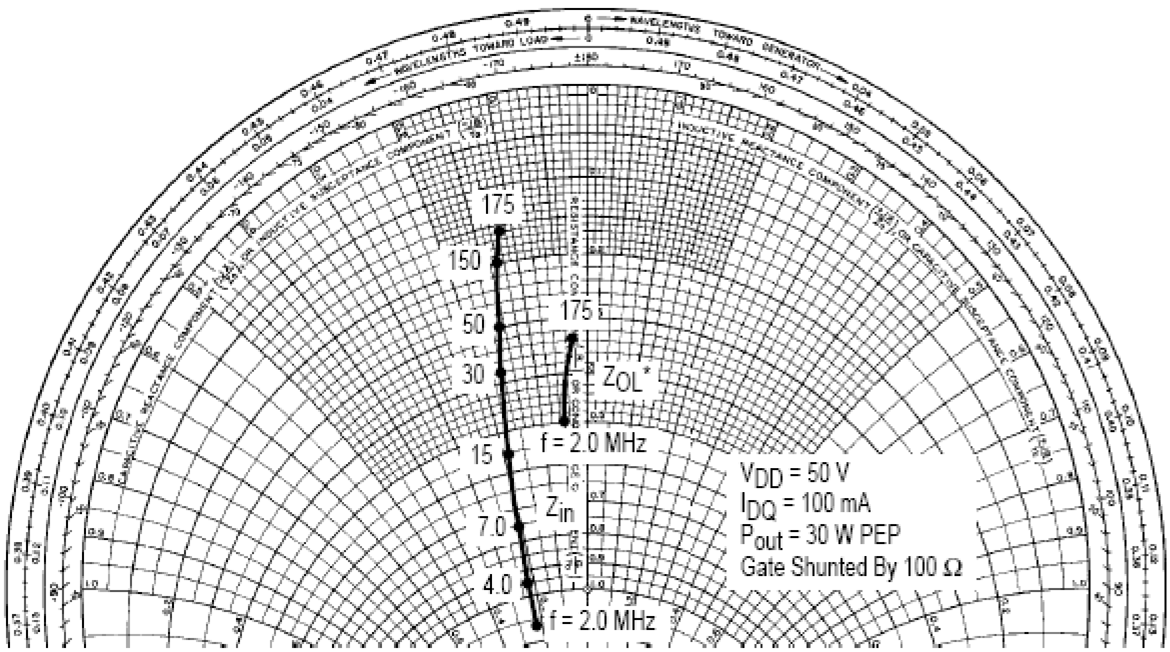


Figure 8. DC Safe Operating Area (SOA)



Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 9. Impedance Coordinates — 50 Ohm Characteristic Impedance

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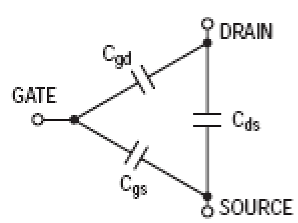
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



$C_{iss} = C_{gd} + C_{gs}$
$C_{oss} = C_{gd} + C_{ds}$
$C_{rss} = C_{gd}$

LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended.

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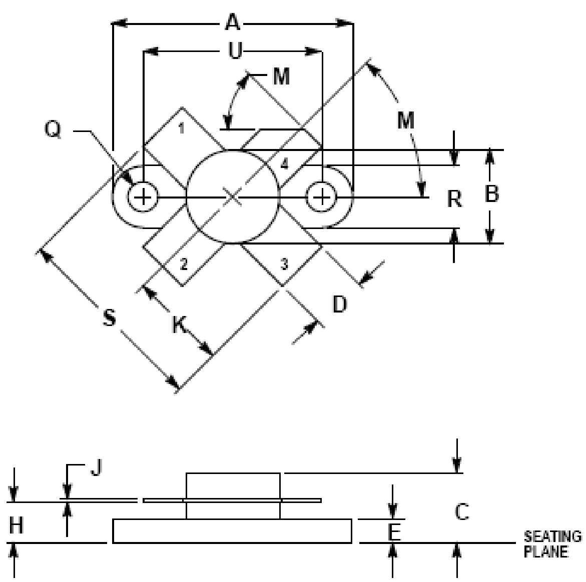
EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

Collector	Drain
Emitter	Source
Base	Gate
$V_{(BR)CES}$	$V_{(BR)DSS}$
V_{CBO}	V_{DGO}
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
$V_{BE(on)}$	$V_{GS(th)}$
$V_{CE(sat)}$	$V_{DS(on)}$
C_{ib}	C_{iss}
C_{ob}	C_{oss}
h_{fe}	g_{fs}
$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$	$r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.960	0.990	24.39	25.14
B	0.370	0.390	9.40	9.90
C	0.229	0.281	5.82	7.13
D	0.215	0.235	5.47	5.96
E	0.085	0.105	2.16	2.66
H	0.150	0.108	3.81	4.57
J	0.004	0.006	0.11	0.15
K	0.395	0.405	10.04	10.28
M	40°	50°	40°	50°
Q	0.113	0.130	2.88	3.30
R	0.245	0.255	6.23	6.47
S	0.790	0.810	20.07	20.57
U	0.720	0.730	18.29	18.54

STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

CASE 211–07
ISSUE N

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