Linear RF Power FET
30W, to 175MHz, 50V

Designed for power amplifier applications in industrial, commercial and amateur radio equipment to 175MHz.

- Superior high order IMD
  - IMD(d3) (30W PEP): –35 dB (Typ.)
  - IMD(d11) (30W PEP): –60 dB (Typ.)

- Specified 50V, 30MHz characteristics:
  - Output power: 30W
  - Gain: 18dB (Typ.)
  - Efficiency: 40% (Typ.)

- 100% tested for load mismatch at all phase angles with 30:1 VSWR
- Lower reverse transfer capacitance (3.0 pF typ.)

MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain–Source Voltage</td>
<td>VDSS</td>
<td>120</td>
<td>Vdc</td>
</tr>
<tr>
<td>Drain–Gate Voltage</td>
<td>VGS</td>
<td>±40</td>
<td>Vdc</td>
</tr>
<tr>
<td>Gate–Source Voltage</td>
<td>ID</td>
<td>6.0</td>
<td>A</td>
</tr>
<tr>
<td>Drain Current — Continuous</td>
<td>PD</td>
<td>115</td>
<td>Watts</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>Tstg</td>
<td>–65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td>TJ</td>
<td>200</td>
<td>°C</td>
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THERMAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Resistance, Junction to Case</td>
<td>Rjuc</td>
<td>1.52</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

NOTE – CAUTION – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.
**MRF148A**

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**ELECTRICAL CHARACTERISTICS**  \( T_C = 25^\circ C \) unless otherwise noted.

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain–Source Breakdown Voltage ( (V_{GS} = 0, I_D = 10 \text{mA}) )</td>
<td>( V_{(BR)DSS} )</td>
<td>125</td>
<td>—</td>
<td>—</td>
<td>Vdc</td>
</tr>
<tr>
<td>Zero Gate Voltage Drain Current ( (V_{DS} = 50 \text{V}, V_{GS} = 0) )</td>
<td>( I_{DSS} )</td>
<td>—</td>
<td>—</td>
<td>1.0</td>
<td>mA/dc</td>
</tr>
<tr>
<td>Gate–Body Leakage Current ( (V_{GS} = 20 \text{V}, V_{DS} = 0) )</td>
<td>( I_{GSS} )</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>nA/dc</td>
</tr>
</tbody>
</table>

**OFF CHARACTERISTICS**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Threshold Voltage ( (V_{DS} = 10 \text{V}, I_D = 10 \text{mA}) )</td>
<td>( V_{GS(th)} )</td>
<td>1.0</td>
<td>2.5</td>
<td>5.0</td>
<td>Vdc</td>
</tr>
<tr>
<td>Drain–Source On–Voltage ( (V_{GS} = 10 \text{V}, I_D = 2.5 \text{A}) )</td>
<td>( V_{DS(on)} )</td>
<td>1.0</td>
<td>3.0</td>
<td>5.0</td>
<td>Vdc</td>
</tr>
<tr>
<td>Forward Transconductance ( (V_{DS} = 10 \text{V}, I_D = 2.5 \text{A}) )</td>
<td>( g_{fs} )</td>
<td>0.8</td>
<td>1.2</td>
<td>—</td>
<td>mhos</td>
</tr>
</tbody>
</table>

**ON CHARACTERISTICS**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Capacitance ( (V_{GS} = 50 \text{V}, V_{GSS} = 0, f = 1.0 \text{MHz}) )</td>
<td>( C_{iss} )</td>
<td>—</td>
<td>62</td>
<td>—</td>
<td>pF</td>
</tr>
<tr>
<td>Output Capacitance ( (V_{DS} = 50 \text{V}, V_{GSS} = 0, f = 1.0 \text{MHz}) )</td>
<td>( C_{oss} )</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>pF</td>
</tr>
<tr>
<td>Reverse Transfer Capacitance ( (V_{DS} = 50 \text{V}, V_{GSS} = 0, f = 1.0 \text{MHz}) )</td>
<td>( C_{rss} )</td>
<td>—</td>
<td>3.0</td>
<td>—</td>
<td>pF</td>
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**DYNAMIC CHARACTERISTICS**

<table>
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<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Common Source Amplifier Power Gain ( (V_{DD} = 50 \text{V}, P_{out} = 30 \text{W} (\text{PEP}), I_{DQ} = 100 \text{mA}) ) ( (30 \text{MHz}) )</td>
<td>( G_{ps} )</td>
<td>—</td>
<td>18</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Drain Efficiency ( (V_{DD} = 50 \text{V}, f = 30 \text{MHz}, I_{DQ} = 100 \text{mA}) ) ( (30 \text{W PEP}) )</td>
<td>( \eta )</td>
<td>—</td>
<td>40</td>
<td>—</td>
<td>%</td>
</tr>
<tr>
<td>Intermodulation Distortion ( (V_{DD} = 50 \text{V}, P_{out} = 30 \text{W} (\text{PEP}), f = 30, 30.001 \text{MHz}, I_{DQ} = 100 \text{mA}) ) ( (30 \text{W CW}) )</td>
<td>( \text{IMD(d3)} )</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Load Mismatch ( (V_{DD} = 50 \text{V}, P_{out} = 30 \text{W} (\text{PEP}), f = 30; 30.001 \text{MHz}, I_{DQ} = 100 \text{mA}, \text{VSWR 30:1 at all Phase Angles}) )</td>
<td>( \psi )</td>
<td>No Degradation in Output Power</td>
<td></td>
<td></td>
<td></td>
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**FUNCTIONAL TESTS (SSB)**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intermodulation Distortion ( (V_{DD} = 50 \text{V}, P_{out} = 10 \text{W} (\text{PEP}), f_1 = 30 \text{MHz}, f_2 = 30.001 \text{MHz}, I_{DQ} = 1.0 \text{A}) )</td>
<td>( \text{IMD(d3)} )</td>
<td>—</td>
<td>20</td>
<td>—</td>
<td>dB</td>
</tr>
</tbody>
</table>

**NOTE:**
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**Figure 1. 2.0 to 50 MHz Broadband Test Circuit**

- C1, C2, C3, C4, C5, C6 — 0.1 μF Ceramic Chip or Equivalent
- C7 — 10 μF, 100 V Electrolytic
- C8 — 100 pF Dipped Mica
- L1 — VK200 20/4B Ferrite Choke or Equivalent (3.0 μH)
- L2 — Ferrite Bead(s), 2.0 μH
- R1, R2 — 200 Ω, 1/2 W Carbon
- R3 — 4.7 Ω, 1/2 W Carbon
- R4 — 4.70 Ω, 1.0 W Carbon
- T1 — 4:1 Impedance Transformer
- T2 — 1:2 Impedance Transformer

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**Figure 2. Power Gain versus Frequency**

- VDD = 50 V
- IDQ = 100 mA
- Pout = 30 W (FEP)

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**Figure 3. Output Power versus Input Power**

- VDD = 50 V
- 40 V
- IDQ = 100 mA
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Rev. V1

Figure 4. IMD versus Pout

Figure 5. Common Source Unity Gain Frequency versus Drain Current

Figure 6. 150 MHz Test Circuit

C1 — 91 pF Unelco Type MCM 01/010
C2, C4 — 0.1 µF Elna Red Cap
C3 — Allen Bradley 680 pF Feed Thru
C5 — 1.0 µF, 50 Vdc Electrolytic
C6 — 15 pF Unelco Type J101
C7 — 24 pF Unelco Type MCM 01/010
L1 — 2 Turns #18 AWG, 5’16” ID
L2 — 4 Turns #18 AWG, 5’16” ID
RFC1 — VK200 21/4B
T1 — 4:1 Transformer, 1.75” Subminiature Coaxial Cable
R1 — 1.0 Ohm, 1/4 W Carbon
R2 — 2000 Ohm, 1/4 W Carbon
+ 50 Vdc
+ Bias
0—6 V
RF INPUT

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Figure 7. Gate Voltage versus Drain Current

Figure 8. DC Safe Operating Area (SOA)

Figure 9. Impedance Coordinates — 50 Ohm Characteristic Impedance

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RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES
The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during the fabrication of the RF MOSFET results in a junction capacitance from drain-to-source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:
1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.

Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS
One figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS
The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of $10^6$ ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated $V_{GS}$ can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open—circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended.

LINEARITY AND GAIN CHARACTERISTICS
In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to $f_T$ for bipolar transistors.
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EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

- Collector
- Emitter
- Base
- V(BR)CES
- V(CBO)
- Ic
- ICE
- V(BR)DSS
- V(DSS)
- V(geo)
- Id
- I(GSS)
- Ciss
- Ciss
- Rd
- Vgs(th)

\[ R_{CE(sat)} = \frac{V_{CE(sat)}}{Ic} \]
\[ R_{DS(on)} = \frac{V_{DS(on)}}{I_{D_{sat}}} \]

PACKAGE DIMENSIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: INCH

<table>
<thead>
<tr>
<th>STYLE</th>
<th>PIN 1</th>
<th>SOURCE</th>
<th>2</th>
<th>GATE</th>
<th>3</th>
<th>SOURCE</th>
<th>4</th>
<th>DRAIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>J</td>
<td></td>
<td></td>
<td></td>
<td>H</td>
<td></td>
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<td></td>
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<td></td>
<td></td>
<td>D</td>
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CASE 211–07
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