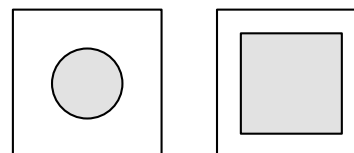


### Features

- Dual Insulating Layer (Nitride-Oxide) for Maximum Reliability
- Low Loss: 0.04 dB in a 50 Ω System
- Maximum Pad Area for Ribbon or Multiple Bonds
- Very Low Temperature Coefficient
- RoHS\* Compliant



### Applications

- DC Blocking
- Bypass
- Tuning

### Description

The MIS (metal-insulating layer-silicon) chip capacitors are devices that have a very high Q and small size for use in microwave hybrid circuit applications. Large rectangular contacts are supplied on most units with the periphery of the contact being typically 2 mils from the edge allowing wire or ribbon bonding near the edge for the lowest practical inductance.

The dielectric layer is composed of a thermally grown silicon dioxide over which a thicker layer of silicon nitride is deposited. This layer is carried out to the edge of the chip. The end result is a capacitor having a thin, high breakdown dielectric resulting in a high capacitance per unit area. This dual insulating layer exhibits a low temperature coefficient, very high insulation resistance and much lower insertion loss at microwave frequencies than porcelain capacitors. These MIS devices (sometimes referred to as MNOS) exhibit long term stability under bias conditions at high temperatures (as compared to the earlier MOS technology) making them suitable for high reliability applications.

These MIS chip capacitors provide much improved performance over other types in hybrid microwave circuits. They provide low loss in supply decoupling circuits and GaAs FET transistor source bypass (providing more gain per stage). They can also be used as tuning elements in various filters and matching networks. Detector diodes and transistors can be mounted on them also to provide DC isolation and a tuning or bypass capacitor to ground. Switch and comb generator performance is significantly improved using MIS capacitors. There are no resonance problems associated with MIS devices.

### 50 V Electrical Specifications:

$I_R = 10 \mu A$ ,  $T_A = +25^\circ C$

Part #	Junction Capacitance $V_R = 0 V$ , 1 MHz	Available Outline
MCC50	20	C
	25	F
	50	D
	100	G

### 100 V Electrical Specifications:

$I_R = 10 \mu A$ ,  $T_A = +25^\circ C$

Part #	Junction Capacitance $V_R = 0 V$ , 1 MHz	Available Outline
MCC100	1	A
	2	B
	5	C
	10	B
	15	B
	20	D
	25	C

### Ordering Information

Part Number	Package
MCCx-y-z <sup>1</sup>	100 piece waffle pack

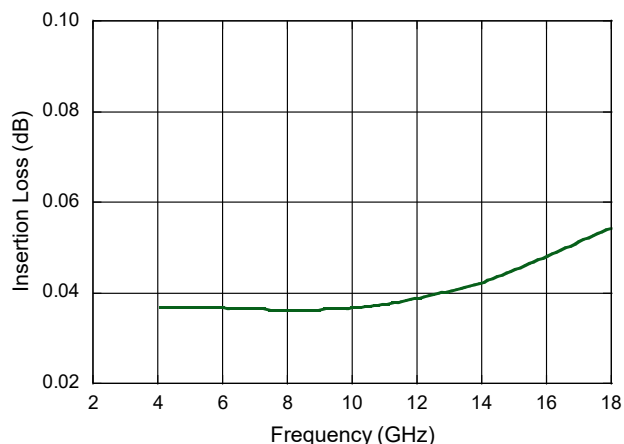
1. x = voltage (either 50 or 100), y = capacitance value, z = available outline.

<sup>1</sup> \* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

**Electrical Characteristics**

Parameter	Value
Operating Temperature	-65°C to +200°C
Capacitance Range	0.5 pF to 100 pF
Temperature Coefficient	50 PPM / °C typical
Dielectric Withstanding Voltage	50 V & 100 V
Insulation Resistance	10 <sup>6</sup> MΩ typical

**Insertion Loss vs. Frequency (10 pF)**

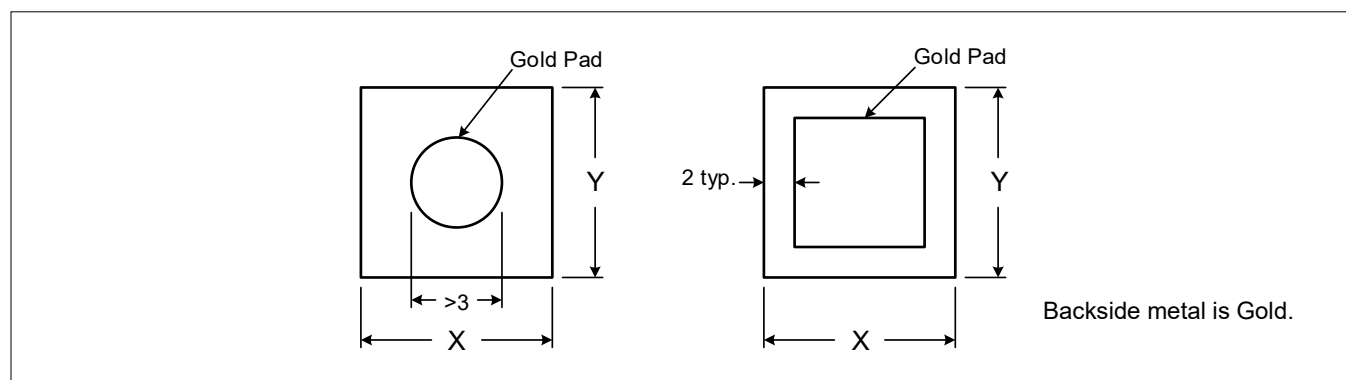


**Die Attach & Wire Bonding**

These chip capacitors are provided with a high quality top pad suitable for thermocompression wire or ribbon bonding. Thermosonic and ultrasonic bonding or gap welding is not recommended as the thin insulating layer could be cracked with these techniques.

The backside metal system is suitable for long term eutectic die attach without breaking down, as may be required when mounting several devices on a hybrid substrate. Gold-tin or gold-germanium eutectic solders are suitable. Epoxy die attach is also acceptable.

**Outline**



**Maximum Dimensions (mils)**

Outline	A	B	C	D	E	F	G	H	I
X	15	10	15	20	22	25	30	40	70
Y	15	10	15	20	42	25	30	40	70
Thickness	4 - 6								

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