Features
- Integrates Image Reject (Balanced) Mixer, LO Buffer, LO Quadrupler and RF Buffer
- 13 dB Conversion Gain
- +20 dBm Input Third Order Intercept (IIP3)
- -30 dBm (4x) LO Leakage (@ RF Port)
- 18 dBc Image Rejection
- Variable Gain with Adjustable Bias
- Lead-Free 4 mm, 24 Lead QFN Package
- RoHS^ Compliant

Description
The MAUC-011009 is an integrated up-converter that has a typical conversion gain of 13 dB, and an image rejection of 18 dBc. The device includes a LO quadrupler, LO buffer amplifier, and RF buffer amplifier. Variable gain can be achieved by adjusting the bias, with turn-down trajectories optimized to maintain linearity and 4x LO leakage over the gain control range. The output IP3 is 32 dBm at maximum gain.

The MAUC-011009 is ideally suited for 38 GHz band point-to-point radios under both LSB and USB operation.

Each device is 100% RF tested to ensure performance compliance.

Ordering Information^1,2

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAUC-011009-TR0500</td>
<td>500 Piece Reel</td>
</tr>
<tr>
<td>MAUC-011009-000SMB</td>
<td>Sample Board</td>
</tr>
</tbody>
</table>

1. Reference Application Note M513 for reel size information.
2. All sample boards include 3 loose parts.

## Electrical Specifications

**LO = 0 dBm, IF = -10 dBm, T_A = +25°C**

\( V_D1 = V_D2 = V_D3 = 4 \text{ V}, I_D1 = 45 \text{ mA}, I_D2 = 135 \text{ mA}, I_D3 = 200 \text{ mA} \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Units</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency Range (RF)</td>
<td>GHz</td>
<td>37</td>
<td>—</td>
<td>40</td>
</tr>
<tr>
<td>Frequency Range (LO)</td>
<td>GHz</td>
<td>8.375</td>
<td>—</td>
<td>10.875</td>
</tr>
<tr>
<td>Frequency Range (IF)</td>
<td>GHz</td>
<td>DC</td>
<td>—</td>
<td>3.5</td>
</tr>
<tr>
<td>LO Input Power (PLO)</td>
<td>dBm</td>
<td>—</td>
<td>0</td>
<td>—</td>
</tr>
<tr>
<td>USB Conversion Gain (IF = 3.5 GHz)</td>
<td>dB</td>
<td>9.5</td>
<td>13</td>
<td>—</td>
</tr>
<tr>
<td>Image Rejection</td>
<td>dBc</td>
<td>—</td>
<td>18</td>
<td>—</td>
</tr>
<tr>
<td>Input IP3 (P_IN = -10 dBm/tone, IF = 3.5 GHz, ( \Delta IF = 10 \text{ MHz} ))</td>
<td>dBm</td>
<td>—</td>
<td>19</td>
<td>—</td>
</tr>
<tr>
<td>USB Output IP3 (P_IN = -10 dBm/tone, IF = 3.5 GHz, ( \Delta IF = 10 \text{ MHz} ))</td>
<td>dBm</td>
<td>28</td>
<td>32</td>
<td>—</td>
</tr>
<tr>
<td>Spurious (4xLO) (tuned - IF voltages ~ 0.2 V)</td>
<td>dBm</td>
<td>—</td>
<td>-30</td>
<td>—</td>
</tr>
<tr>
<td>Spurious (1xLO)</td>
<td>dBm</td>
<td>—</td>
<td>-70</td>
<td>—</td>
</tr>
<tr>
<td>RF Return Loss</td>
<td>dB</td>
<td>—</td>
<td>10</td>
<td>—</td>
</tr>
<tr>
<td>LO Return Loss</td>
<td>dB</td>
<td>—</td>
<td>15</td>
<td>—</td>
</tr>
<tr>
<td>IF Return Loss</td>
<td>dB</td>
<td>—</td>
<td>15</td>
<td>—</td>
</tr>
<tr>
<td>Current, Drain 1 (I_D1)</td>
<td>mA</td>
<td>—</td>
<td>45</td>
<td>—</td>
</tr>
<tr>
<td>Current, Drain 2 (I_D2)</td>
<td>mA</td>
<td>—</td>
<td>135</td>
<td>—</td>
</tr>
<tr>
<td>Current, Drain 3 (I_D3)</td>
<td>mA</td>
<td>—</td>
<td>200</td>
<td>—</td>
</tr>
<tr>
<td>Gate Voltage (V_G4)</td>
<td>V</td>
<td>—</td>
<td>-3.25</td>
<td>—</td>
</tr>
<tr>
<td>Gate Current (I_G4)</td>
<td>mA</td>
<td>—</td>
<td>-1</td>
<td>—</td>
</tr>
</tbody>
</table>

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5. Apply gate voltages prior to drain voltages. Adjust \( V_G1, V_G2 \) and \( V_G3 \) between -1.0 and -0.1 V to achieve specified drain current. Typical current 380 mA = 45 (I_D1) + 135 (I_D2) + 200 (I_D3) mA. Refer to App Note [1] for biasing details.
Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Absolute Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain Voltage</td>
<td>+4.3 V</td>
</tr>
<tr>
<td>Gate Bias Voltage (V_G1,2,3)</td>
<td>-1.5 V &lt; V_G &lt; +0.3 V</td>
</tr>
<tr>
<td>Gate Bias Voltage (V_G4)</td>
<td>-4.0 V &lt; V_G &lt; 0 V</td>
</tr>
<tr>
<td>Input Power</td>
<td>10 dBm</td>
</tr>
<tr>
<td>LO Input Power</td>
<td>13 dBm</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-55°C to +150°C</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Junction Temperature^8</td>
<td>+150°C</td>
</tr>
</tbody>
</table>

6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. MACOM does not recommend sustained operation near these survivability limits.
8. Junction Temperature \((T_J) = T_C + \Theta_{jc} * (V * I)\)
   Typical thermal resistance \((\Theta_{jc}) = 36°C/W\).

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Biasing Quickstart

**Turn ON:**
Step 1: Turn on the fixed voltage on VG4 first.
Step 2: Turn on VG1, VG2 and VG3 at approximately -1.0V.
Step 3: Turn on IF voltages at the fixed voltage.
Step 4: Turn on VD1, VD2 and VD3 at the fixed voltages, and adjust corresponding VG to get the required current levels.

**Turn OFF:**
Reverse steps indicated in *Turn ON* sequence

For further details please see App Note [1]
Typical Performance Curves: LO = 0 dBm, IF = -10 dBm @ 2 GHz, P_{DC} = 1.52 W

**Conversion Gain**

![Conversion Gain at 37 GHz](image1)

![Conversion Gain at 40 GHz](image2)

**Conversion Gain @ IF = 21.4 MHz**

![Conversion Gain @ IF = 21.4 MHz](image3)

**Conversion Gain @ IF = 3.5 GHz**

![Conversion Gain @ IF = 3.5 GHz](image4)
Typical Performance Curves: LO = 0 dBm, IF = -10 dBm @ 2 GHz, P_{DC} = 1.52 W

Input IP3

Input IP3, LO Power swept

Input IP3 @ 37 GHz

Input IP3 @ 40 GHz

Input IP3, IF = 21.4 MHz

Input IP3, IF = 3.5 MHz
Typical Performance Curves: LO = 0 dBm, IF = -10 dBm @ 2 GHz, $P_{DC} = 1.52$ W

**Output IP3**

**Output IP3, LO Power swept**

**Output IP3 @ 37 GHz**

**Output IP3 @ 40 GHz**

**Output IP3, IF = 21.4 MHz**

**Output IP3, IF = 3.5 GHz**

MAUC-011009

Up Converter
37 - 40 GHz

Rev. V2

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Up Converter
37 - 40 GHz

Typical Performance Curves: LO = 0 dBm, IF = -10 dBm @ 2 GHz, P_{DC} = 1.52 W

P_{OUT} vs. P_{IN}

P_{1dB, Input & Output}

P_{OUT} vs. P_{IN} @ IF = 21.4 MHz

P_{1dB, @ Input & Output, IF = 21.4 MHz}

P_{OUT} vs. P_{IN} @ IF = 3.5 GHz

P_{1dB, @ Input & Output, IF = 3.5 GHz}
Up Converter
37 - 40 GHz

Typical Performance Curves: LO = 0 dBm, IF = -10 dBm @ 2 GHz, P_{DC} = 1.52 W

Image Rejection

Image Rejection, LO Power swept

Image Rejection, IF = 21.4 MHz

Image Rejection, IF = 3.5 GHz

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MAUC-011009

Up Converter
37 - 40 GHz

Typical Performance Curves

1xLO Leakage @ RF port

![1xLO Leakage @ RF port graph]

2xLO Leakage @ RF Port

![2xLO Leakage @ RF Port graph]

3xLO Leakage @ RF Port

![3xLO Leakage @ RF Port graph]

4xLO Leakage @ RF Port

![4xLO Leakage @ RF Port graph]

5xLO Leakage @ RF Port

![5xLO Leakage @ RF Port graph]

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Typical Performance Curves

IF Return Loss

RF Return Loss

LO Return Loss

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App Note [1] Biasing

MAUC-011009 is operated by biasing \( V_{D1}, V_{D2} \) and \( V_{D3} \) at 4.0 V. The corresponding drain currents are set to 45 mA, 135 mA and 200 mA respectively. \( V_{G4} \) requires a fixed voltage bias of nominally -3.25 V. It is recommended to use active bias on \( V_{G1}, V_{G2}, V_{G3} \) to keep the currents in \( V_{D1}, V_{D2} \) and \( V_{D3} \) constant, in order to maintain the best performance over temperature. Depending on the supply voltages available and the power dissipation constraints, the bias circuits may include a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply to sense the current. Make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply. If IF bias is to be used, it is important that \( V_{G4} \) is applied first.

App Note [2] IF Inputs

The IF input to the typical configuration is through a 90° hybrid coupler. The hybrid splits the IF input into inphase and quadrature phase components which feed into two 180° hybrid couplers splitting into 4 signals. These four signals enter the MAUC-011009 on \( I/I^*,Q/Q^* \) IF inputs through bias tees. For highest gain, best image rejection and highest OIP3, all the 4 IF inputs should be used. See App Note [4] for IF bias.
App Note [3] Board Layout

As shown in the recommended board layout, it is recommended to provide 100 pF decoupling capacitors as close to the bias pins as possible. Additional 10 nF and 1 µF on each of the bias lines are recommended placed a distance further away.

Recommended Board Layout

App Note [4] IF Bias

To obtain optimum 4xLO leakage performance, tuning is achieved by adjusting the DC bias on each of the IF inputs (I, Q, I*, Q*). DC bias is implemented by adding simple bias tees to each of the four IF ports (see drawing from App Note [2] for the bias tees location). The diagram below shows a typical bias tee design used.

A typical tuning arrangement is to apply a fixed 0.2 V DC bias to I, Q. The remaining two IF ports can be tuned independently between -0.5 and 1 V for minimum 4xLO leakage. Please note that $V_{G4}$ must be applied to the device before IF bias is applied.

For minimum 4xLO leakage in a system, it may be necessary to correct the IF DC bias for different frequency and temperature conditions. This can be implemented by calibration and offset tables stored in memory, and used to control IF bias over all practical conditions.

Typical Configuration
**Lead-Free 4 mm 24-Lead PQFN †**

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.
Plating is NiPdAuAg over copper.
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