Features

- CW Power Handling: 36 dBm
- Insertion Loss:
  0.5 dB @ 3 GHz
  0.7 dB @ 8 GHz
- Isolation:
  60 dB @ 3 GHz
  43 dB @ 8 GHz
- Return Loss at Each RF Port: 18 dB
- Pulsed Input P0.1dB: 39 dBm
- Input IP3: 66 dBm
- 3 mm, 16 lead PQFN Package
- RoHS* Compliant

Applications

- Test and Measurement
- Automated Test Equipment
- Microwave Radios & VSAT
- Defense Radar and ECMs
- General Purpose Tx/Rx Switch

Description

The MASW-011248 is an absorptive wideband single pole double throw (SPDT) switch with 0.7 dB of insertion loss and 43 dB isolation at 8 GHz. The RF output ports are terminated in 50 Ω in the isolated path. The power handling capability is 36 dBm CW. The input and output return losses in the thru path are typically 18 dB. The on-die negative bias generator allows single positive bias operation, and can be disabled if spurious-free performance is desired.

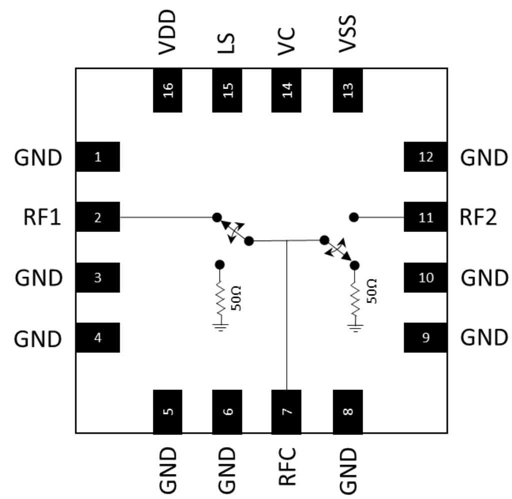
The MASW-011248 is manufactured on a Silicon-on -Insulator process. The 3 x 3 mm QFN package is lead free and RoHS compliant.

Ordering Information[1,2]

Part Number	Package
MASW-011248-TR1000	1000 Piece Reel
MASW-011248-TR3000	3000 Piece Reel
MASW-011248-SMB	Sample Board

1. Reference Application Note M513 for reel size information.
2. All sample boards include 5 loose parts.

Functional Schematic



Pin Configuration[3]

Pin #	Pin Name	Description
1,3-6,8-10,12	GND	Ground
2	RF1[4]	RF Input/Output 1
7	RFC[4]	Common RF Input/Output
11	RF2[4]	RF Input/Output 2
13	VSS[5]	-3.3 V or Ground
14	VC	Control
15	LS[6]	Level Select
16	VDD[7]	Positive Bias

3. The exposed pad centered on the package bottom must be connected to RF, DC, and thermal ground.
4. RF ports are DC-coupled to GND. There are no internal DC blocking capacitors.
5. Connect VSS to ground to enable on-die negative voltage generator.
6. LS is used to configure control pin logic levels for the convenience of application.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications[7]: VDD = +3.3 V, VSS = 0 V or -3.3 V, T_{BASE} = 25°C, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Insertion Loss, RFC to RF1/2	9 kHz - 50 MHz 10 MHz - 3 GHz 3 GHz - 8 GHz 8 GHz - 13 GHz	dB	—	0.40 0.50 0.70 0.90	0.70 1.00 1.05 1.50
Isolation, RFC to RF1/2	9 kHz - 50 MHz 10 MHz - 3 GHz 3 GHz - 8 GHz 8 GHz - 13 GHz	dB	— 45 33 20	80 60 43 32	—
Isolation, between RF1 and RF2	9 kHz - 50 MHz 10 MHz - 3 GHz 3 GHz - 8 GHz 8 GHz - 13 GHz	dB	—	80 54 45 35	—
RFC Return Loss	9 kHz - 50 MHz 10 MHz - 3 GHz 3 GHz - 8 GHz 8 GHz - 13 GHz	dB	—	28 25 18 17	—
RF1/RF2 Return Loss, Thru Port	9 kHz - 50 MHz 10 MHz - 3 GHz 3 GHz - 8 GHz 8 GHz - 13 GHz	dB	—	27 24 18 20	—
RF1/RF2 Return Loss, Isolated Port	9 kHz - 50 MHz 10 MHz - 3 GHz 3 GHz - 8 GHz 8 GHz - 13 GHz	dB	—	28 27 23 21	—
Input P0.1 dB, pulse	pulse width = 1 µs, duty cycle = 0.1% 0.8 to 3.8 GHz	dBm	—	39	—
Input IP2	834 MHz and 1950 MHz P_{IN} = +20 dBm, Δf = 1 MHz	dBm	—	120	—
Input IP3	834 MHz, 1950 MHz and 2700 MHz P_{IN} = +20 dBm, Δf = 1 MHz	dBm	—	66	—
T_{ON}/T_{OFF}	50% control to 90%/10% RF	µs	—	4.5	6.5
Settling time	50% control to 0.05 dB final value	µs	—	8.7	12.5
Switching Rate[8]	VSS = 0 V	kHz	—	—	25
Logic Voltage	Input High (V_{IH})[9] Input Low (V_{IL})	V	1.2 0.0	1.8 0.0	3.45 0.60
Logic Pin Current (VC)	VC = +1.8 V	µA	—	—	7
Voltage Supply, VDD	VSS = 0 V VSS = -3.3 V	V	+2.3 +2.6	+3.3 +3.3	+5.5 +5.5
Supply Current, VDD	VSS = 0 V VSS = -3.3 V	µA	—	47 14	80 25
Voltage Supply, VSS	VSS = -3.3 V	V	-3.6	-3.3	-2.6
Supply Current, VSS	VSS = -3.3V	µA	—	-8.9	—

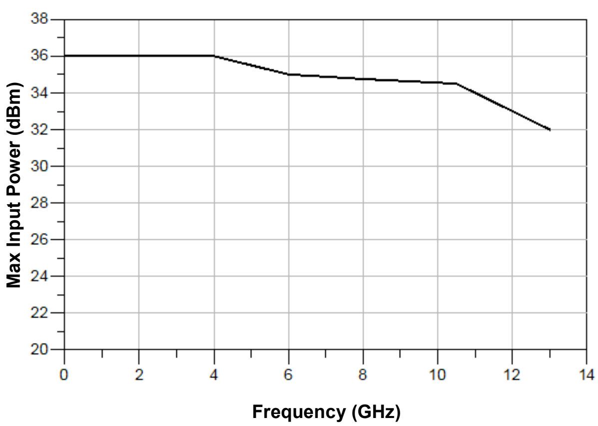
7. RF performance will degrade when VDD is less than 2.6 V.
8. For higher switching rate and spurious free operation, apply -3.3 V to VSS to disable internal negative voltage generator. Switching rate is defined as 1 over the time between two consecutive switching events.
9. For VDD < +3.3 V, control voltage shall not be higher than VDD + 0.3 V.

Maximum Operating Ratings

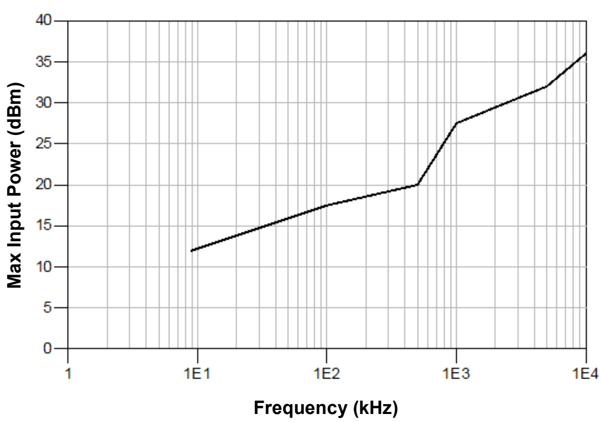
Parameter	Maximum
Input Power, 10 MHz to 4 GHz, RFC to RF1/RF2 Thru Path[10]	36 dBm
Input Power, 800 kHz to 13 GHz, RF1/RF2 Terminated Path[10]	26 dBm
VDD	-0.3 to +5.25 V
VC and LS	Note 11
Operating Temperature[12]	-40 to +85°C

10. T_{PADDLE} = 85 ºC. See power derating curves for details.
11. The minimum input voltage for VC and LS is -0.3 V. The maximum input voltage for VC and LS is the lower value of VDD+0.3 V and +3.45 V.
12. Guarantees 10 years lifetime.

Max Input Power (CW)



Max Input Power (CW) below 10 MHz



Absolute Maximum Ratings[13,14,15]

Parameter	Absolute Maximum
Input Power, 10 MHz to 4 GHz, RFC to RF1/RF2 Thru Path[10]	37 dBm
Input Power, 800 kHz to 8 GHz, RF1/RF2 Terminated Path[10]	28 dBm
VDD	-0.3 to +5.5 V
VSS	-3.6 to +0.3 V
VC and LS	Note 16
Junction Temperature[17,18]	+135°C

13. Exceeding any one or combination of these limits may cause permanent damage to this device.
14. MACOM does not recommend sustained operation near these survivability limits.
15. Based on testing with input power applied for 30 seconds.
16. The absolute minimum input voltage for VC and LS is -0.3 V. The absolute maximum input voltage for VC and LS is the lower value of VDD+0.3 V and +3.6 V.
17. Junction Temperature (T_J) = T_C + Ɵjc * (V * I) Typical thermal resistance (Ɵjc) = 18 ºC/W.
18. Thermal resistance cannot be used to determine maximum input power over operating temperature. The maximum input power and power de-rating curves apply to the whole operating temperature ranges.

Truth Table

Control Input		Condition of Switch	
LS	VC	RFC - RF1 Path	RFC - RF2 Path
V_{IL}	V_{IL}	Off	On
V_{IL}	V_{IH}	On	Off
V_{IH}	V_{IL}	On	Off
V_{IH}	V_{IH}	Off	On

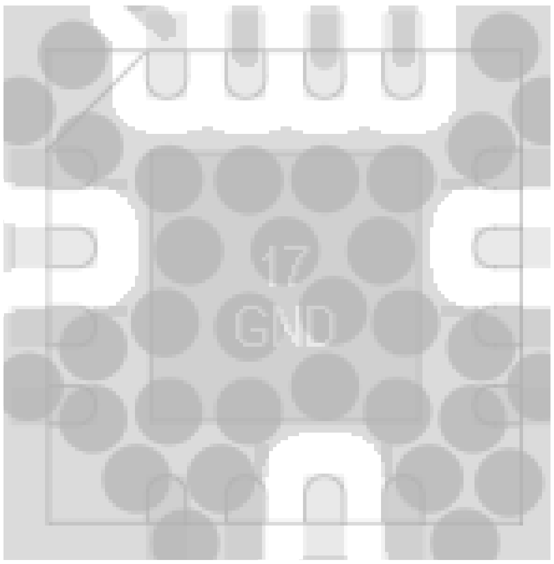
Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1C and CDM Class C3 devices.

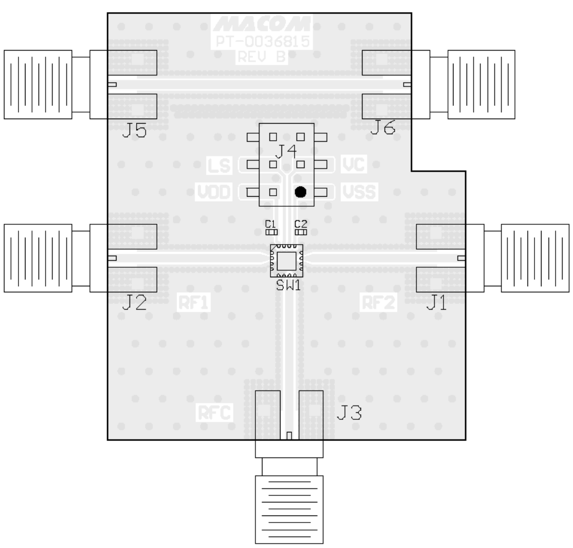
Recommended PCB Footprint

The evaluation PCB of the MASW-011248 is a 4-layer board with 16 mil Rogers RO4003C dielectric material on top layer and 1 oz. copper on primary and secondary metal layers. For this stack-up, the recommended PCB footprint is shown below.

The 50Ω RF transmission lines are CPWG of 28.5 mil width with 10 mil gap.



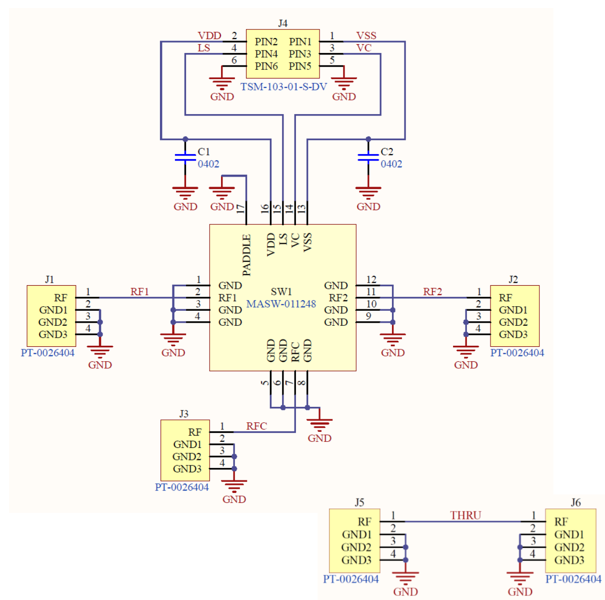
Evaluation Board Layout



Power Supplies

De-coupling capacitors should be placed at the VDD and VSS supply pins to minimize noise and fast transients. Supply voltage change or transients should have a slew rate smaller than 1 V / 30 µs for VDD equal to or less than 3.3 V and smaller than 1 V / 100 us for VDD equal to 5.5 V. Ramp VDD before VSS. In addition, all control pins should remain at 0 V (+/- 0.3 V) and no RF power should be applied while the power supplies ramp or while they return to zero.

Application Schematic

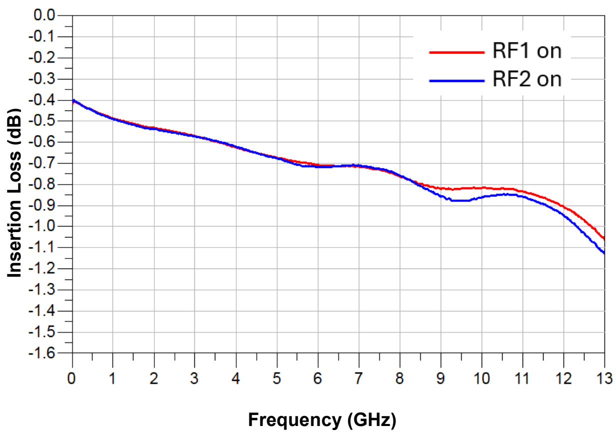


Parts List

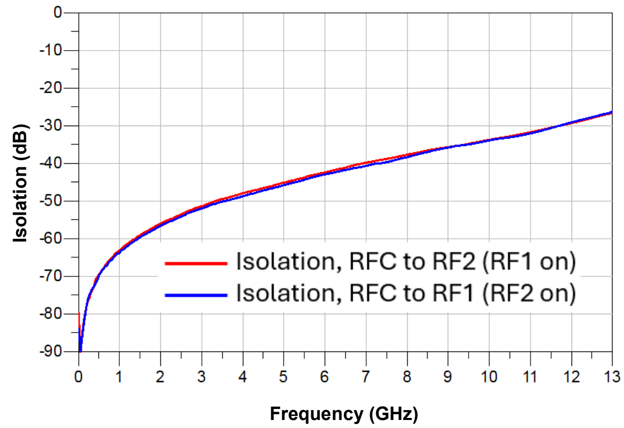
Part	Value	Case Style	Description
C1, C2	0.1 µF	0404	capacitor
J1-J3, J5, J6	Johnson End Launch Connector, 142-0761-871 (16 mil substrate)		
J4	Standard 2-array 6 pin SMT header		

Typical Performance Curves

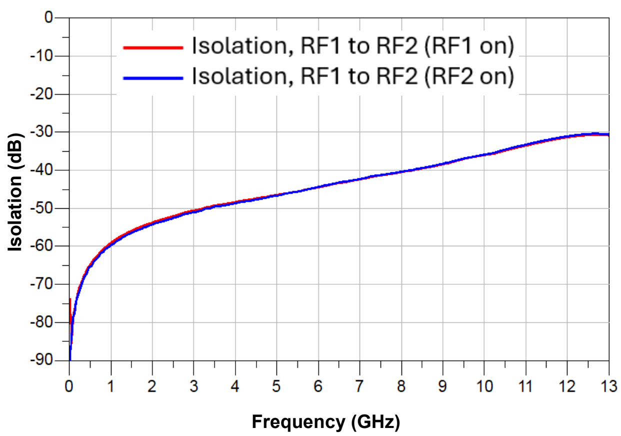
Insertion Loss (T=25°C)



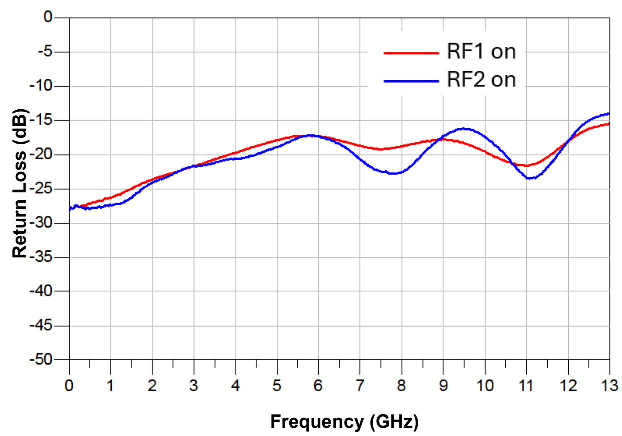
Isolation, RFC to RF1/2 (T=25°C)



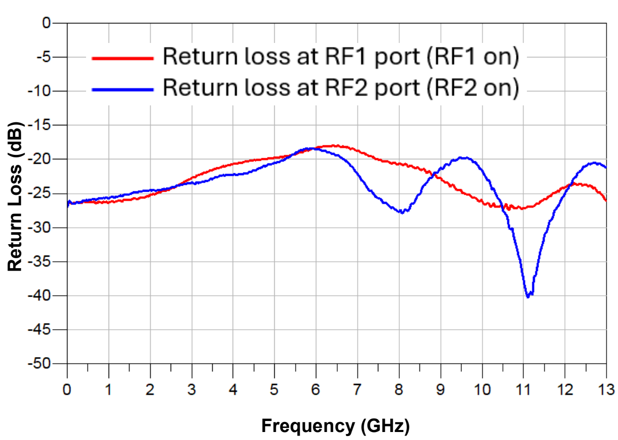
Isolation, RF1 to RF2 (T=25°C)



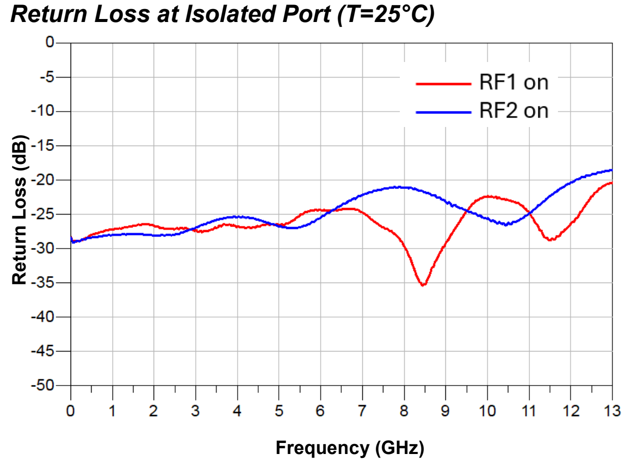
Return Loss, RFC (T=25°C)



Return Loss, RF1/2 (T=25°C)

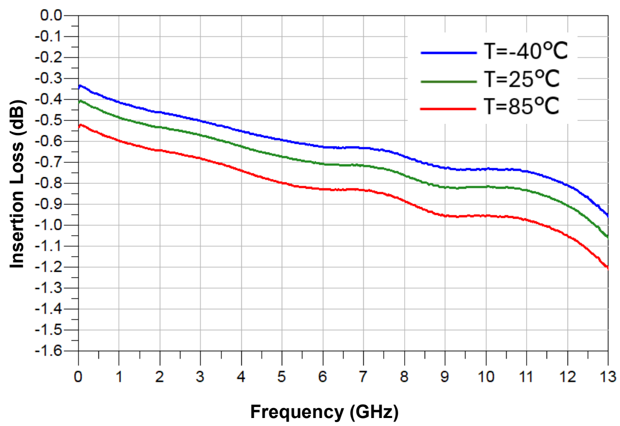


Return Loss at Isolated Port (T=25°C)

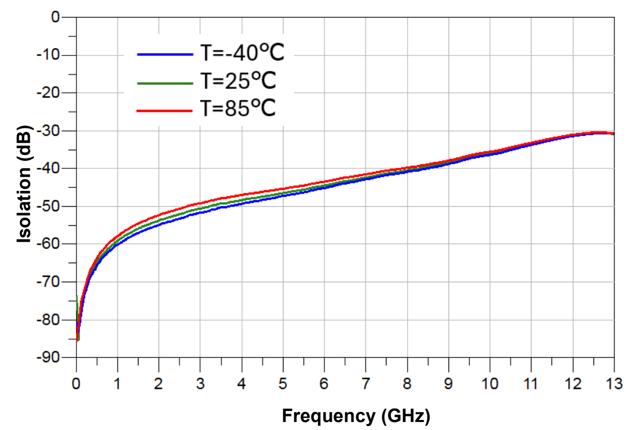


Typical Performance Curves

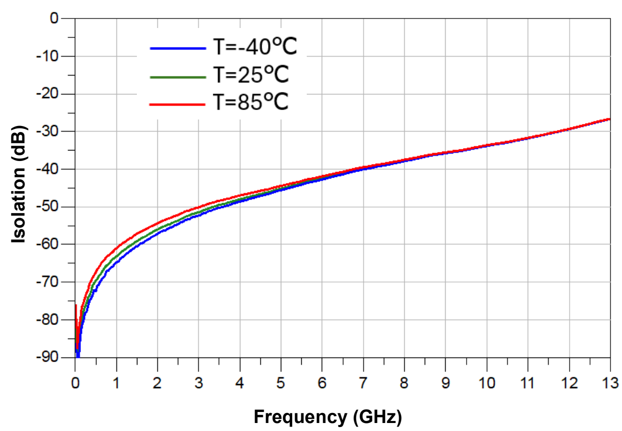
Insertion Loss vs Temperature (RF1 on)



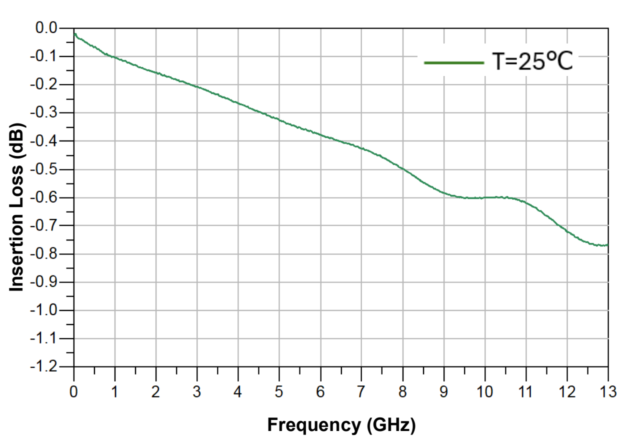
Isolation vs Temperature, RF1 to RF2 (RF1 on)



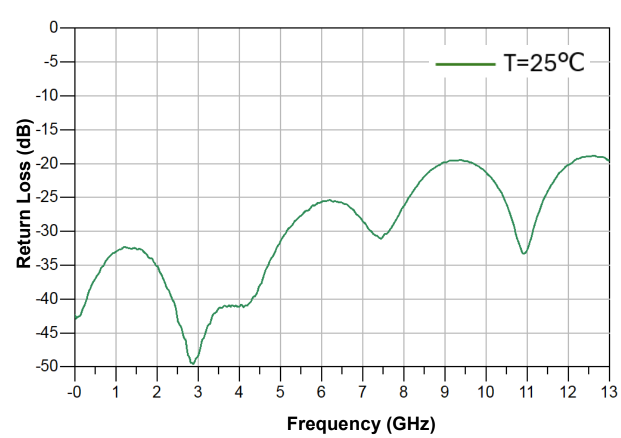
Isolation vs Temperature, RFC to RF2 (RF1 on)



Evaluation PCB losses

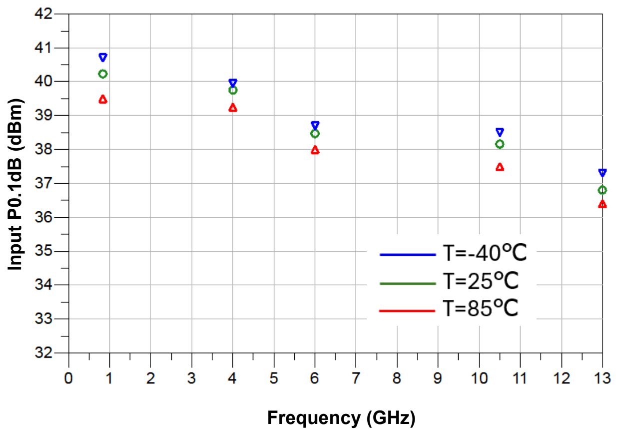


Evaluation PCB Return loss

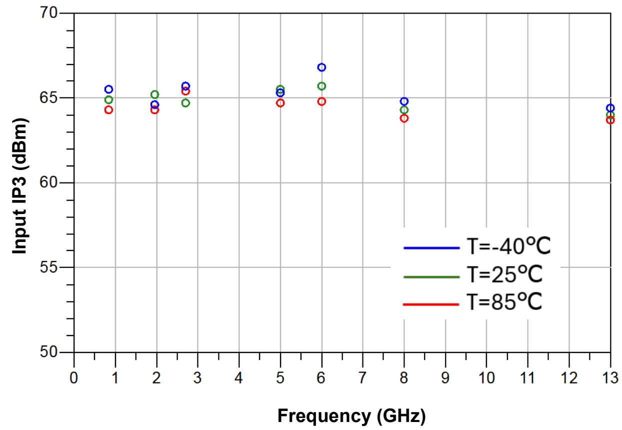


Typical Performance Curves

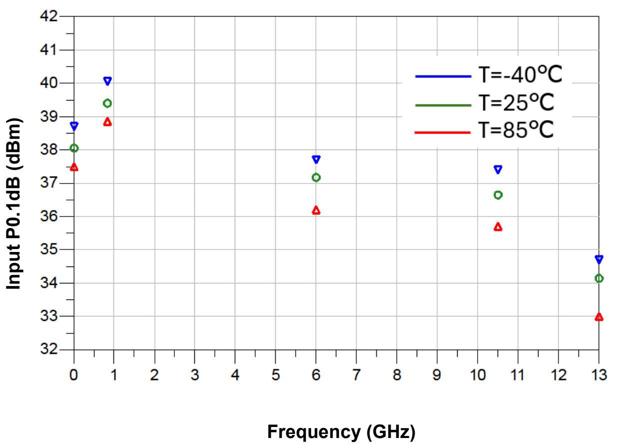
Input P0.1dB (Pulsed) vs Frequency over Temperature
Pulse width=1us, duty cycle=0.1%



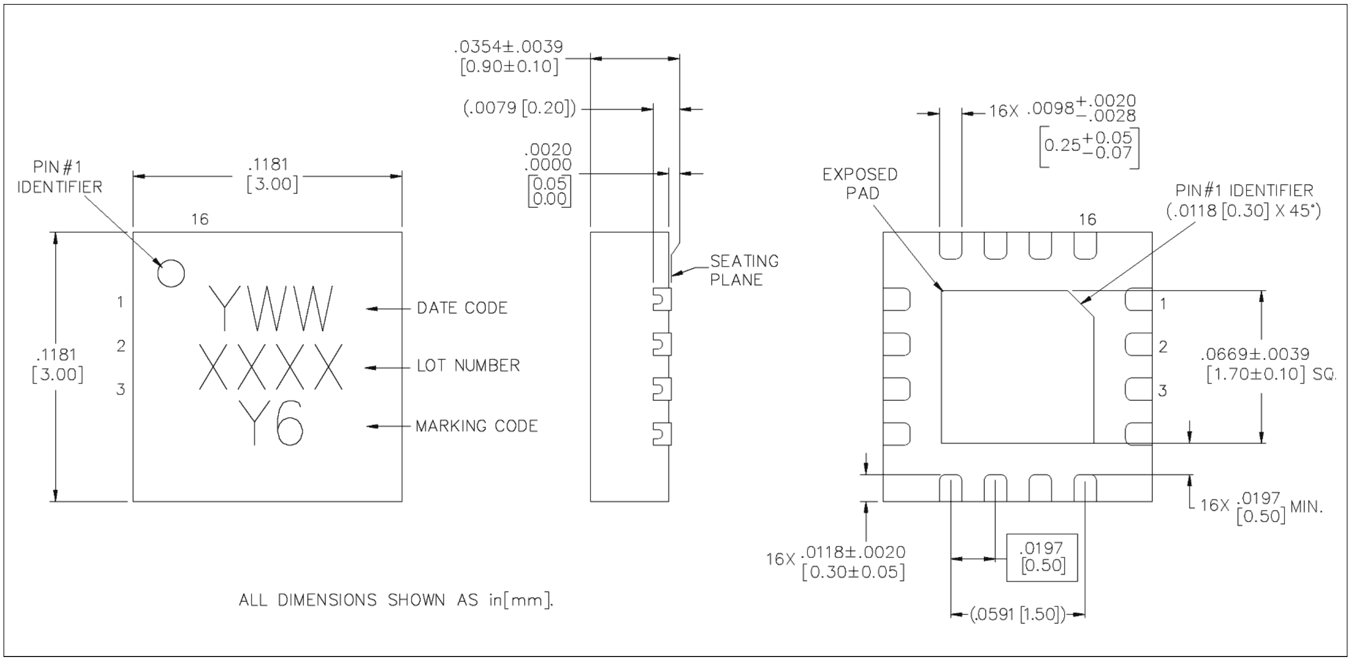
Input IP3 vs Frequency over Temperature



Input P0.1dB (CW) vs Frequency over Temperature



Lead-Free 3 mm 16-Lead PQFN†



† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.
Lead and pad finish: NiPdAu

Revision History

Rev	Date	Change Description
V1	9/01/25	Initial Production Release