SP4T Reflective Switch
7 kHz - 18 GHz

MASW-011222-DIE
Rev. V1

Features

- Insertion Loss: 1 dB
- Isolation: 60 dB
- Input P0.1dB: 33.5 dBm
- Input IP3: 65 dBm
- Return Loss at Each RF Port: 15 dB
- Power Handling: 31 dBm
- No Low Frequency Spurious
- Compatible with 1.8, 2.5, and 3.3 V CMOS Logic
- Cu-pillar bumped bare die
- RoHS* Compliant
- Die Size: 2380 x 1905 µm

Applications

- Aerospace and defense
- Test & Measurement
- ISM, Multi Market

Description

The MASW-011222-DIE is a reflective, ultra wideband single pole four throw (SP4T) switch with 1 dB of insertion loss at 10 GHz. The power handling capability is up to 31 dBm. The input and output return losses in the thru path are 15 dB typical. The logic levels are compatible with standard 1.8, 2.5, or 3.3 V CMOS.

The MASW-011222-DIE is designed for test and measurement and industrial, scientific, aerospace and defense applications.

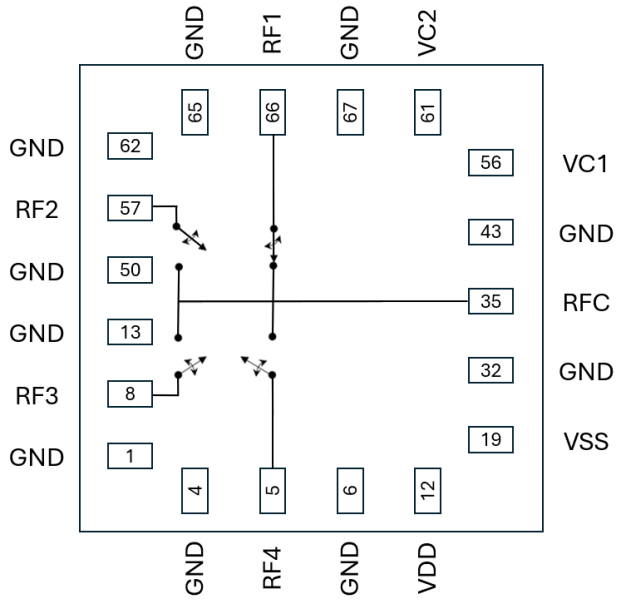
The MASW-011222-DIE is manufactured on a Silicon-on-Insulator process. The die comes with Copper pillars and it can be flipped and soldered to the appropriate substrate.

Ordering Information[1]

Part Number	Package
MASW-011222-DIE100	100 pc tape & reel
MASW-011222-DIE500	500 pc tape & reel

1. Reference Application Note M513 for reel size information.

Functional Schematic (bump up)



Pin Configuration[2]

Pin #	Label	Description
35	RFC[3]	RF Input/Output 1
66	RF1[3]	RF Input/Output 1
57	RF2[3]	RF Input/Output 2
8	RF3[3]	RF Input/Output 3
5	RF4[3]	RF Input/Output 4
56	VC1	Digital control voltage
61	VC2	Digital control voltage
12	V_{DD}	Positive supply voltage
19	V_{SS}	Negative supply voltage
7,28,49,68	AGND	Ground these pins
1-4,6,9-11,13-18, 20-27,29-34,36-48, 50-55,58-60,62-65,67	RF GND	Ground these pins

2. All the ground pillars must be connected to RF, DC, and thermal ground.
3. RF ports are DC-coupled to GND. There are no internal DC blocking capacitors.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Pin Description

Pin #	Name	Description
35	RFC	Common RF Input/Output
66	RF1	RF Input/Output 1
57	RF2	RF Input/Output 2
8	RF3	RF Input/Output 3
5	RF4	RF Input/Output 4
56	VC1	Digital Control voltage. Pulled down to GND with 100 kΩ resistor internally.
61	VC2	Digital Control voltage. Pulled down to GND with 100 kΩ resistor internally.
12	V_{DD}	Positive supply voltage. No special sequencing required.
19	V_{SS}	Negative supply voltage. No special sequencing required.
7,28,49,68	AGND	Ground these pins. Provide low thermal resistance to the Exposed Paddle center pad.
1-4,6,9-11,13-18, 20-27,29-34,36-48, 50-55,58-60,62-65,67	RF GND	Ground these pins. Provide low thermal resistance to the Exposed Paddle center pad.

RF Electrical Specifications[4,5]:
V_{DD} = +4 V, V_{SS} = -4 V, V_C1 / V_C2 = 0 V or 1.8 V, T_C[6] = 25°C, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Insertion Loss	2 GHz 10 GHz 18 GHz	dB	—	0.50 0.85 1.50	— 1.50 —
Isolation, Between RF1 / RF2 / RF3 / RF4	7 kHz - 18 GHz	dB	—	60	—
Isolation, RFC to RF1 / RF2 / RF3 / RF4	7 kHz - 18 GHz	dB	—	60	—
RFC Return Loss	7 kHz - 18 GHz	dB	—	15	—
RF1/RF2/RF3/RF4 Return Loss, Thru Port	7 kHz - 18 GHz	dB	—	15	—
Input P0.1dB	6 GHz - 15 GHz	dBm	—	33.5	—
Input IP3	1 GHz - 18 GHz Two tone, P_{IN} / tone = +15 dBm	dBm	—	65	—
T_{ON}	50% control to 90% RF	ns	—	85	—
T_{RISE}	10% to 90% RF	ns	—	20	—
T_{OFF}	50% control to 10% RF	ns	—	60	—
T_{FALL}	90% to 10% RF	ns	—	10	—

4. Parameters are measured on a laminate where the device is mounted on and de-embedded to the edge of the device.
5. Parameters in bold underline are tested in production.
6. Operating temperature is defined at the back of the die.

DC Electrical Specifications: V_{DD} = +4 V, V_{SS} = -4 V

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Voltage Supply, VDD	—	V	+3.15	+4.0	+4.15
Voltage Supply, VSS	—	V	-4.15	-4.0	-3.15
Logic Voltage, Input Low (V_{IL})	—	V	0.0	—	+0.8
Logic Voltage, Input High (V_{IH})	—	V	+1.2	—	V_{DD}
Supply Current, V_{DD}	—	mA	—	0.35	—
Supply Current, V_{SS}	—	mA	—	0.57	—
Logic Pin Current (VC1 / VC2)	Pulled down to GND with 100 kΩ resistor, 1.8 V on pin	µA	—	12	—

Recommended Operating Conditions

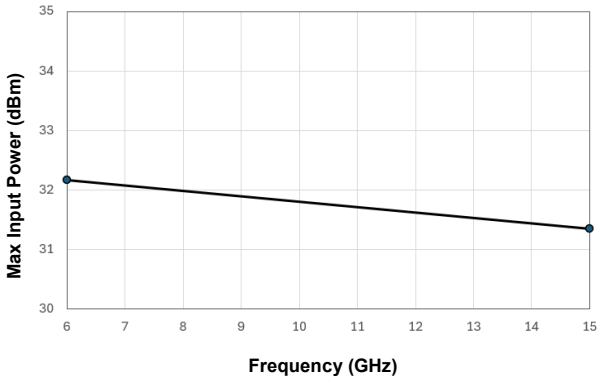
Parameter	Symbol	Unit	Min.	Typ.	Max.
Input Power @ RFC, RF1 - RF4 @ T_C = 85°C, 6 GHz	P_{IN}	dBm	—	—	31
Junction Temperature	T_J	°C	-40	—	125
Operating Temperature[6]	T_C	°C	-40	—	85
Positive DC Supply	V_{DD}	V	3.15	—	4.15
Negative DC Supply	V_{SS}	V	-4.15	—	-3.15
Logic Control Voltage	V1, V2	V	-0.3	—	VDD

Absolute Maximum Ratings[7,8]

Parameter	Symbol	Unit	Min.	Max.
Input Power @ RFC, RF1 - RF4 @ T_C = 85°C, 6 GHz	P_{IN}	dBm	—	32
Positive DC Supply	V_{DD}	V	—	4.4
Negative DC Supply	V_{SS}	V	-4.4	—
Junction Temperature	T_J	°C	—	135
Storage Temperature	T_{STG}	°C	-65	125
Logic Control Voltage	V1, V2	V	-0.3	4.5

7. Exceeding any one or combination of these limits may cause permanent damage to this device.
8. MACOM does not recommend sustained operation near these survivability limits.

Max Input Power



Truth Table

Control 1	Control 2	Condition of Switch			
VC1	VC2	RF1	RF2	RF3	RF4
V_{IL}	V_{IL}	On	Off	Off	Off
V_{IH}	V_{IL}	Off	On	Off	Off
V_{IL}	V_{IH}	Off	Off	On	Off
V_{IH}	V_{IH}	Off	Off	Off	On

Handling Procedures

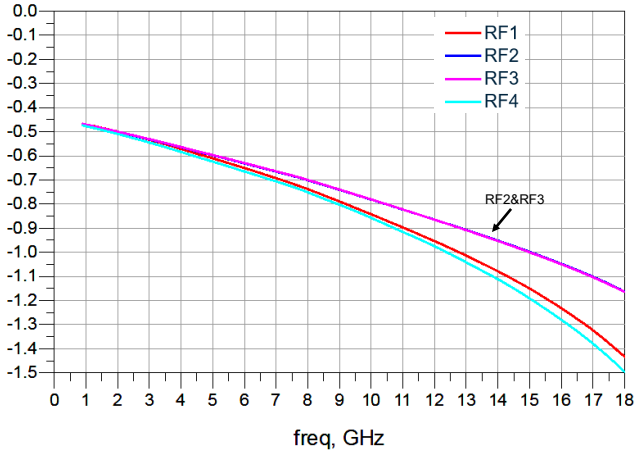
Please observe the following precautions to avoid damage:

Static Sensitivity

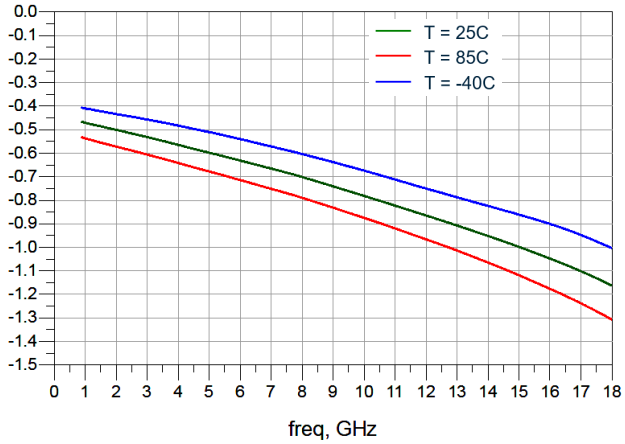
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Typical Performance Curves

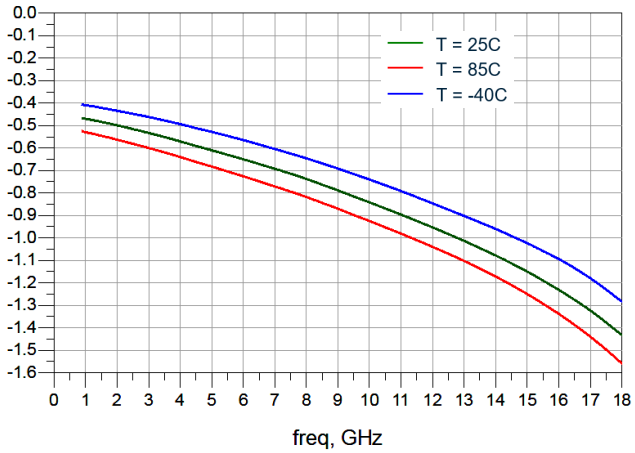
Insertion Loss (T = 25C°)



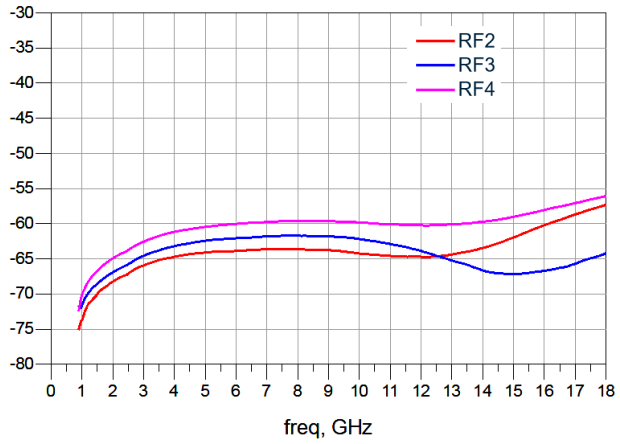
Insertion Loss vs Temp (RF2 on)



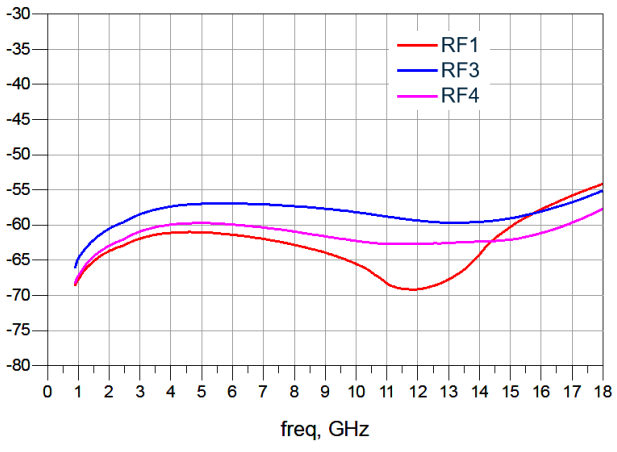
Insertion Loss vs Temp (RF1 on)



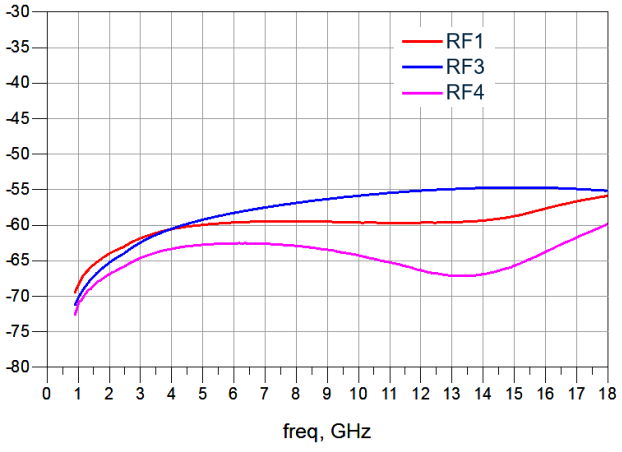
Isolation, RFC to RF2/3/4 (RF1 on, T = 25°C)



Isolation, RFC to RF1 / 3 / 4 (RF2 on, T = 25°C)

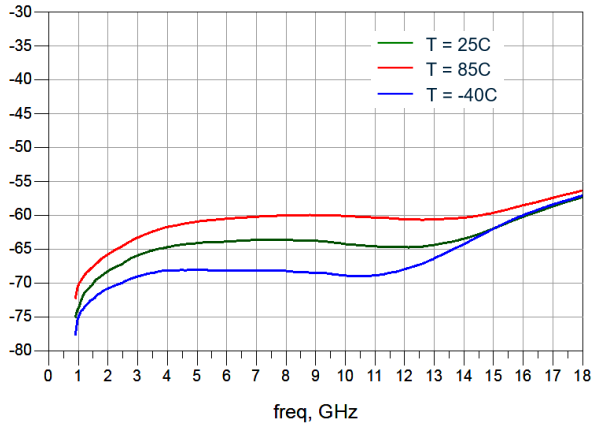


Isolation, RF2 to RF 1 / 3 / 4 (RF2 on, T = 25°C)

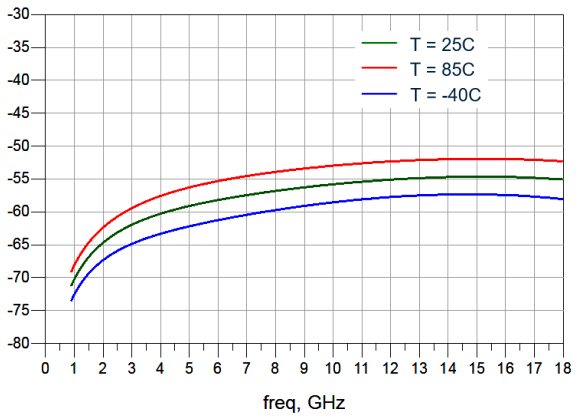


Typical Performance Curves

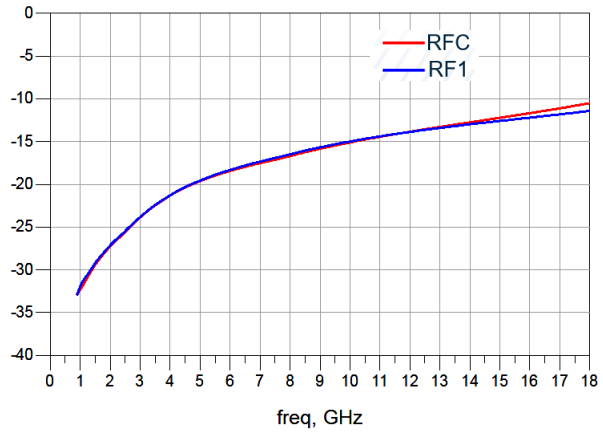
Isolation vs Temp, RFC to RF2 (RF1 on)



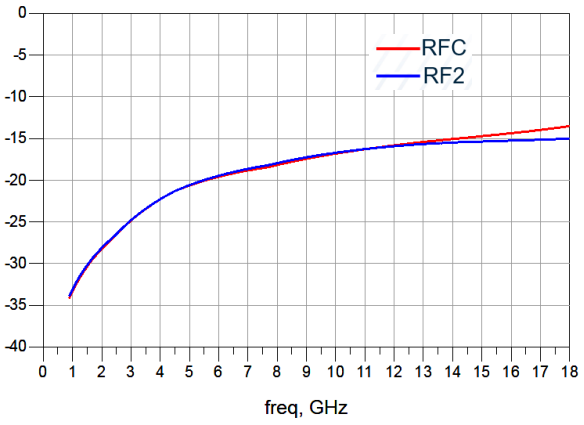
Isolation vs Temp, RF2 to RF3 (RF2 on)



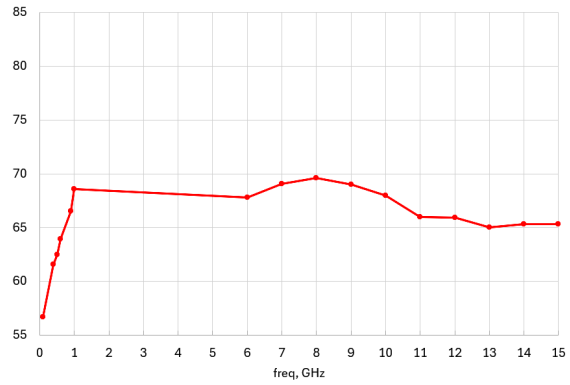
Return Loss, RF1 and RFC (RF1 on, T = 25°C)



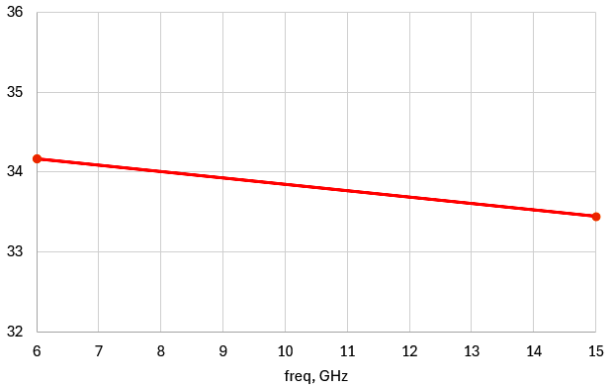
Return Loss, RF2 and RFC (RF2 on, T = 25°C)



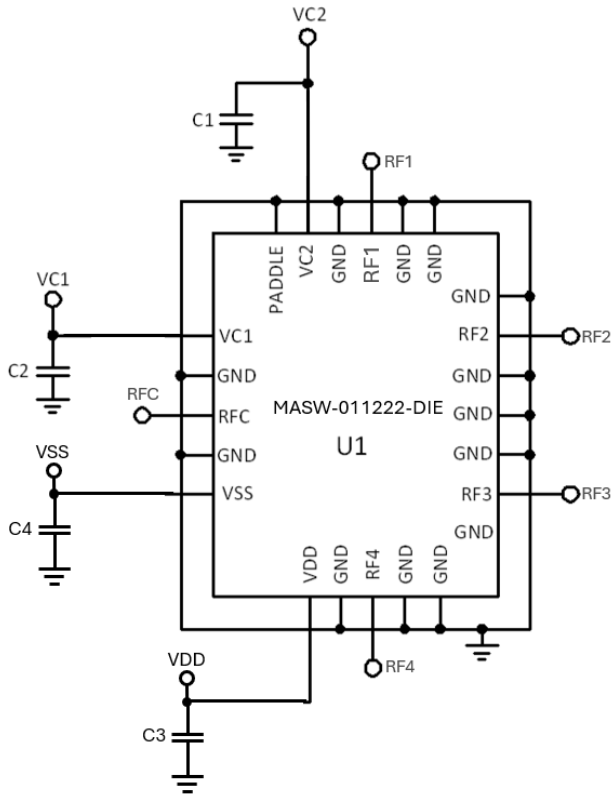
Input IP3 @ 25°C (dBm)



Input P0.1dB (dBm)



Application Schematic



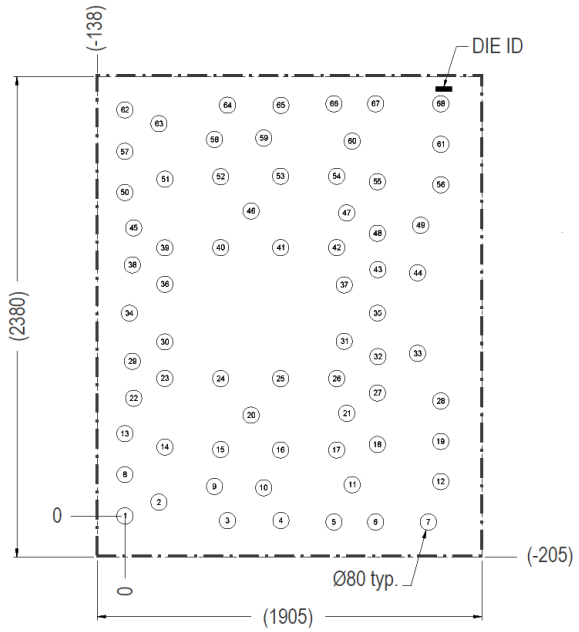
Supply and I/O Sequencing

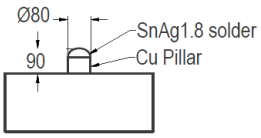
All logic pins should be set to 0 V before ramping up or down the supply voltages. V_{DD} and V_{SS} can ramp in any order.

Parts List

Part	Value	Case Style
U1	MASW-011222-DIE	Bumped Die
C1, C2	Capacitor, 5 pF, 16 V	0402
C3, C4	Capacitor, 0.01 µF, 50 V	0402

Chip Outline Drawing[9,10,11,12]





Pin #	Pin Name
35	RFC
66	RF1
57	RF2
8	RF3
5	RF4
56	V1
61	V2
12	VDD
19	VSS
7,28,49,68	AGND
1-4,6,9-11,13-18, 20-27,29-34,36-48, 50-55,58-60,62-65,67	RF GND

9. Unless otherwise specified, all dimensions shown are µm with a tolerance of ±5 µm.
10. Die thickness is 203 ±10 µm.
11. Die size reflects final dimensions.
12. Copper pillar with SnAa1.8 solder plate shall be 90 µm max. protrusion.

Bump Location (X, Y)

BUMP	X	Y	BUMP	X	Y	BUMP	X	Y	BUMP	X	Y
1	0	0	18	1249.865	354.745	35	1250.2	1004.81	52	475.185	1679.62
2	168.35	67.945	19	1565	369.81	36	197.64	1148.185	53	771.405	1682.035
3	508.85	-23.38	20	625.57	499.55	37	1085.905	1144.87	54	1048.645	1682.035
4	773.045	-22.415	21	1098.15	508.985	38	36.65	1243.835	55	1249.865	1654.875
5	1035	-30.19	22	43.435	583.06	39	197.225	1328.325	56	1565	1639.81
6	1240.975	-30.19	23	197.225	681.295	40	475.24	1329.24	57	0	1804.81
7	1503.635	-30.19	24	475.24	680.38	41	771.405	1329.24	58	444.875	1863.78
8	0	204.81	25	771.405	680.38	42	1048.645	1329.24	59	688.11	1870.665
9	444.875	145.84	26	1048.645	680.38	43	1252.29	1220.61	60	1125.065	1855.46
10	688.11	138.955	27	1249.865	609.435	44	1450.2	1204.81	61	1565	1839.81
11	1125.065	154.16	28	1565	569.81	45	43.435	1426.56	62	0	2009.62
12	1565	169.81	29	36.65	765.785	46	625.57	1510.07	63	168.35	1941.675
13	-0.11	408.175	30	197.64	861.435	47	1098.15	1500.635	64	508.85	2033
14	197.945	342.31	31	1085.905	864.75	48	1249.865	1400.185	65	773.045	2032.035
15	475.185	330	32	1252.29	789.01	49	1465	1439.81	66	1035	2039.81
16	771.405	327.585	33	1450.2	804.81	50	-0.11	1601.445	67	1240.975	2039.81
17	1048.645	327.585	34	22.485	1004.815	51	197.945	1667.31	68	1565	2039.81

Revision History

Rev.	Date	Change Description
V1	Sep 2025	Final release