

## GaAs WLAN Dual SPDT Switch 2.4 - 5.8 GHz

Rev. V3

### Features

- 802.11a & b/g, UNII, and Hiperlan Applications
- Optimized for 2.4 - 5.8 GHz WLAN
- Low Insertion Loss:
  - 0.85 dB @ 2.4 GHz
  - 1.1 dB @ 5.8 GHz
- High Isolation: 28 dB Typical
- Low Harmonics: <-63 dBc @ 20 dBm
- RoHS\* Compliant

### Description

The MASW-008206-000DIE is a WLAN GaAs pHEMT MMIC Dual SPDT switch. One SPDT (RF2) is optimized for 2.4 GHz WLAN and the other (RF5) is optimized for 5.8 GHz WLAN applications. Typical applications are for 802.11a and 802.11b/g PC card and access point applications.

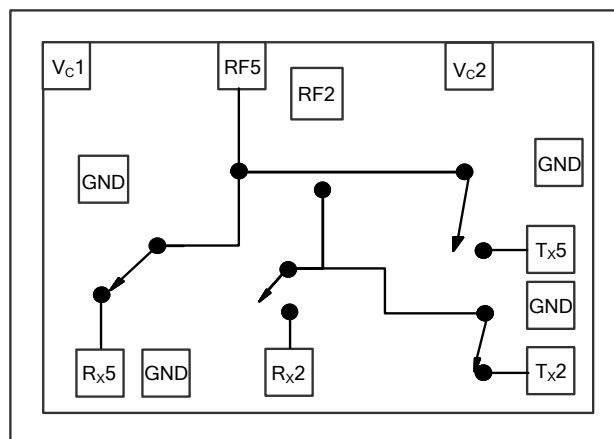
The MASW-008206-000DIE delivers high isolation, low insertion loss, and high linearity up to 5.8 GHz. This device is fabricated using a 0.5 micron gate length GaAs pHEMT process. The process features full passivation for performance and reliability.

### Ordering Information <sup>1</sup>

Part Number	Package
MASW-008206-000DIE	Separated Die on Grip Ring

1. Die quantity varies.

### Die Bond Pad Layout



### Die Bond Pad Configuration

Pad No.	Name	Description
1	V <sub>c</sub> 1	Voltage Control 1
2	GND	Ground
3	R <sub>x</sub> 5	5 GHz R <sub>x</sub> Port
4	GND	Ground
5	R <sub>x</sub> 2	2.4 GHz R <sub>x</sub> Port
6	T <sub>x</sub> 2	2.4 GHz T <sub>x</sub> Port
7	GND	Ground
8	T <sub>x</sub> 5	5 GHz T <sub>x</sub> Port
9	GND	Ground
10	V <sub>c</sub> 2	Voltage Control 2
11	RF2	2.4 GHz Antenna Port
12	RF5	5 GHz Antenna Port

\* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

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### Electrical Specifications<sup>2,3</sup>: $T_A = 25^\circ\text{C}$ , $Z_0 = 50\ \Omega$ , $V_C = 0\text{V} / 3\text{V}$ , $P_{IN} = 0\ \text{dBm}$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Insertion Loss	RF2 to Tx2/Rx2, 2.4 GHz RF5 to Tx5/Rx5, 5.0 GHz	dB	—	0.85 1.1	1.0 1.2
Isolation	RF2 to Tx2/Rx2, 2.4 GHz RF5 to Tx5/Rx5, 5.0 GHz	dB	25.5 21.0	30.0 25.0	— —
Return Loss	DC - 6.0 GHz	dB	—	15	—
IP3	20 dBm Total Power, 1 MHz Spacing RF2 to Tx2/Rx2, 2.4 GHz RF5 to Tx5/Rx5, 4.9 GHz	dBm	— —	54 55	— —
Input P1dB	RF2 to Tx2, 2.4-2.5 GHz RF5 to Tx5, 4.9-5.9 GHz	dBm	— —	28 28	— —
Harmonics	RF2 to Tx2, 2.4-2.5 GHz, 20 dBc RF5 to Tx5, 4.9-5.9 GHz, 20 dBc	dBc	— —	-63 -67	— —
Control Current	$ V_C  = 3\ \text{V}$	$\mu\text{A}$	—	<1	10.0
$T_{RISE} / T_{FALL}$	10% - 90% RF, 90% - 10% RF	ns	—	22	—
$T_{ON} / T_{OFF}$	50% Control - 90% RF, 50% Control - 10% RF	ns	—	30	—

2. External blocking capacitors on all RF ports.
3. Electrical min/max are guaranteed in die form only.

### Absolute Maximum Ratings<sup>4,5</sup>

Parameter	Absolute Maximum
Input Power @ 3 V Control @ 5 V Control	+32 dBm +33 dBm
Operating Voltage	+8 volts
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

4. Exceeding any one or combination of these limits may cause permanent damage to this device.
5. M/A-COM Technology Solutions does not recommend sustained operation near these survivability limits.

### Qualification

Qualified to M/A-COM specification REL-201, Process Flow -2.

### Truth Table<sup>6,7,8</sup>

Control $V_{C1}$	Control $V_{C2}$	RF2 - Tx2 RF5 - Rx5	RF2 - Rx2 RF5 - Tx5
1	0	On	Off
0	1	Off	On

6. For positive voltage control, external DC blocking capacitors are required on all RF ports.
7. Differential voltage, V (state 1) - V (state 0), must be +2.7 V minimum and must not exceed +5 V.
8. 0 =  $0 \pm 0.3\ \text{V}$ , 1 = +2.7 V to +5 V.

### Handling Procedures

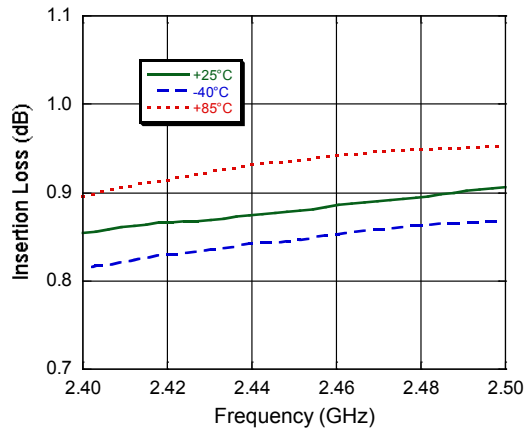
Please observe the following precautions to avoid damage:

### Static Sensitivity

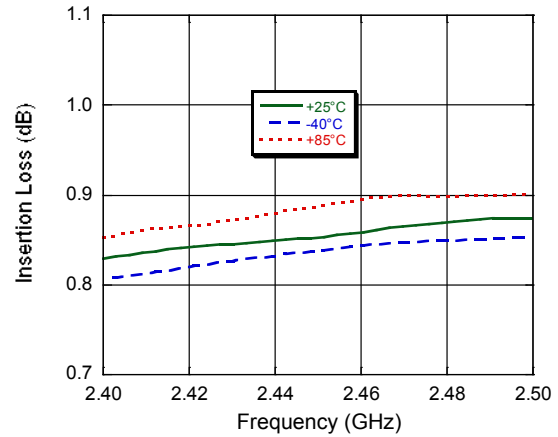
Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Class Zero (100 V) devices.

**Typical Performance Curves: 2.4-2.5 GHz (plots = chip on board assembly)**

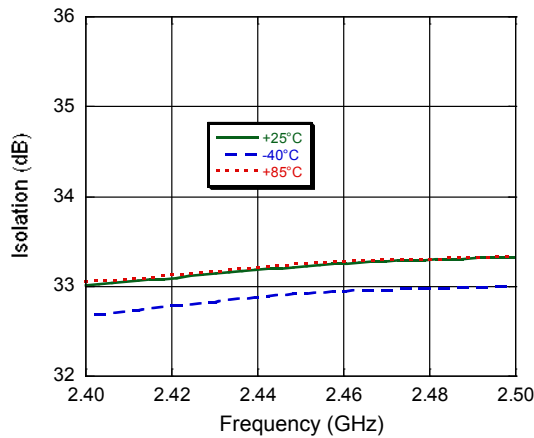
**$T_X$  Insertion Loss**



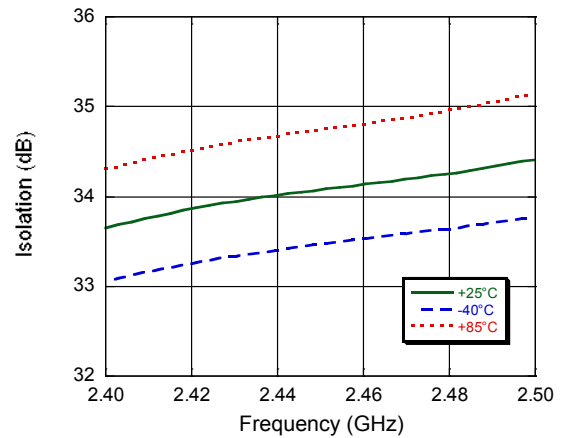
**$R_X$  Insertion Loss**



**$T_X$  Isolation**

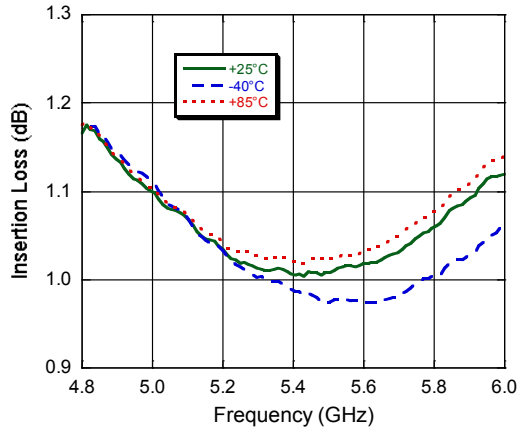


**$R_X$  Isolation**

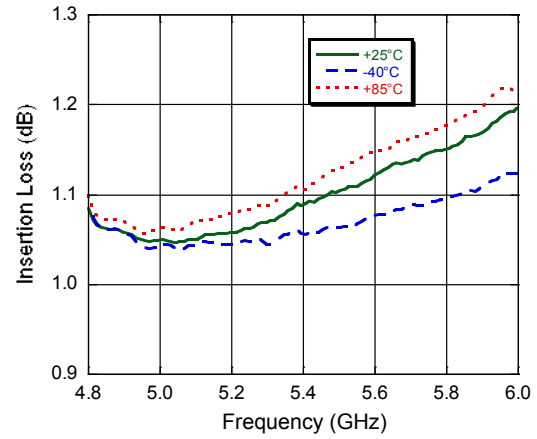


## Typical Performance Curves: 4.8-6.0 GHz (plots = chip on board assembly)

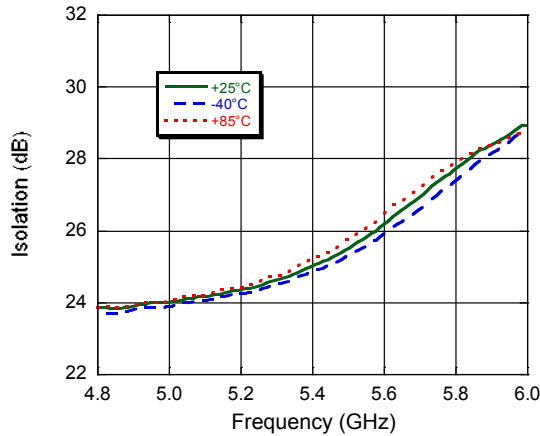
**$T_x$  Insertion Loss**



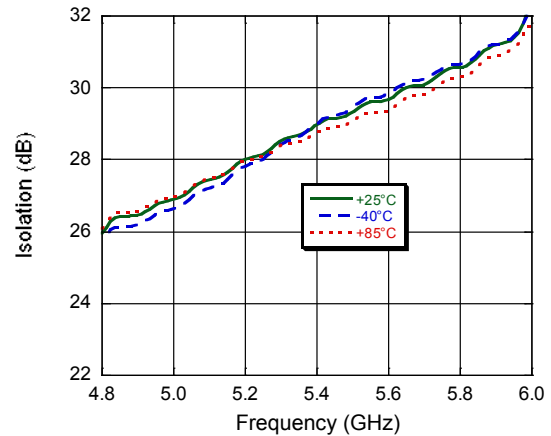
**$R_x$  Insertion Loss**



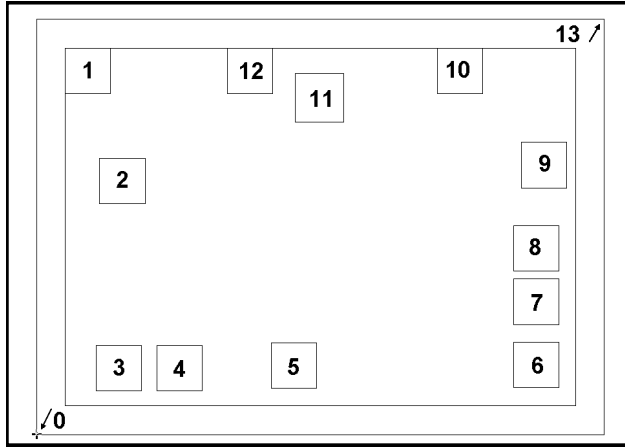
**$T_x$  Isolation**



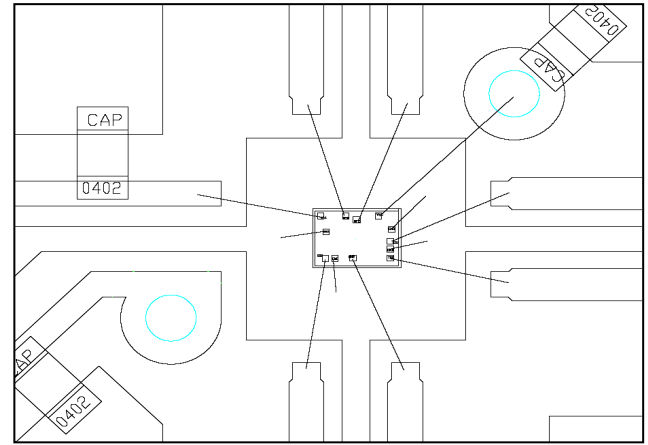
**$R_x$  Isolation**



## Outline Drawing



## Chip mounted to PWB for testing purposes



## Pad Configuration <sup>9</sup>

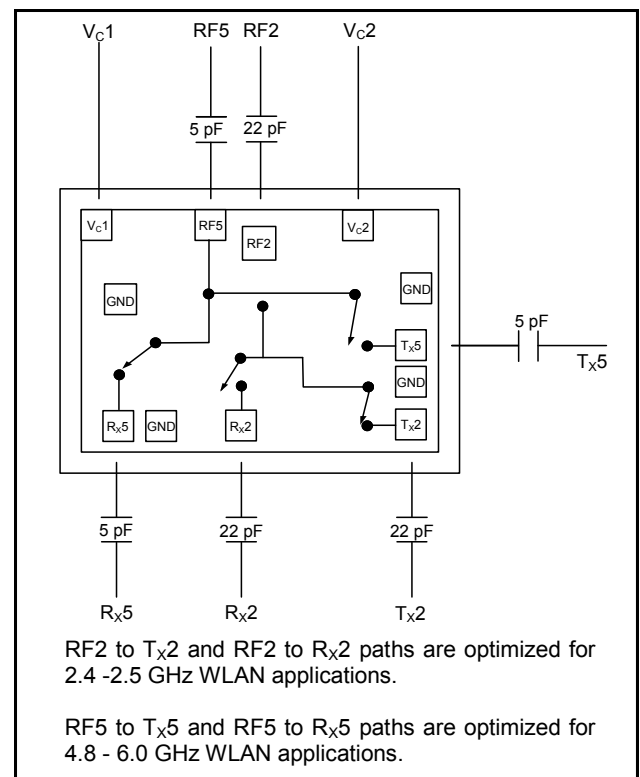
**Die Size: 890 x 650  $\mu\text{m}$  (nominal)**

**Die Thickness: 6 mils (nominal)**

Pad No.	X ( $\mu\text{m}$ ) nominal	Y ( $\mu\text{m}$ ) nominal	Pad Size ( $\mu\text{m}$ )
0	0	0	Lower left edge of die
1	80.5	569.5	71 x 71
2	134.5	397	71 x 71
3	129	104	71 x 71
4	224	104	71 x 71
5	403.75	108	71 x 71
6	783.5	109	71 x 71
7	783.5	208	71 x 71
8	783.5	292	71 x  71
9	795.25	421.75	71 x 71
10	664	569.5	71 x 71
11	443	527	76 x 76
12	334.75	569.5	71 x 71
13	890	650	Upper right edge of die

9. All X,Y dimensions are at bond pad center.

## Application Schematic



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