

MAPC-A3009-AB

Rev. V1

MACOM PURE CARBIDE

Features

- Saturated Power: 60 W
- Drain Efficiency: 67%
- Small Signal Gain: 16 dB
- Lead-Free Air Cavity Ceramic Package
- RoHS* Compliant

Applications

- Avionics TACAN, DME, IFF
- Military Radio
- L, S-band Radar
- Electronic Warfare
- ISM
- General Amplification

Description

The MAPC-A3009-AB is a 60 W packaged, unmatched transistor utilizing a high performance, 0.15 μ m GaN on SiC production process. This transistor supports both defense and commercial related applications.

Offered in a thermally-enhanced flange package, the MAPC-A3009-AB provides superior performance under CW operation allowing customers to improve SWaP-C benchmarks in their next generation systems.

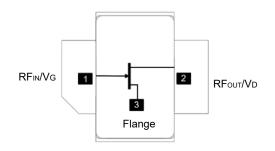
Typical RF Performance:

• Measured @ CW = P_{SAT} , defined at I_{GS} = 1.44 mA V_{DS} = 28 V, I_{DQ} = 400 mA, T_C = 25°C

Frequency (GHz)	Output Power Gain (dBm) (dB)		h₀ (%)
2.3	48.74	13.4	56.7
2.5	48.60	14.2	69.2
2.7	47.58	13.6	70



Functional Schematic



Pin Configuration

Pin #	Pin Name	Function		
1	RF_{IN} / V_G	RF Input / Gate		
2	RF _{OUT} / V _D	RF Output / Drain		
3	Flange ¹	Ground / Source		

1. The flange on the package bottom must be connected to RF, DC and thermal ground.

Ordering Information

Part Number	MOQ Increment
MAPC-A3009-AB	Bulk
MAPC-A3009-ABSB1	Sample Board

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

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RF Electrical Specifications²: Frequency = 2.5 GHz, P_{SAT} @ I_{GS} = 1.44 mA, T_A = +25°C, V_{DS} = 28 V, I_{DQ} = 400 mA, Low Power Gain tested at Input Power of 10 dBm

Low Power Gain tested at input Power of 10 dBin.					
Parameter	Conditions Units Min. Ty		Typ. Max.		
Saturated Power (P _{SAT})	_	W	60.7	69	_
Drain Efficiency (η_{SAT})	—	%	67.3	72	—
Low Power Gain (G _{ss})	P _{IN} = 10 dBm, CW	dB	16	17.3	_

2. Final testing and screening for all transistor sales is performed using the MAPC-A3009-AB-AMP at 2.5 GHz.

Absolute Maximum Ratings^{3,4}

Parameter	Absolute Maximum
Drain-Source Voltage	84 V
Gate Voltage	-10, +2 V
Drain Current	6 A
Gate Current	15 mA
Input Power	35 dBm
Storage Temperature	-55C to +150°C
Mounting Temperature	+245°C
Junction Temperature ^{5,6}	+225°C
Operating Temperature	-40°C to +85°C

3. Exceeding any one or combination of these limits may cause permanent damage to this device.

MACOM does not recommend sustained operation near these survivability limits.

5. Operating at nominal conditions with T_J \leq +225 C will ensure MTTF > 1 x 10⁶ hours.

6. Junction Temperature $(T_J) = T_C + \Theta jc * (V * I)$ Typical thermal resistance $(\Theta jc) = 2.8 \text{ °C/W}$ for CW. a) For $T_C = +25 \text{ °C}$,

T_J = 122 °C @ P_{DISS} = 34.6 W

b) For T_C = +85°C,

2

T_J = 185 °C @ P_{DISS} = 36.0 W

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

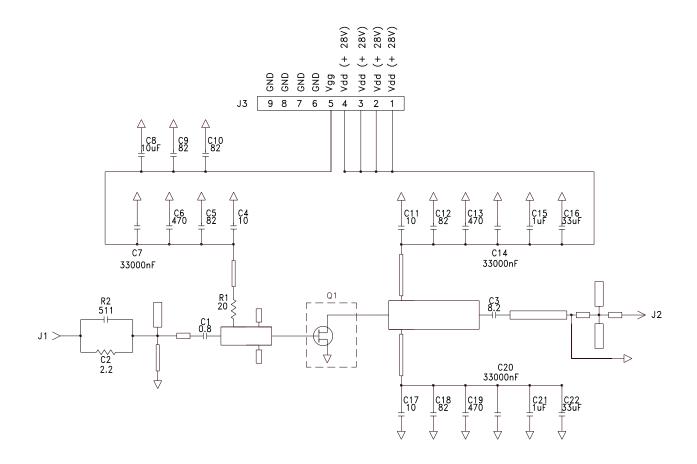
GaN on SiC Transistor, 60 W, 28 V DC - 4 GHz



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MAPC-A3009-AB Rev. V1

Evaluation Test Fixture and Recommended Tuning Solution, 2.3 - 2.7 GHz



Description

Parts measured on evaluation board (20-mil thick RO4350). Matching is provided using a combination of lumped elements and transmission lines as shown in the simplified schematic above. Recommended tuning solution component placement, transmission lines, and details are shown on the next page.

Biasing Sequence

Bias ON

- 1. Ensure RF is turned off
- 2. Apply pinch-off voltage of -5 V to the gate
- 3. Apply nominal drain voltage
- 4. Bias gate to desired quiescent drain current
- 5. Apply RF

Bias OFF

- 1. Turn RF off
- 2. Apply pinch-off voltage of -5 V to the gate
- 3. Turn-off drain voltage
- 4. Turn-off gate voltage

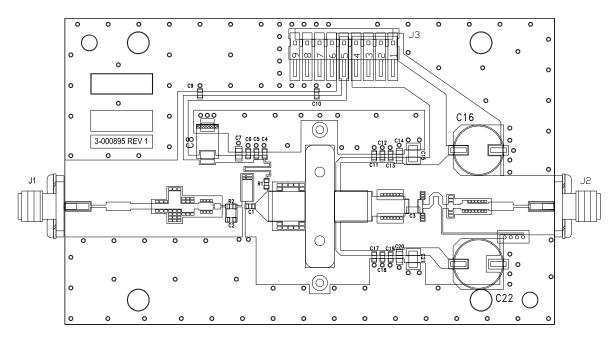
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Evaluation Test Fixture and Recommended Tuning Solution, 2.3 - 2.7 GHz



Assembly Parts List

Reference Designator	Reference Designator Description	
C1	Cap, 0.8 pF, ±0.1pF, 0603, ATC	1
C2	Cap, 2.2 pF, ±0.1pF, 0603, ATC	1
C3 ⁷	Cap, 8.2 pF, ±5%, ATC800B	1
C4, C11, C17	Cap, 10 pF, ±5%, 0603, ATC	3
C5, C9, C10, C12, C18	Cap, 82 pF, ±5%, 0603, ATC	5
C6, C13, C19	Cap, 470 pF, ±5%, 100V, 0603, X7R, RoHS Compliant	3
C7, C14, C20	Cap, 33000 pF, 10%, 0805, 100V, X7R	3
C8	Cap, 10 µF, 16V, Tantalum, 2312	1
C15, C21	Cap, 1 µF, ±10%, 100V, X7R, 1210	2
C16, C22	Cap, 33 µF, ±20%, G Case	2
R1	Res, 20 Ω , ±1%, 0603, IMS NDX0603WA	1
R2	Res, 511 Ω, ±1%, 0603, 1/16W	1
J1, J2	SMA Connector, Panel Jack, Post Contact, DC-18GHz, 50Ω, 0.05in	2
J3	Header, 9POS, 0.1in Pitch, 105°C, 250V	1
-	PCB, RO4350B, Er = 3.48, h = 20 mil	1
Q1	MAPC-A3009-AB	1

7. Component C3 is mounted vertically.

⁴

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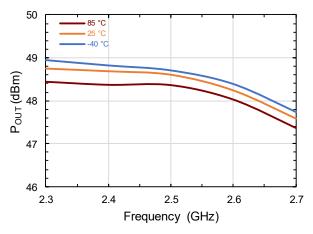
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Typical Performance Curves as Measured in the 2.3-2.7 GHz Evaluation Test Fixture

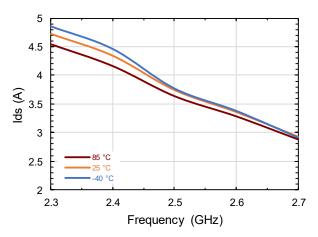
CW, P_{SAT} measurements @ I_{gs} = 1.44 mA, V_{DS} = 28 V, I_{DQ} = 400 mA.

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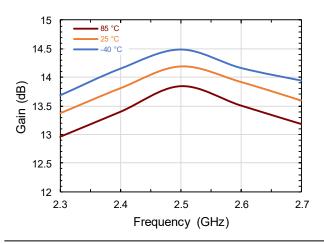
Output Power vs. Temperature and Frequency



Drain Current vs. Temperature and Frequency



Large Signal Gain vs. Temperature and Frequency

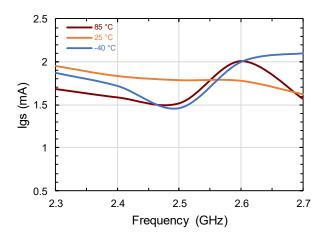




80 85 °C 75 -40 Drain Efficiency (%) 70 65 60 55 50 2.4 2.5 2.6 2.7 2.3 Frequency (GHz)

Drain Efficiency vs. Temperature and Frequency

Gate Current vs. Temperature and Frequency





MAPC-A3009-AB

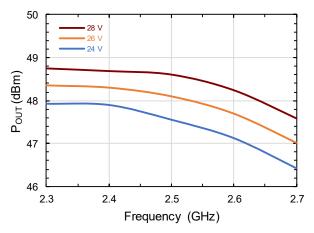
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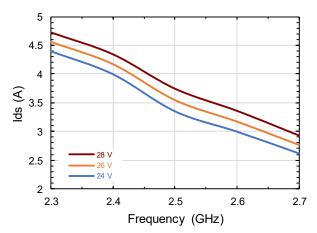
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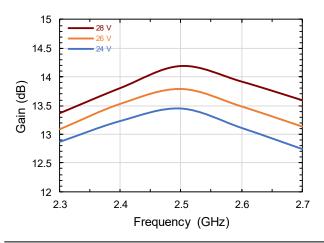
Output Power vs. V_{DS} and Frequency



Drain Current vs. V_{DS} and Frequency

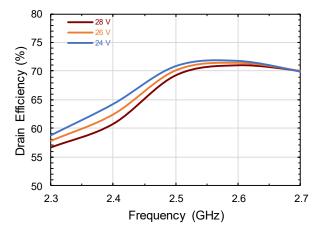


Large Signal Gain vs. V_{DS} and Frequency

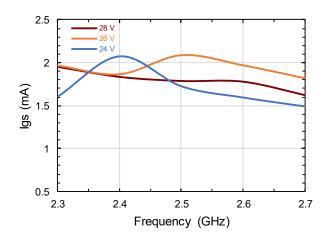


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Drain Efficiency vs. V_{DS} and Frequency



Gate Current vs. V_{DS} and Frequency





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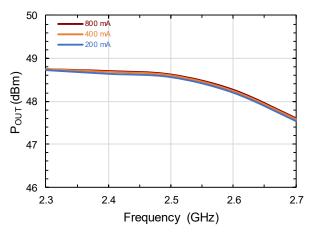
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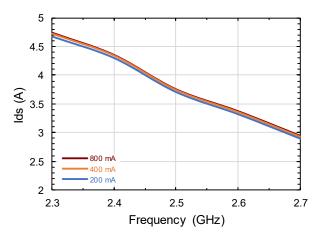
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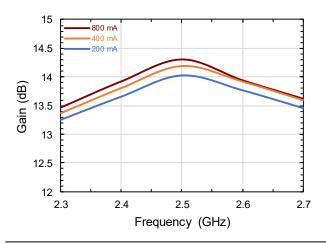
Output Power vs. IDQ and Frequency



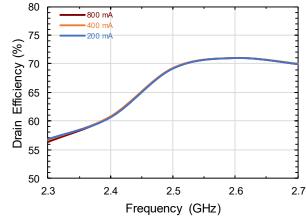
Drain Current vs. I_{DQ} and Frequency



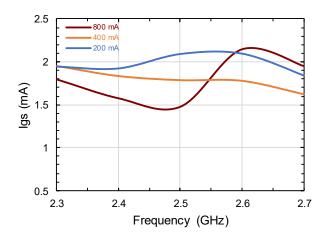
Large Signal Gain vs. IDQ and Frequency



Drain Efficiency vs. I_{DQ} and Frequency



Gate Current vs. I_{DQ} and Frequency



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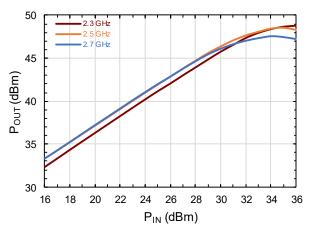
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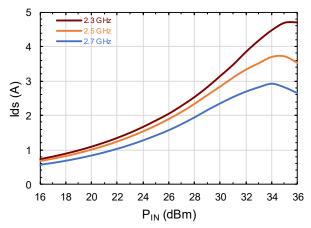
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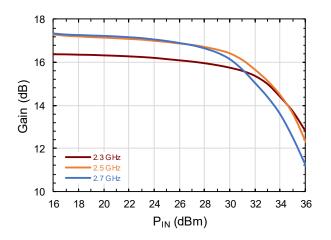
Output Power vs. Frequency and PIN



Drain Current vs. Frequency and P_{IN}

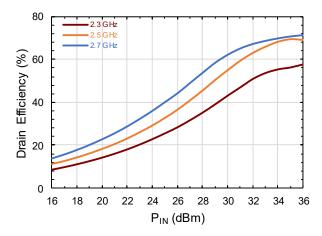


Large Signal Gain vs. Frequency and PIN

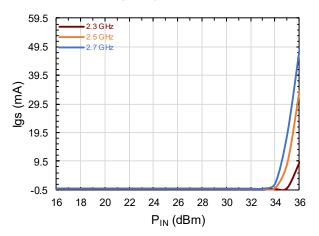


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Drain Efficiency vs. Frequency and PIN



Gate Current vs. Frequency and PIN





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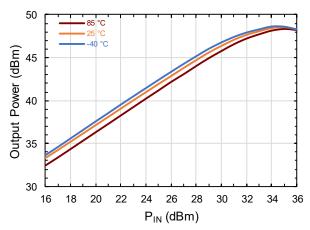
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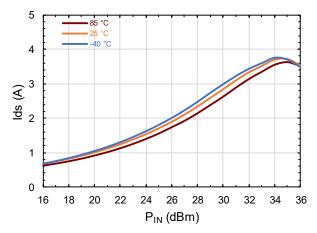
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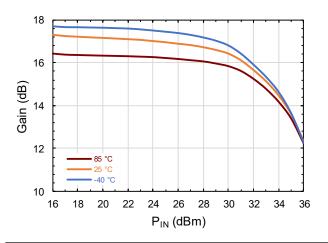
Output Power vs. Temperature and PIN



Drain Current vs. Temperature and P_{IN}

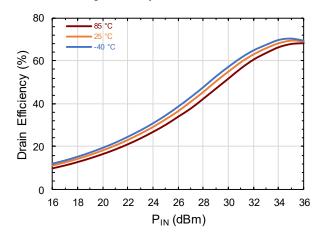


Large Signal Gain vs. Temperature and PIN

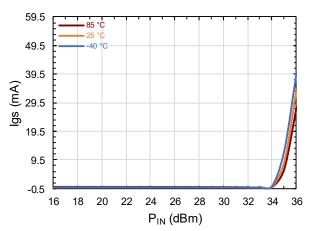


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Drain Efficiency vs. Temperature and P_{IN}



Gate Current vs. Temperature and PIN



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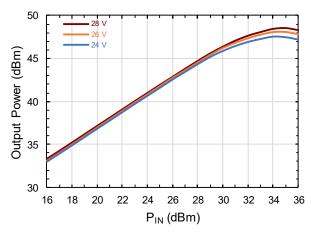
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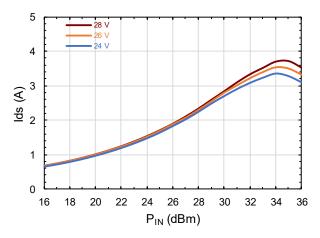
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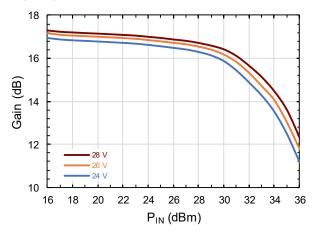
Output Power vs. V_{DS} and P_{IN}



Drain Current vs. V_{DS} and P_{IN}

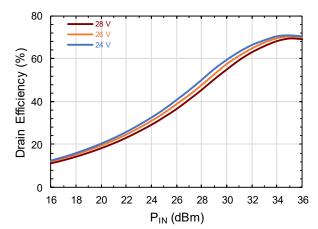


Large Signal Gain vs. V_{DS} and P_{IN}

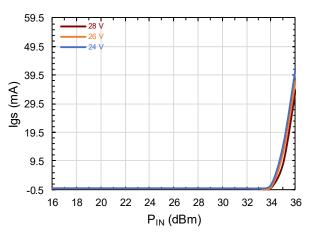


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Drain Efficiency vs. V_{DS} and P_{IN}



Gate Current vs. V_{DS} and P_{IN}





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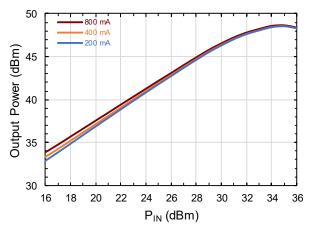
Rev. V1

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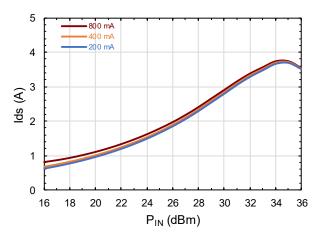
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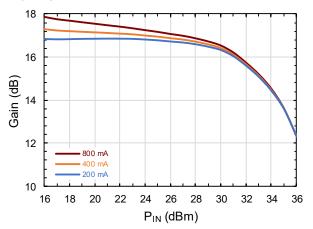
Output Power vs. Inc and PIN



Drain Current vs. I_{DQ} and P_{IN}

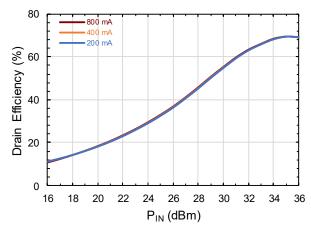


Large Signal Gain vs. IDQ and PIN

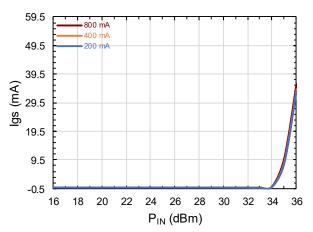


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Drain Efficiency vs. Inc and PIN



Gate Current vs. I_{DQ} and P_{IN}





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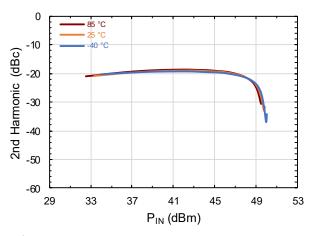
Rev. V1

Typical Performance Curves as Measured in the 2.3-2.7 GHz Evaluation Test Fixture

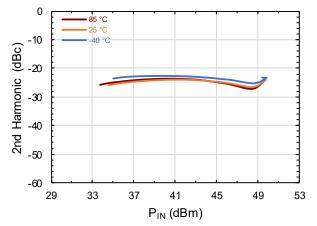
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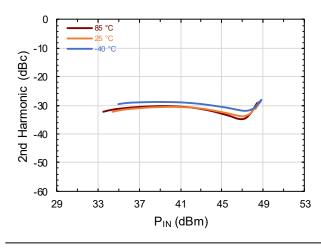
2nd Harmonic vs. Temperature and P_{IN}



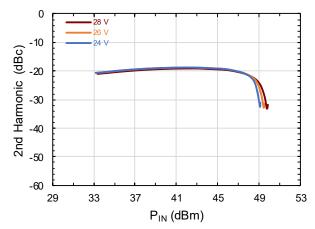
2nd Harmonic vs. Temperature and P_{IN}



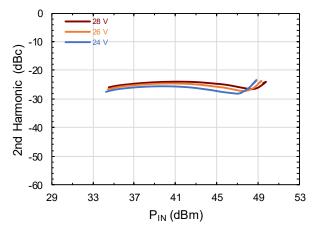




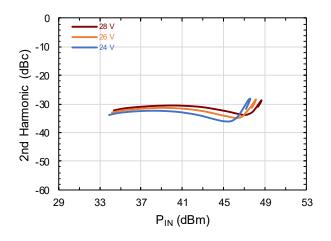
2nd Harmonic vs. V_{DS} and P_{IN}



2nd Harmonic vs. V_{DS} and P_{IN}



2nd Harmonic vs. V_{DS} and P_{IN}



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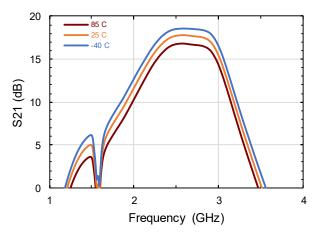
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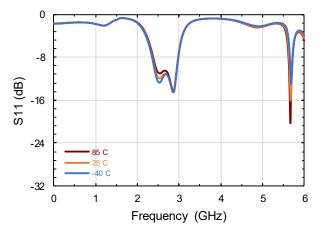
CW, V_{DS} = 28 V, I_{DQ} = 400 mA, Pin=-20dBm (Unless Otherwise Noted)

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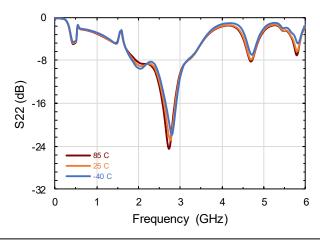
S21 vs Frequency and Temperature



S11 vs Frequency and Temperature

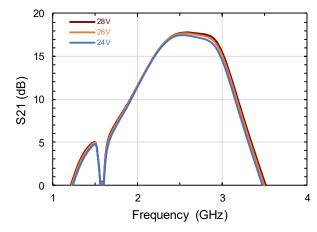


S22 vs Frequency and Temperature

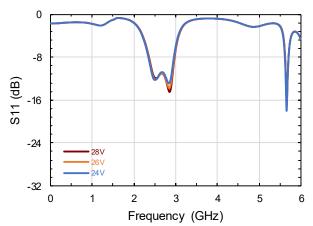


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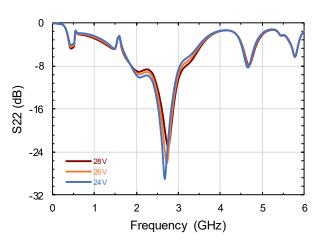
S21 vs Frequency and V_{DS}



S11 vs Frequency and V_{DS}



S22 vs Frequency and V_{DS}



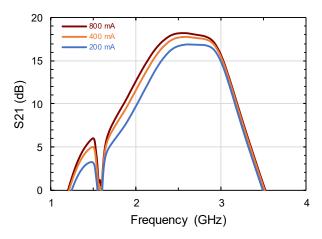


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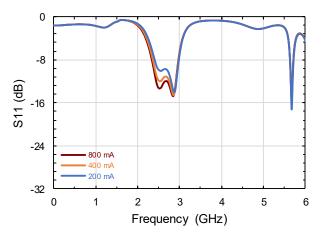
Rev. V1

Typical Performance Curves as Measured in the 2.3- 2.7 GHz Evaluation Test Fixture: CW, $V_{DS} = 28 \text{ V}$, $I_{DQ} = 400 \text{ mA}$, Pin=-20dBm (Unless Otherwise Noted) For Engineering Evaluation Only—This data does not Modify MACOM's Datasheet Limits.

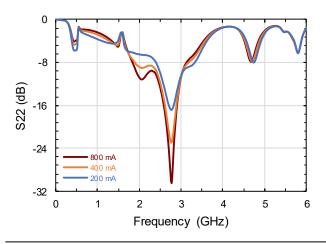
S21 vs Frequency and IDQ



S11 vs Frequency and IDQ



S22 vs Frequency and I_{DQ}



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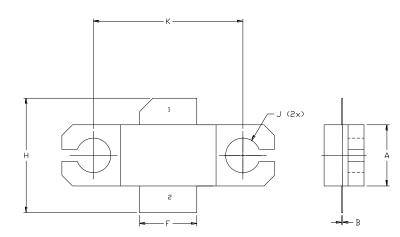


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Lead-free 440223 Package Dimensions

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NDTES: 1. DIMENSIONING AND TOLERANICING PER ANSI Y14.5M, 1982.

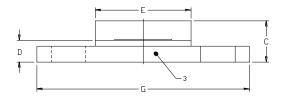
2. CONTROLLING DIMENSION: INCH.

3. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF 0.020' BEYOND EDGE OF LID.

 LID MAY BE MISALIGNED TO THE BODY OF THE PACKAGE BY A MAXIMUM OF 0.008" IN ANY DIRECTION.
ALL PLATED SURFACES ARE NI/AU

ſ		INCHES		MILLIMETERS	
	DIM	MIN	MAX	MIN	MAX
ſ	А	0.225	0.235	5.72	5.97
[В	0.004	0.006	0.10	0.15
[С	0.145	0.165	3.68	4.19
	D	0.077	0.087	1.96	2.21
ſ	E	0.355	0.365	9.02	9.27
ſ	F	0.210	0.220	5.33	5.59
ſ	G	0.795	0.805	20.19	20.45
[н	0.400	0.460	10.16	11.68
[J	ø .130		3.3	30
	k	0.562		14.27	

PIN 1. GATE PIN 2. DRAIN PIN 3. SDURCE



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