Integrated Switch and LNA Module
1.4 - 6.5 GHz

MAMF-011184
Rev. V2

Features

- Broadband: 1.4 - 6.5 GHz
- TX P0.1dB: 42 dBm CW
- Second LNA has Bypass Mode
- Rx High Gain Mode:
  DC Current: 110 mA
  Gain: 33 dB @ 3.5 GHz, 32 dB @ 5.9 GHz
  NF: 1.5 dB @ 3.5 GHz, 2.3 dB @ 5.9 GHz
  OIP3: 35 dBm @ 3.5 GHz, 34 dBm @ 5.9 GHz
- Rx Low Gain Mode:
  DC Current: 45 mA
  Gain: 19 dB @ 3.5 GHz, 17 dB @ 5.9 GHz
  NF: 1.5 dB @ 3.5 GHz, 2.2 dB @ 5.9 GHz
  OIP3: 32 dBm @ 3.5 GHz, 29 dBm @ 5.9 GHz
- Single 5 V Supply
- Compatible with 1.8 V and 3.3 V logic
- Lead-Free 4mm 24-Lead QFN Package
- RoHS* Compliant

Applications

- 5G TDD Base Station
- Automotive V2X
- General Purpose Wireless

Description

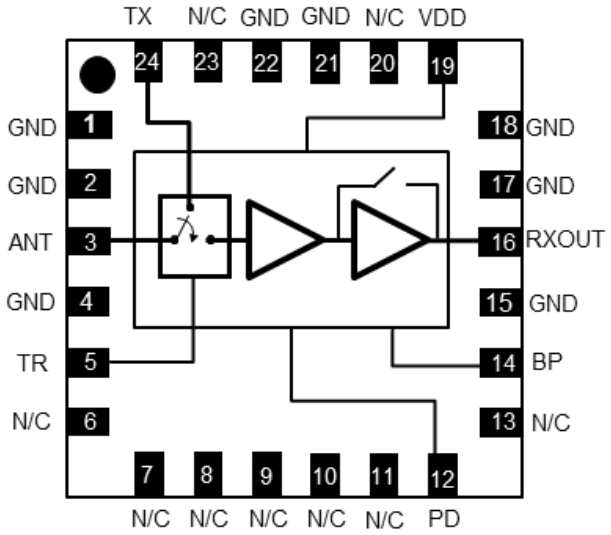
The integrated Switch and LNA Module includes Antenna Switch and 2-stage low noise amplifiers in a compact low cost 4 mm QFN package. The second stage LNA be bypassed. Mixed technologies are used to achieve high power handling, low noise figure, and low power consumption. The module only needs a single +5 V supply. T/R switch, LNA enable, and bypass function can be controlled with 1.8 V or 3.3 V logic.

Ordering Information[1]

Part Number	Package
MAMF-011184-TR1000	1000 piece reel
MAMF-011184-001SMB	Sample Board

1. Reference Application Note M513 for reel size information.

Functional Schematic



Pin Function[2]

Pin #	Function
1, 2, 4, 15, 17, 18, 21, 22	Ground
3	Antenna Port
5	T/R Logic Control
6-11,13, 20, 23	No Internal Connect
12	LNA Power Down Logic
14	Bypass logic
16	RX Output Port
19	Supply voltage
24	TX Input / Load
25	Paddle[3]

2. MACOM recommends connecting unused package pins to ground.
3. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Pin Description

Pin #	Name	Description
1, 2, 4, 15, 17, 18, 21, 22	GND	These pin are grounded internally.
3	ANT	Antenna Pin needs external DC block.
5	TR	TR control signal for switch between RX and TX modes.
6-11,13, 20, 23	N/C	Not connected internally. It is recommended to connect N/C pins to RF grounds of the PCB.
12	PD	Power Down control signal for the LNA.
14	BP	Bypass control signal for second stage of the LNA.
16	RXOUT	RX output pin needs external DC block.
19	VDD	5V Supply pin needs external decoupling capacitors
24	TX	TX input or connected to 50 ohm load, DC Voltage present internally at this pin, needs external DC block.
25	Paddle	Exposed Pad. The exposed pad must be connected to RF, DC and thermal GND.

AC Electrical Specifications: Freq. = 3.5 GHz, T_C = 25°C, VDD = +5 V, Z_0 = 50 Ω, P_{IN}= -30 dBm (unless otherwise stated)

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain at Rx High Gain Mode	2.6 GHz 3.5 GHz 5.0 GHz 5.9 GHz	dB	32 31 29 —	34 33 31 32	—
NF at Rx High Gain Mode	2.6 GHz 3.5 GHz 5.0 GHz 5.9 GHz	dB	—	1.3 1.5 1.9 2.3	—
Input RL at Rx High Gain Mode	—	dB	—	20	—
Output RL at Rx High Gain Mode	—	dB	—	14	—
Output IP3 at Rx High Gain Mode	Tone Spacing = 10 MHz P_{IN} / Tone = -30 dBm 3.5 GHz 5.9 GHz	dBm	—	 35 34	—
Output P1dB at Rx High Gain Mode	—	dBm	—	19.5	—
Gain at Rx Low Gain Mode	2.6 GHz 3.5 GHz 5.0 GHz 5.9 GHz	dB	17 17 16 —	19 19 18 17	—
NF at Rx Low Gain Mode	2.6 GHz 3.5 GHz 5.0 GHz 5.9 GHz	dB	—	1.3 1.5 1.9 2.2	—
Input RL at Rx Low Gain Mode	—	dB	—	18	—
Output RL at Rx Low Gain Mode	—	dB	—	13	—
Output IP3 at Rx Low Gain Mode	Tone Spacing = 10 MHz P_{IN} / Tone = -30 dBm 3.5 GHz 5.9 GHz	dBm	—	 32 29	—
Output P1dB at Rx Low Gain Mode	—	dBm	—	15	—
Insertion Loss at Tx Mode	2.6 GHz	dB	—	0.35	0.8
Return Loss at Tx Mode	—	dB	—	20	—
Input P0.1dB at Tx Mode	—	dBm	—	42	—
Power Consumption	Rx High Gain Rx Low Gain Tx mode	W	—	0.55 0.23 0.008	—

DC Electrical Specifications: Freq. = 3.5 GHz, T_C = 25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Supply Voltage	—	V	4.75	5.0	5.25
Supply Current	Rx High Gain Mode Rx Low Gain Mode Tx Mode	mA	—	110 45 1.3	—
Control Voltage	Logic High Logic Low	V	1.2 0	—	3.45 0.6
Logic Input Current	Logic High Logic Low	µA	—	45	—
RF Switching Time	50% CTL to 10/90% RF	ns	—	500	—
High/Low Gain Mode Switching Time	50% CTL to 10/90% RF	ns	—	150	—

Control Truth Table

Mode	TR	PD	BP	Note
RX mode	Low or Open	Low or Open	Low or Open	HGM[4]
RX mode	Low or Open	Low or Open	High	LGM[5]
TX Mode	High	High	High, Low, or Open	TX

4. HGM: High Gain Mode.
5. LGM: Low Gain Mode.

Recommended Operating Conditions

Parameter	Symbol	Unit	Min.	Typ.	Max.
DC Supply V_{DD}	V_{DD}	V	4.75	5.0	5.25
Logic Pins	TR, BP, PD	V	0	—	3.45
Junction Temperature RX Mode[6,7] TX Mode[6,7] TX Mode[8]	T_J	°C	—	—	 +150°C +125°C +140°C
Operating Temperature[9]	T_C	°C	-40	—	+105

Absolute Maximum Ratings[10,11]

Parameter	Symbol	Unit	Min.	Max.
Antenna Input Power Tx Mode Rx Mode	ANT	dBm	—	40 dBm LTE, 43 dBm CW 23 dBm LTE, 26 dBm CW
DC Voltages	ANT, TX, RXOUT VDD TR, PD, BP	V	-0.3 -0.3 -0.3	+3.6 +5.5 +3.6
Functional Temperature[9]	T_C	°C	-40	+125
Storage Temperature	—	°C	-65	+150

6. Operating at nominal conditions with $T_J \leq +150°C$ in RX mode and <+125°C in TX Mode will ensure MTTF > 1 x 10^6 hours.
7. Junction Temperature $T_J = T_C + \Theta_{JC} * P_{DISS}$ where P_{DISS} is the total DC & RF dissipated power.
   - RX Mode: Typical thermal resistance (Θ_{JC}) = 33.4 ºC/W
   - TX Mode: Typical thermal resistance (Θ_{JC}) = 9.8 ºC/W.
8. Single event, up to 10 seconds duration.
9. Exceeding any one or combination of these limits may cause permanent damage to this device.
10. MACOM does not recommend sustained operation near these survivability limits.
11. Operating Temperature Tc is defined by exposed paddle temperature.

Handling Procedures

Please observe the following precautions to avoid damage:

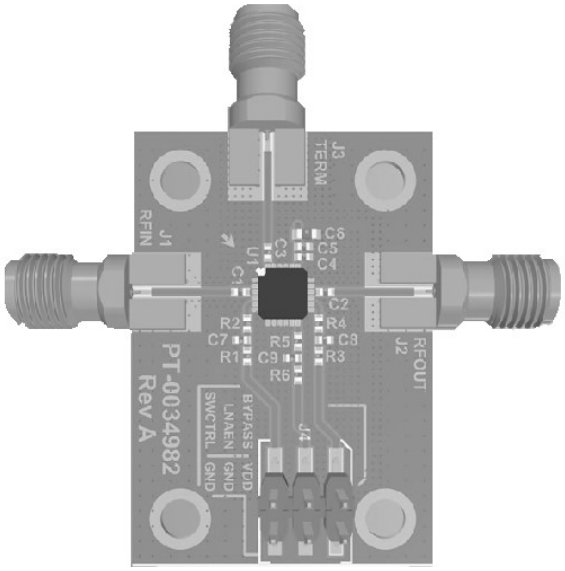
Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A and CDM Class C3 devices.

Power Supplies

De-coupling capacitors should be placed at the V_{DD} supply pin to minimize noise and fast transients. Supply voltage change or transients should have a slew rate smaller than 1 V / 10 µs. In addition, all control pins should remain at 0 V (+/- 0.3 V) and no RF power should be applied while the supply voltage ramps or while it returns to zero.

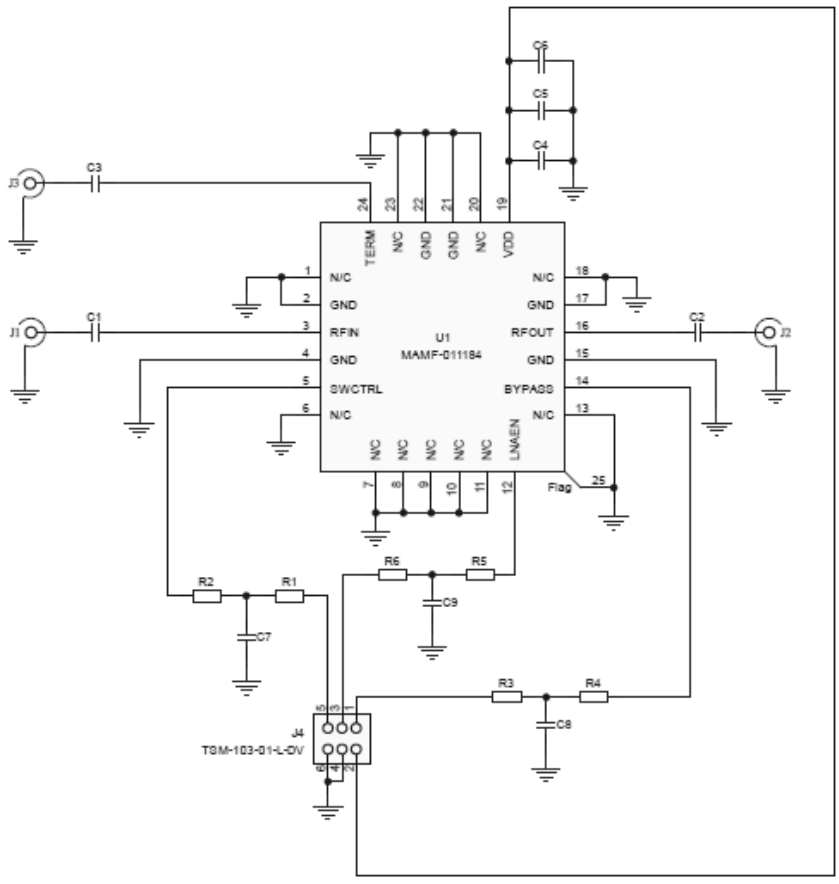
PCB Layout



Parts List

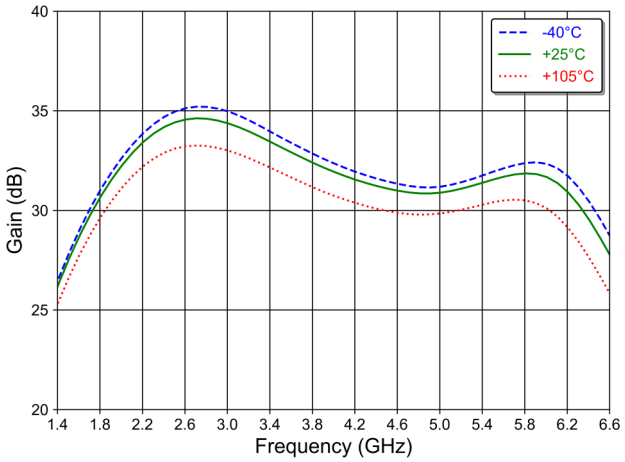
Part	Value	Case Style
C1, C2, C3	20 pF	0402
C4,	470 pF	0402
C5	10 nF	0402
C6	1 µF	0603
C7, C8, C9	5 pF	0402
R1, R3, R6	1 kΩ	0402
R2, R4, R5	0 Ω	0402

Application Schematic

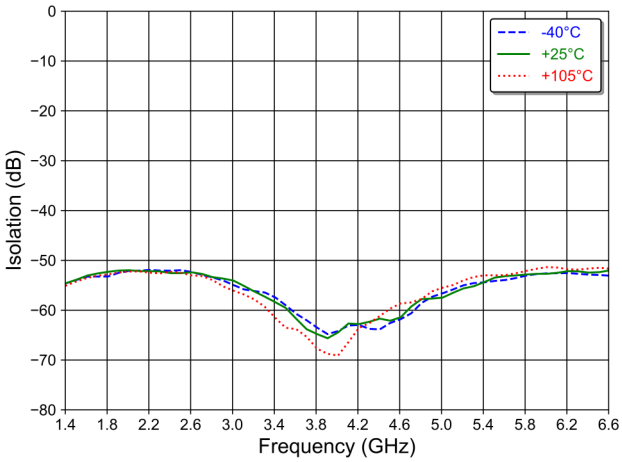


Typical Performance Curves - RX High Gain Mode:
P_{IN} = -30 dBm, VDD = +5 V, Z_0 = 50 Ω (unless otherwise stated)

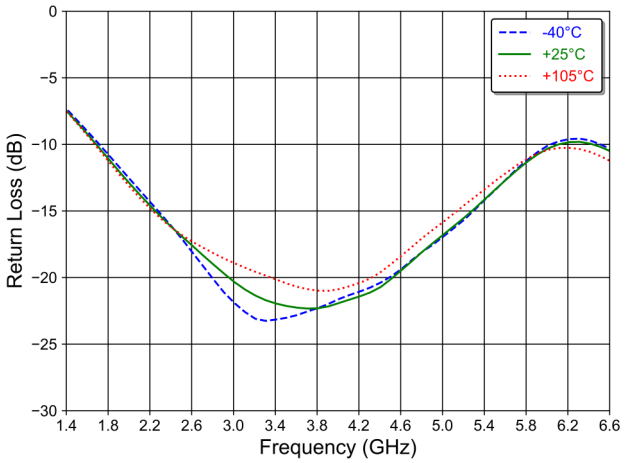
Gain[12]



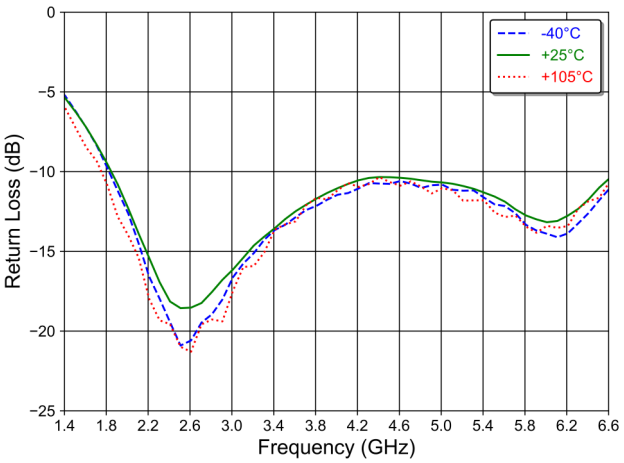
Reverse Isolation



Input Return Loss



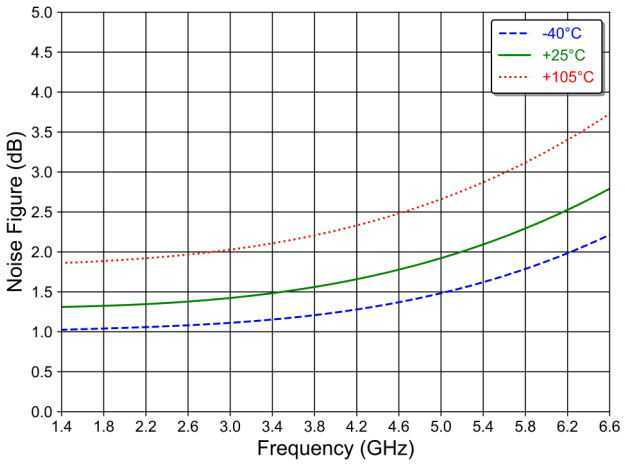
Output Return Loss



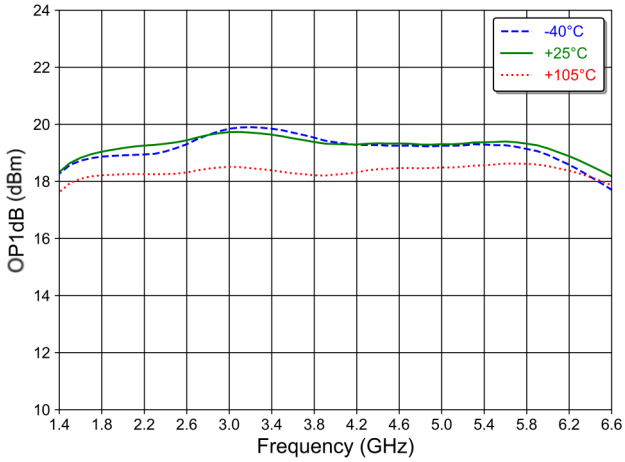
12. For Gain, Insertion Loss, Noise Figure, and Gain Compression plots, RF trace and connector losses are de-embedded .

Typical Performance Curves - RX High Gain Mode:
P_{IN} = -30 dBm, VDD = +5 V, Z_0 = 50 Ω (unless otherwise stated)

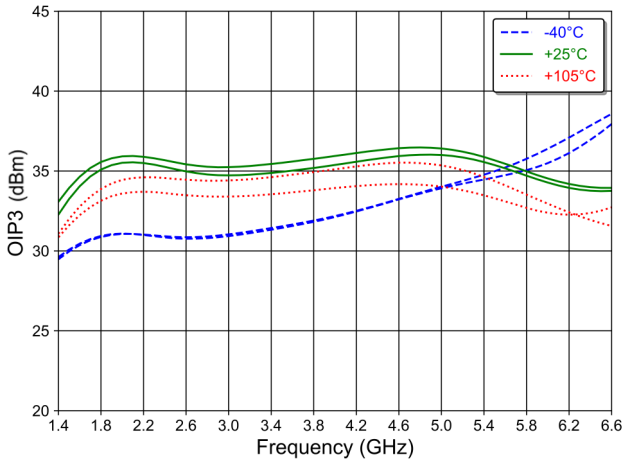
Noise Figure[12]



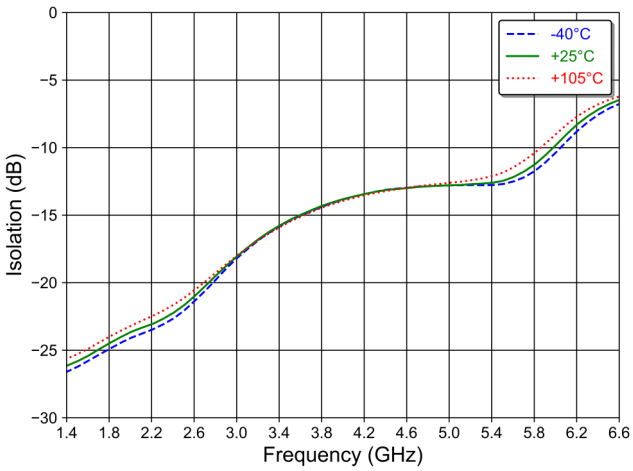
Gain Compression[12]



OIP3 (P_{IN}/Tone = -30 dBm & 10 MHz tone spacing)

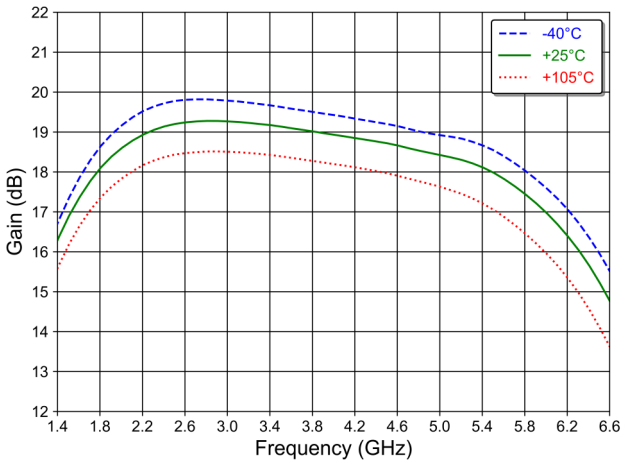


ANT to TERM Isolation

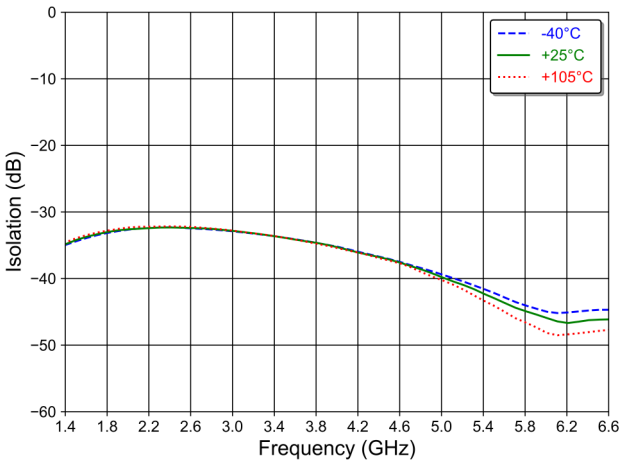


Typical Performance Curves - RX Low Gain Mode:
P_{IN} = -30 dBm, VDD = +5 V, Z_0 = 50 Ω (unless otherwise stated)

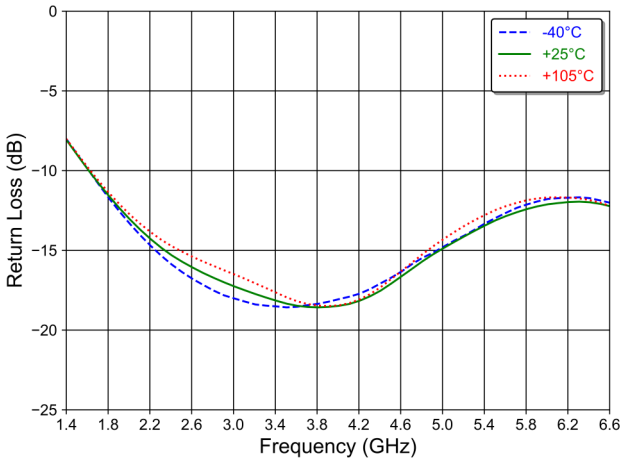
Gain[12]



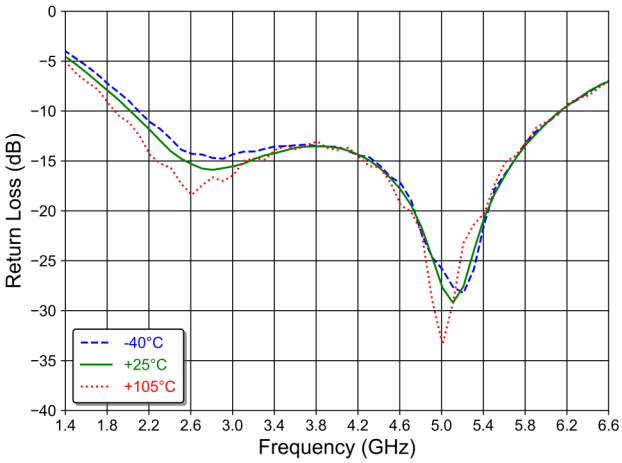
Reverse Isolation



Input Return Loss

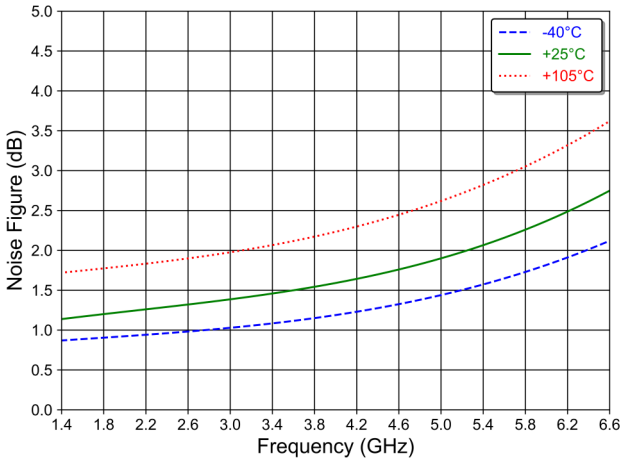


Output Return Loss

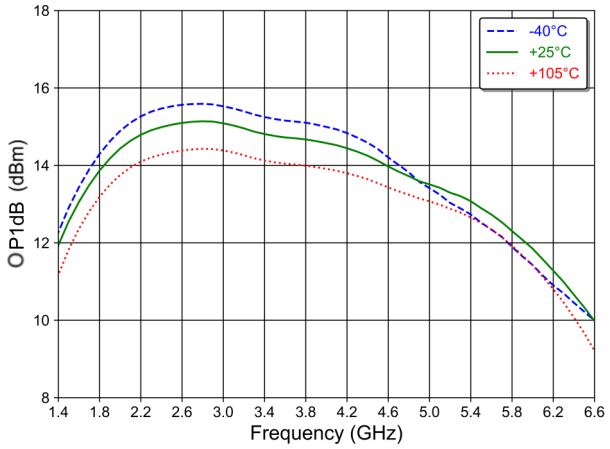


Typical Performance Curves - RX Low Gain Mode:
P_{IN} = -30 dBm, VDD = +5 V, Z_0 = 50 Ω (unless otherwise stated)

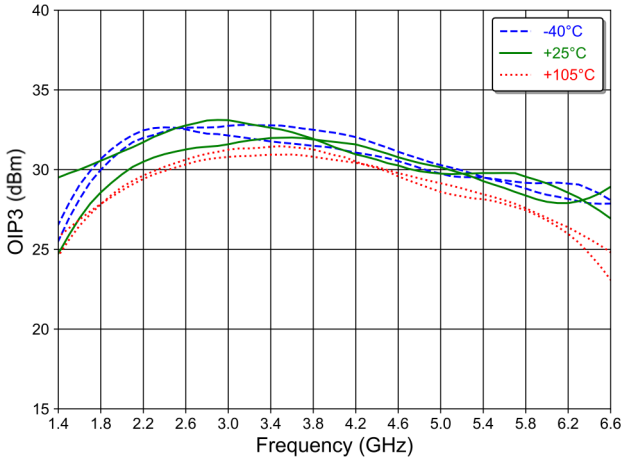
Noise Figure[12]



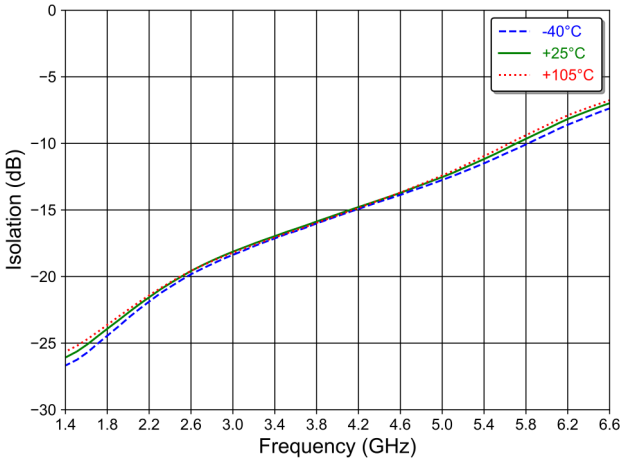
Gain Compression[12]



OIP3 (P_{IN}/Tone = -30 dBm & 10 MHz tone spacing)



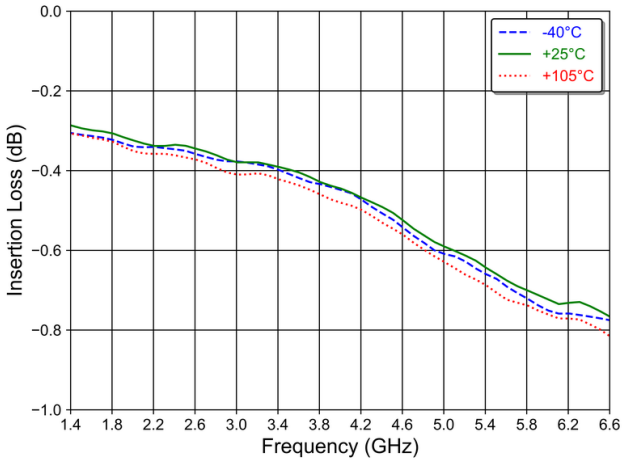
ANT to TERM Isolation



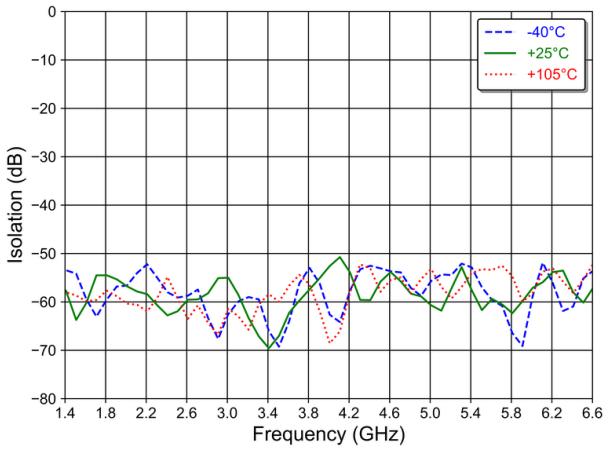
Typical Performance Curves - TX Mode:

P_{IN} = -30 dBm, VDD = +5 V, Z_0 = 50 Ω (unless otherwise stated)

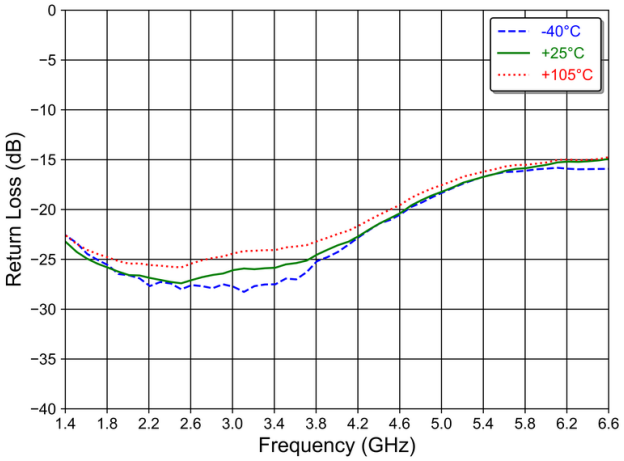
Insertion Loss[12]



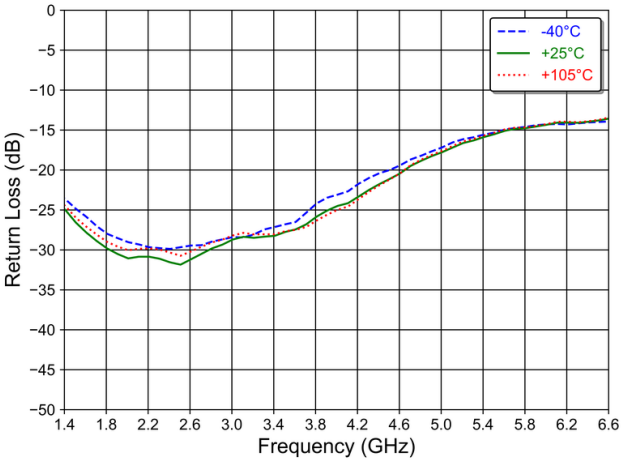
ANT to RXOUT Isolation



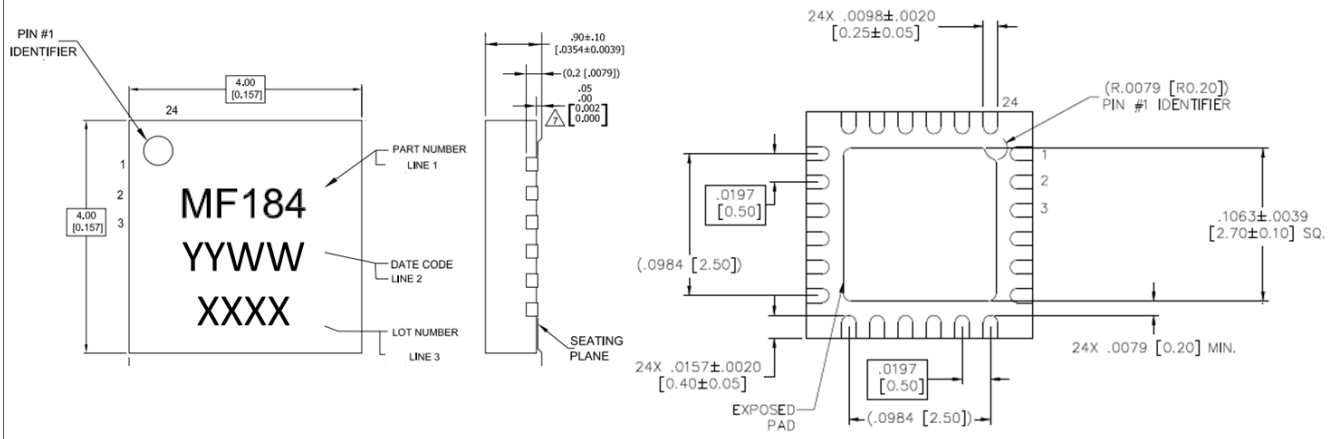
ANT Return Loss



TERM Return Loss



Lead-Free 4 mm 24-Lead QFN†



Notes:
1. Dimensions are in mm [in]
2. Reference JEDEC MO-220 for additional dimensional and tolerance information

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level MSL-1 requirements.
Plating is NiPdAuAg

Revision History

Rev	Date	Change Description
V1	09/27/23	Initial release
V2	11/10/23	Add TX plots and ESD data. Some text corrections.