True Time Delay, 1 Bit
4 - 12 GHz

MADU-FR1012
Rev. V2

Features

- Insertion Loss: 5 dB
- Input Return Loss: -23 dB @ 8 GHz
- Output Return Loss: -10 dB @ 8 GHz
- Input P1dB: 13 dBm @ 8 GHz
- 0 / 4V Control Lines
- Voltage: +/-5 V
- Lead-Free 7 mm, 48-Lead PQFN
- RoHS Compliant to current EU directive

Applications

- Radar
- Telecommunication
- Instrumentation

Description

The MADU-FR1012 is a GaAs MMIC 1-bit True Time Delay operating from 4 GHz up to 12 GHz packaged in a 7 mm plastic QFN.

The application of True Time Delay instead of phase shifter offers an enhanced broadband bandwidth with less beam squinting effects. It uses an optimum switched line to obtain very low delay error and insertion loss variation.

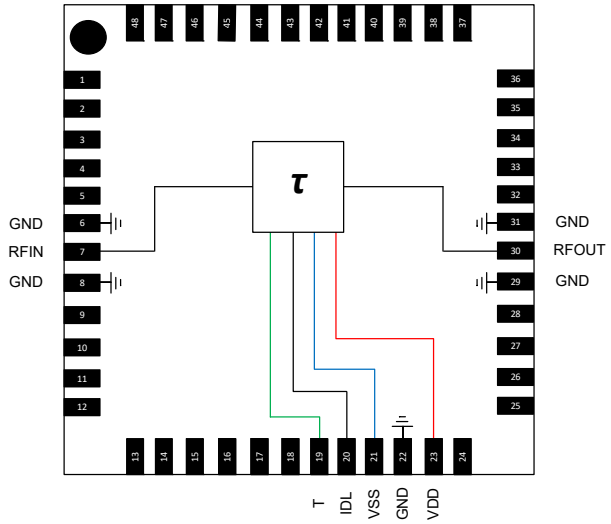
The die is manufactured using 0.18 µm gate length pHEMT technology. The MMIC uses gold bond pads and backside metallization. This technology has been evaluated for Space applications and is on the European Preferred Parts List of the European Space Agency.

Ordering Information[1]

Part Number	Package
MADU-FR1012-TR0500	500 part reel
MADU-FR1012-001SMB	Evaluation Board

1. Reference Application Note M513 for reel size information.

Functional Schematic

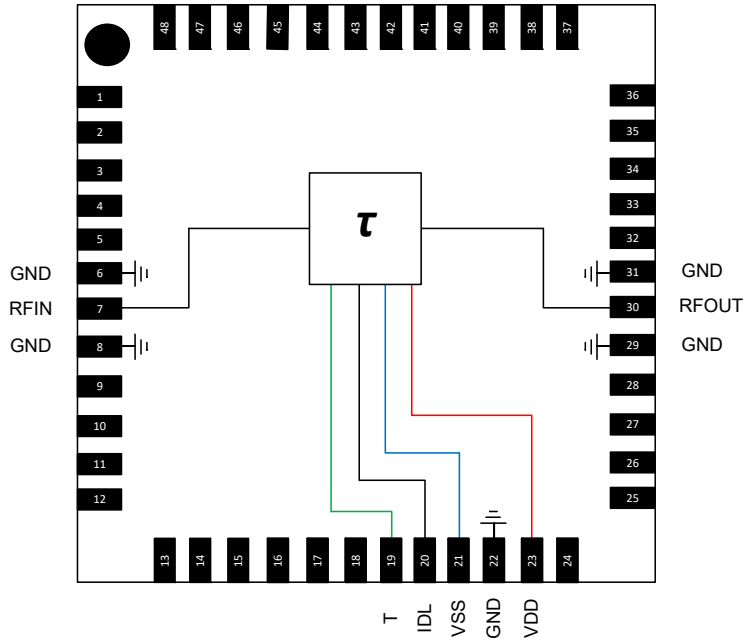


Pin Configuration[2]

Pin #	Function
1 - 5, 9 - 18, 24 - 28, 32 - 48	N/C
6, 8, 22, 29, 31	GND
7	RFIN
19	T
20	IDL
21	VSS
23	VDD
30	RFOUT
Paddle[3]	GND Paddle

2. MACOM recommends connecting unused package pins to ground.
3. The exposed pad centered on the package bottom must be connected to RF and DC ground.

Pin Configuration and Functional Descriptions



Pin #	Pin Name	Description
1,2,3,4,5,9,10,11,12,13,14, 15,16,17,18,24,25,26,27, 28,32,33,34,35,36,37,38,39, 40,41,42,43,44,45,46,47,48	N/C	These pins are not connected internally. It is recommended these are grounded on the application PCB.
7	RFIN	RF Signal Input. This pad is matched to 50 Ω and is DC coupled.
30	RFOUT	RFOUT RF Signal Output. This pad is matched to 50 Ω and is AC coupled
23	VDD	Positive bias supply voltage. For bypassing 47 pF and 0.1 µF SMT capacitors are recommended. The 47 pF capacitor should be placed as closely to the package as physically possible. The positioning of the 0.1 µF capacitor is not as critical but should be placed as close as practically possible.
21	VSS	Negative bias supply voltage. Must be decoupled to the ground with capacitors as close as possible to the package to ensure stability and prevent oscillations.
20	IDL	Amplifier Current Control. No decoupling required.
19	T	An input signal that determines the delay state of the unit. When the control input is High = 4 V, the delay state is activated. When the control input is Low = 0 V, the reference (no delay) state is selected.
6,8,22,29,31	GND	RF, DC ground

Electrical Specifications: Freq. = 4 - 12 GHz, T_A = +25°C, Z_0 = 50 Ω, VSS = -5 V, VDD = +5 V, IDD = 40 mA, ISS = 4.4 mA

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Insertion Loss	Reference State	dB	—	5	8
Time Delay Range	—	ps	290	—	410
Time Delay Error	Delayed State	ps	—	-5/+55	—
Input Reflection Coefficient	Reference State @ 8 GHz	dB	—	-23	—
Output Reflection Coefficient	Reference State @ 8 GHz	dB	—	-10	—
Insertion Loss Variation	Delayed State - Reference State	dB	—	-1.1	—
Input P1dB	Reference State @ 8 GHz	dBm	—	13	—

Recommended Operating Conditions

Parameter	Condition
Time Delay Control Inputs	0 V to 4 V
Supply Voltage Negative Positive	 -5 V to 0 V 0 V to +5 V
Junction Temperature	+150°C
Operating Temperature	-40°C to +85°C

Control Voltage

State	Min.	Typ.	Max.	Unit
Low	-0.1	0	+0.1	V
High	+3.5	+4.0	+4.5	V

Absolute Maximum Ratings[4,5]

Parameter	Absolute Maximum
Time Delay Control Inputs	-0.1 V to 4.5 V
Supply Voltage Negative Positive	 -6 V to 0 V 0 V to +6 V
Input Power @ RFIN	23 dBm
Junction Temperature[6,7]	+150°C
Storage Temperature	-55°C to +150°C

4. Exceeding any one or combination of these limits may cause permanent damage to this device.
5. MACOM does not recommend sustained operation near these survivability limits.
6. Operating at nominal conditions with $T_J \leq$ +150°C will ensure MTTF > 1 x 10^6 hours.
7. Junction Temperature (T_J) = T_C + Θjc * (V * I)
   a) For T_C = +25°C,
   Typical thermal resistance (Θjc) = 118.98°C/W
   T_J = 51.4°C @ 5 V, 44.4 mA
   b) For T_C = +85°C,
   Typical thermal resistance (Θjc) = 142.62°C/W
   T_J = 116.7°C @ 5 V, 44.4 mA

Handling Procedures

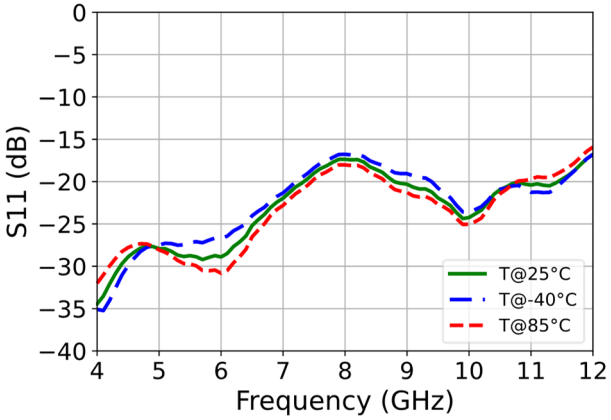
Please observe the following precautions to avoid damage:

Static Sensitivity

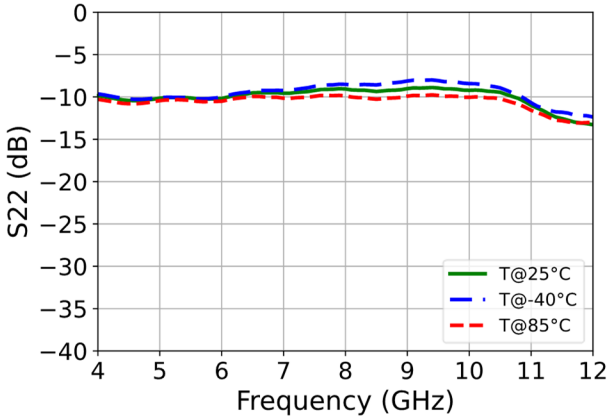
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Typical Performance Curves @ PCB level with De-Embedding:
VDD= +5 V, VSS = -5 V, IDD = 40 mA, ISS = 4.4 mA

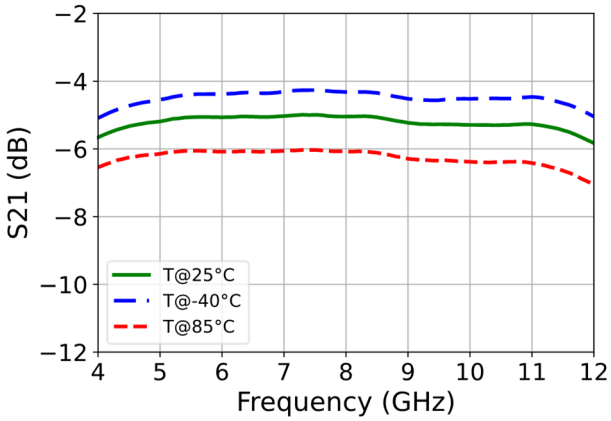
S11 vs. Frequency over Temperature



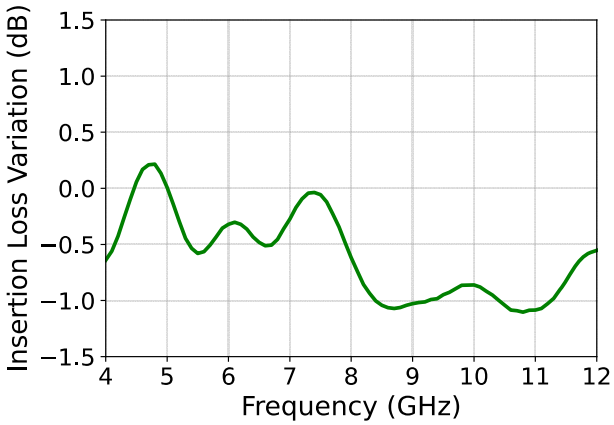
S22 vs. Frequency over Temperature



S21 vs. Frequency over Temperature

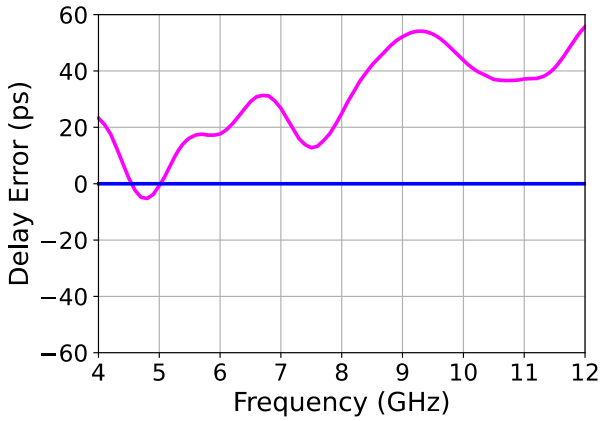


Insertion Loss Variation vs. Frequency at T_c=25°C

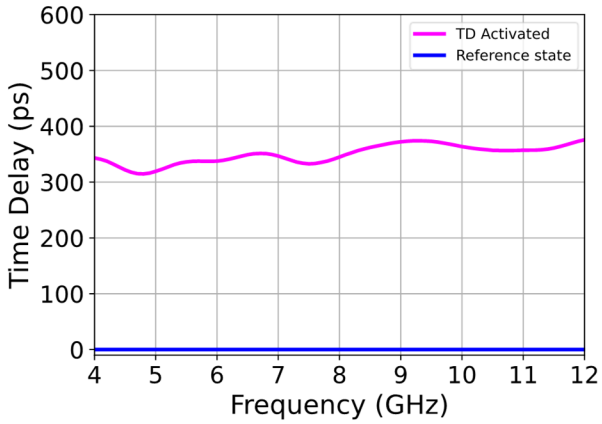


Typical Performance Curves @ PCB level with De-Embedding:
VDD= +5 V, VSS = -5 V, IDD = 40 mA, ISS = 4.4 mA

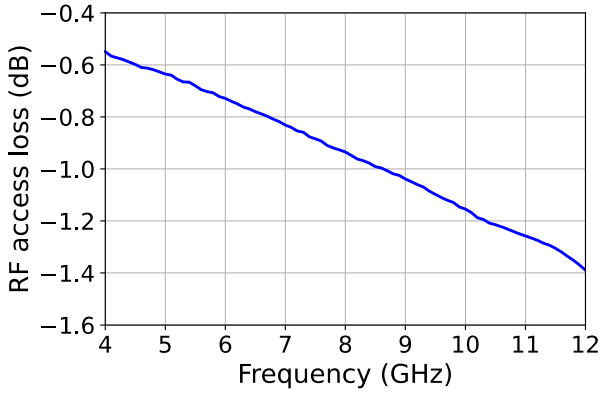
Delay Error vs. Frequency



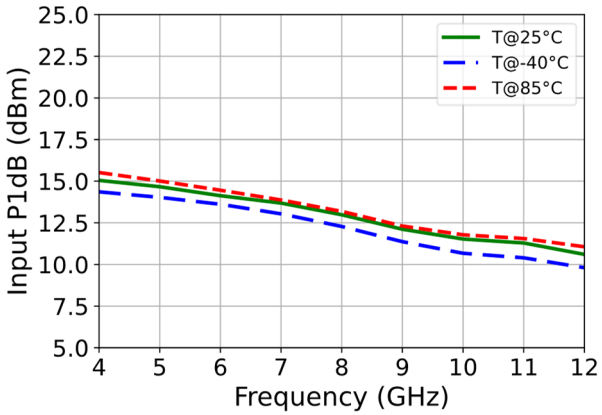
Time delay vs. Frequency



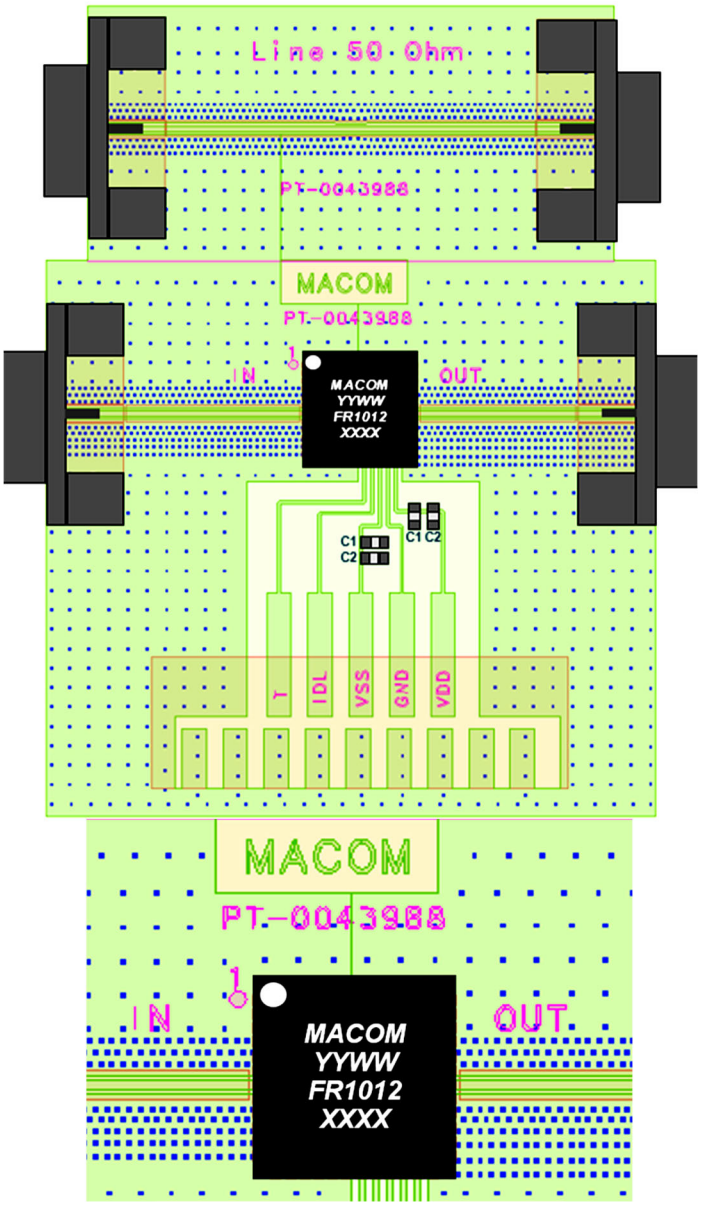
PCB RF Access Loss vs. Frequency



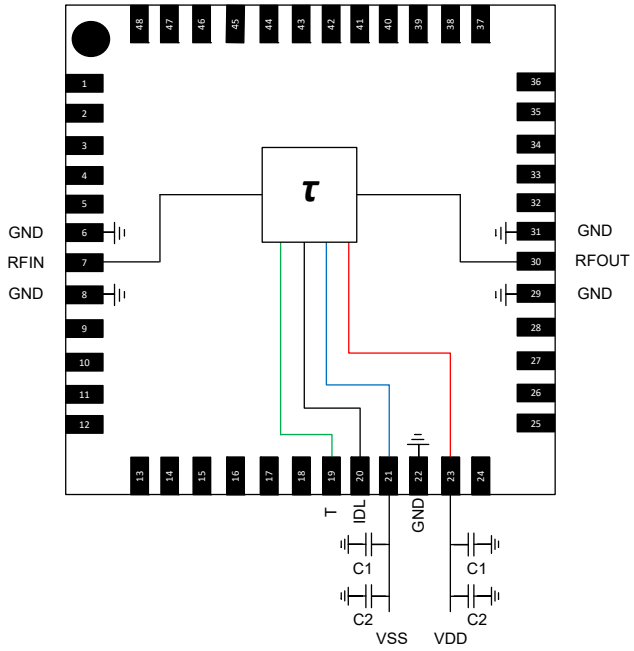
Input P1dB vs. Frequency over Temperature



PCB Layout



Application Schematic



Biasing Procedure

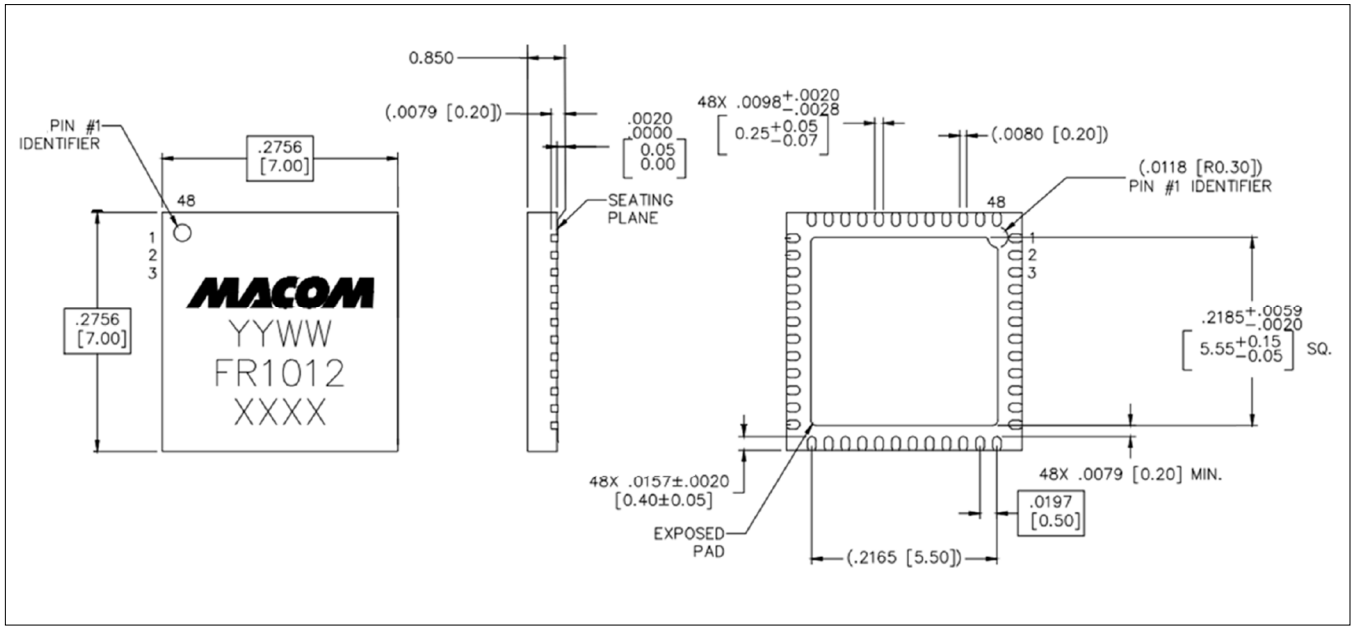
Biasing UP
Set ID limit to 80 mA.
Ensure voltages are at 0 before turning on DC supply.
Set VSS to -5 V and VDD to +5 V.
Ensure ID≈ 40 mA.

Biasing Down
Set VDD and then VSS to 0 V.
Turn off DC supply.

Parts List

Part	Value	Case Style	Manufacturer	Manufacturer's Part #
C1	47 pF	0402	MURATA	GRT1555C1H470JA02D
C2	0.1 µF	0402	KYOCERA AVX	0402YD104KAT2A

Lead-Free 6 mm 48-Lead PQFN†



† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.
Plating is 100% matte tin over copper.

Revision History

Rev	Date	Change description
V1	12/11/25	Production Release
V2	15/01/26	Updated Features Section