

Features

- 40-bit Serial to Parallel Converter
- 20-bit Multiplexer for TX Control bits
- Serial Out Ports for Diagnostics and Daisy Chaining
- Compatible with 5.0 V and 3.3 V CMOS Logic
- Built-in Active Pull-down for Logic Inputs
- Fast Switching
- Low Current consumption
- Lead-Free 6 mm 48-lead PQFN Package
- Halogen-Free “Green” Mold Compound
- RoHS* Compliant and 260°C Reflow Compatible

Description

The MADR-011007 is a 40-bit serial to parallel driver in a low cost 6 mm 48-lead PQFN plastic package. It is designed as the serial control interface for MACOM’s transmit module MAIA-010365 and receive module MAIA-009579. A 20-bit multiplexer is designed on-chip to provide TX bits control capability. High speed digital CMOS technology is utilized to achieve low power dissipation. Even though it is designed to drive GaAs FETs using a -5 V power supply, it can also be used as a general serial to parallel converter when using a +5 V power supply.

This driver, used in conjunction with MACOM’s MAIA-010365 S-Band radar transmit module, MAAP-011022 S-Band 7 W high power amplifier, and the MAIA-009579 receiver, provides a complete chipset for S-Band dual polarization air traffic control and weather radar applications.

Ordering Information¹

Part Number	Package
MADR-011007-TR0500	500 piece reel

1. Reference Application Note M513 for reel size information.

Pin Configuration

Pin No.	Function	Pin No.	Function
1	TX2-phase 1	25	RX2-atten 4
2	TX1-phase 1	26	RX1-atten 4
3	TX1-phase 2	27	RX1-atten 3
4	TX1-phase 3	28	RX1-atten 2
5	TX1-phase 4	29	RX1-atten 1
6	TX1-phase 5	30	RX1-phase 6
7	TX1-phase 6	31	RX1-phase 5
8	TX1-atten 1	32	RX1-phase 4
9	TX1-atten 2	33	RX1-phase 3
10	TX1-atten 3	34	RX1-phase 2
11	TX1-atten 4	35	RX1-phase 1
12	TX2-atten 4	36	RX2-phase 1
13	TX2-atten 3	37	RX2-phase 2
14	TX2-atten 2	38	RX2-phase 3
15	TX2-atten 1	39	RX2-phase 4
16	TX2-phase 6	40	RX2-phase 5
17	GND	41	LOAD
18	VEE	42	CLK
19	TX_STATE	43	SER_IN
20	SNGL_DUAL	44	SER_OUT
21	RX2-phase 6	45	TX2-phase 5
22	RX2-atten 1	46	TX2-phase 4
23	RX2-atten 2	47	TX2-phase 3
24	RX2-atten 3	48	TX2-phase 2
		49	Paddle ²

2. The exposed paddle centered on the package bottom must be either left "open" (no connection) or connected to V_{EE}.

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

40-bit Serial to Parallel Driver for GaAs FETs

Rev. V2

Guaranteed Operating Ranges^{3,4,5}

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{EE}^6	Negative DC Supply Voltage	-5.5	-5.0	-4.5	V
T_{OPER}	Operating Temperature	-40	25	85	°C
I_{OH}	DC Output Current - High	-1	—	—	mA
I_{OL}	DC Output Current - Low	—	—	1	mA

3. Unused logic inputs must be tied to either GND or V_{EE} .

4. 0.01 μ F decoupling capacitors are required on the power supply line.

5. This driver can also operate at -3.3 V V_{EE} , but at slower speed.

6. When using positive logic, GND should be connected to positive power supply +5 V, and V_{EE} should be connected to ground.

Performance over Guaranteed Operating Range

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	Guaranteed High Input Voltage	-1.5	0.0	0.0	V
V_{IL}	Input Low Voltage	Guaranteed Low Input Voltage	-5.5	-5.0	-3.5	V
V_{OH}	Output High Voltage	$I_{OH} = -250 \mu A$	—	-0.1	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 250 \mu A$	—	$V_{EE} + 0.1$	—	V
I_{IN}	Input Leakage Current (per Input)	$V_{IN} = GND$ or V_{EE}	—	80	—	μA
I_{OH}	DC Output Current-High (per Output)	$V_{EE} = -5.0$ V	-1	—	—	mA
I_{OL}	DC Output Current-Low (per Output)	$V_{EE} = -5.0$ V	—	—	1	mA
I_{EE}	Quiescent Supply Current	$V_{IN} = GND$ or V_{EE} , No Output Load	—	—	400	μA
T_D	Propagation Delay	50% LOAD signal to 90% V_O	—	12	—	ns
C_{IN}	Input Capacitance	—	—	6	—	pF

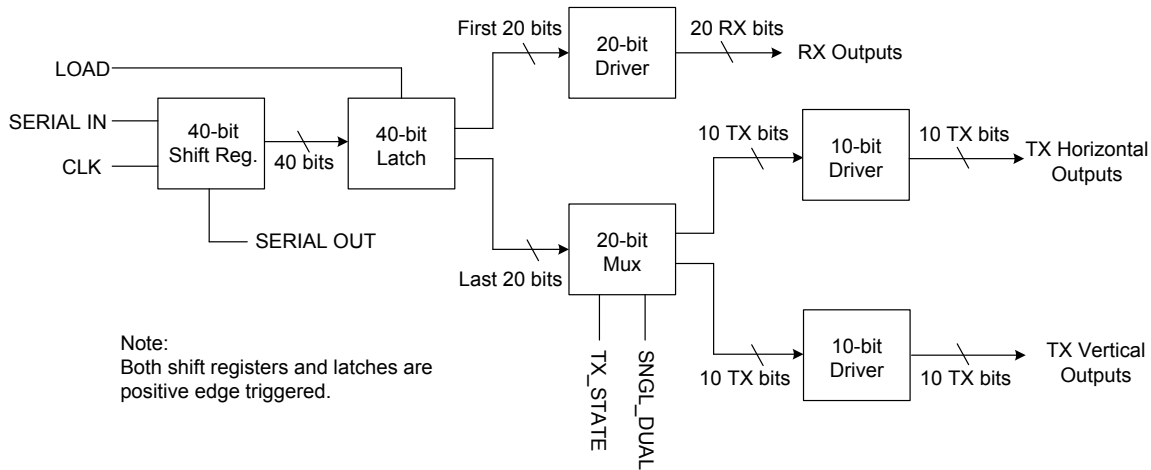
Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{EE}	Negative DC Supply Voltage	-7.0	0.3	V
V_{IN}	DC Input Voltage	$V_{EE} - 0.3$	0.3	V
V_O	DC Output Voltage	$V_{EE} - 0.3$	0.3	V
T_{OPER}	Operating Temperature	-55	125	°C
T_{STG}	Storage Temperature	-65	150	°C
ESD	ESD Sensitivity (HBM)	2.0	—	kV

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Rev. V2

Function Diagram



Note:
Both shift registers and latches are positive edge triggered.

Serial Bit Stream Definition⁷

Bit No.	Bit Function	Bit No.	Bit Function
1	RX2-phase 1	21	TX-phase 1-A
2	RX2-phase 2	22	TX-phase 1-B
3	RX2-phase 3	23	TX-phase 2-A
4	RX2-phase 4	24	TX-phase 2-B
5	RX2-phase 5	25	TX-phase 3-A
6	RX2-phase 6	26	TX-phase 3-B
7	RX2-atten 1	27	TX-phase 4-A
8	RX2-atten 2	28	TX-phase 4-B
9	RX2-atten 3	29	TX-phase 5-A
10	RX2-atten 4	30	TX-phase 5-B
11	RX1-phase 1	31	TX-phase 6-A
12	RX1-phase 2	32	TX-phase 6-B
13	RX1-phase 3	33	TX-atten 1-A
14	RX1-phase 4	34	TX-atten 1-B
15	RX1-phase 5	35	TX-atten 2-A
16	RX1-phase 6	36	TX-atten 2-B
17	RX1-atten 1	37	TX-atten 3-A
18	RX1-atten 2	38	TX-atten 3-B
19	RX1-atten 3	39	TX-atten 4-A
20	RX1-atten 4	40	TX-atten 4-B

7. Bit No. 1 should be the first bit going into the serial interface.

TX Mux Truth Table

Vertical Beam Bits		SNGL_DUAL	
		L	H
TX_STATE	L ⁸	A ⁹	B ⁹
	H ⁸	A	A

Horizontal Beam Bits		SNGL_DUAL	
		L	H
TX_STATE	L	B	A
	H	B	B

8. For $V_{EE} = -5\text{ V}$, Logic "L" = -5 V, and Logic "H" = 0 V.

9. "A" represents odd bits of the 20-bit TX bit stream, and "B" represents even bits of the 20-bit TX bit stream.

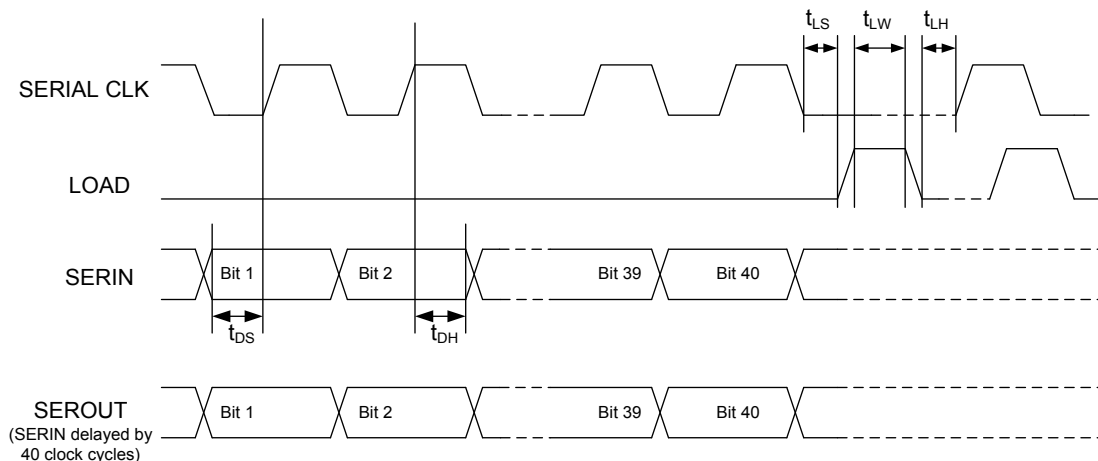
Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Silicon Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Serial Interface Timing Diagram



Serial Interface Timing Characteristics

Symbol	Parameter	Typical performance			Unit
		-40°C	+25°C	+85°C	
t_{SCK}	Min. Serial Clock Period	100	100	100	ns
t_{DS}	Min. DATA Set-up Time	20	20	20	ns
t_{DH}	Min. DATA Hold Time	20	20	20	ns
t_{LS}	Min. LOAD Set-up Time	20	20	20	ns
t_{LW}	Min. LOAD Pulse Width	20	20	20	ns
t_{LH}	Min. Serial CLK Hold Time from LOAD	20	20	20	ns

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