Downconverter
71 - 86 GHz

MADC-011022-DIE
Rev. V1

Features

- E-Band Downconverter
- Direct Down-Conversion with I/Q BW up to 4 GHz
- LO×8 with Buffer
- Conversion Gain: 12 dB
- Noise Figure: 5 dB
- Input IP3: 2 dBm
- Die Size: 2.48 × 2.98 × 0.1 mm

Applications

- Point to Point
- Infrastructure
- Satellite Communications

Description

The MADC-011022-DIE is an integrated E-band down-convertor die combining an LNA, local oscillator multiplier, and a mixer. The MMIC operates from 71 - 86 GHz and is designed to be used in direct conversion or heterodyne applications.

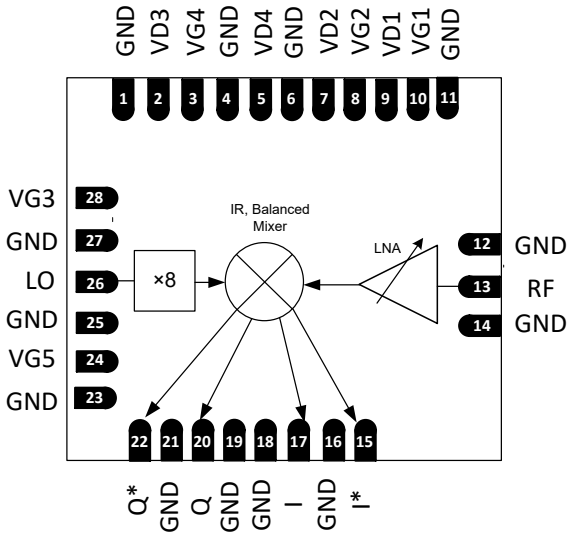
The MMIC provides 12 dB of conversion gain and a noise figure of 5 dB. The linear mixer topology allows for strong IIP3 performance (2 dBm) to be maintained up to the radio input levels recommended in the standards. The baseband is a quadrature balanced four line interface (I, I*, Q, Q*).

The MMIC is ideally suited for low to high capacity, high power E-band point to point radios, and E-band Satcom systems. Each device is 100% RF tested to ensure performance compliance.

Ordering Information

Part Number	Package
MADC-011022-DIE	NA

Functional Schematic



Pin Configuration[1]

Pin #	Pin Name	Function
1,4,6,11,16, 18,19,21,23	GND	DC Ground[2]
2	VD3	Drain Voltage 3
3	VG4	Gate Voltage 4
5	VD4	Drain Voltage 4
7	VD2	Drain Voltage 2
8	VG2	Gate Voltage 2
9	VD1	Drain Voltage 1
10	VG1	Gate Voltage 1
12, 14, 25, 27	GND	RF GND
13	RF	RF Port
15	I*	I*, IF Port
17	I	I, IF Port
20	Q	Q, IF Port
22	Q*	Q*, IF Port
24	VG5	Gate Voltage 5
28	VG3	Gate Voltage 3

1. The backside of the die must be connected to RF, DC and Thermal GROUND.
2. DC ground pads used for on-wafer testing. These do not need to be bonded to GND.

Electrical Specifications:
VD = 3 V, ID1,2,3,4 = 50, 160, 125, 100 mA, VG5 = -2.25 V, PLO = -5 dBm, Backside Temperature (T_B) = +25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
RF Frequency	—	GHz	71	—	86
IF Bandwidth	—	GHz	DC	—	4
LO Frequency	—	GHz	8.625	—	11
LO Multiplication Factor	—			8	
LO Input Power	—	dBm	—	-5	—
Conversion Gain	IF = 700 MHz	dB	14	18	22
Image Rejection	IF = 21.4 MHz	dBc	—	-20	—
Noise Figure	IF = 700 MHz	dB	—	5	7.5
LO×7, LO×9 at RF Port Leakage	No IF Applied	dBm	—	-50	—
LO×8 at RF Port Leakage	No IF Applied	dBm	—	-40	—
Input IP3	IF = 21.4 MHz, ΔIF = 4.6 MHz, Pin = -30 dBm per tone	dBm	—	2	—
C/I2 Two Tones	IF = 21.4 MHz, ΔIF = 4.6 MHz, Pin = -30 dBm per tone	dBc	—	55	—
C/I2 (IF/2)	IF = 21.4 MHz, Pin = -30 dBm	dBc	—	55	—
Input P1dB	IF = 21.4 MHz	dBm	—	-5	—
Return Loss	RF LO IF	dB	—	8 15 8	—

Biasing over Temperature

It is recommended to have a current controlled biasing method.
Temperature data presented here is at the following bias levels unless otherwise specified.
For graphs labelled ID12, stages 1 and 2 are combined to create ID1 + ID2; similarly for ID34.

Pad Label	Current @ -40°C (mA)	Gate Voltage @ -40°C (V)	Current @ +25°C (mA)	Gate Voltage @ +25°C (V)	Current @ +85°C (mA)	Gate Voltage @ +85°C (V)
VD1	37.5	-0.55	50	-0.45	62.5	-0.35
VD2	112.5	-0.55	150	-0.45	187.5	-0.35
VD3	120	-0.38	120	-0.35	120	-0.32
VD4	100	-0.38	100	-0.35	100	-0.32
VG5	-3	-2.25	-3	-2.25	-3	-2.25

Absolute Maximum Ratings[3,4]

Parameter	Absolute Maximum
Drain Voltage	4.3 V
Gate Bias Voltage (VG1,2,3,4)	-1.5 V < VG < 0.3 V
Gate Bias Voltage (VG5)	-5 V < VG < 0.3 V
RF Input Power	0 dBm
LO Input Power	10 dBm
Junction Temperature[5,6]	+150°C
Storage Temperature	-55 to 150°C
Operating Temperature	-40 to 85°C

3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. MACOM does not recommend sustained operation near these survivability limits.
5. Operating at nominal conditions with $T_J \leq 150°C$ will ensure MTTF > 1×10^6 hours.
6. Junction Temperature (T_J) = $T_B + \Theta_{jc} \times (V \times I)$, where T_B is backside temperature of package and Θ_{jc} is thermal resistance of the device.

   See table below for Junction Temperature for each stage of the module. Each stage must remain below 150°C.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1B static sensitive devices.

Pin Label	Thermal Resistance (°C/W)	Current @ +85°C (mA)	T_J for T_B = +85°C (°C)	Maximum Drain Current Rating (mA)
VD1	139	63	111	130
VD2	54	187	115	220
VD3	75	120	112	300
VD4	115	100	120	190

Biasing Methods

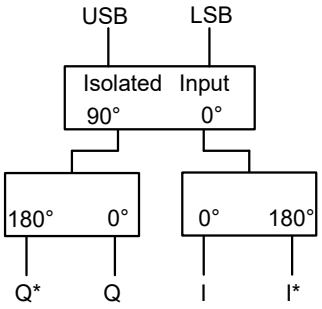
The datasheet presents two different methods for biasing. The first one is to actively biased with a fixed current. This provides a method that consistently groups packages between different manufacturing lots, however it will show variation in gain versus temperature.

The second method is also an active bias, however it is tuned over temperature to maintain constant gain level. This current compensation is a more complex method of biasing but enables consistent performances over both temperature and manufacturing lots.

Bias Sequencing

All gates should be pinched off (VG < -2 V) before the drain voltage (VD = 3 V) is applied. This requirement includes VG5 even though there is no external drain voltage. The gate voltages should then be adjusted as per bias table on Page 2. The current will change when LO is applied to stages three and four.

LSB/USB Operation



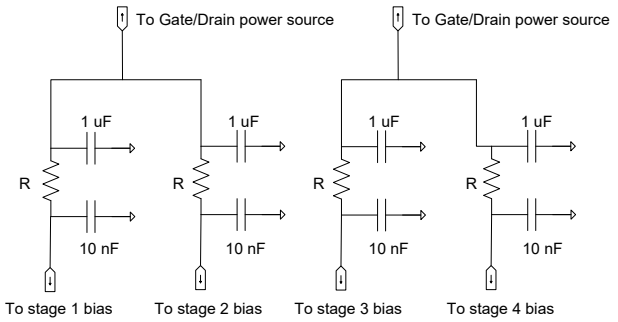
DC Bypassing

Each pin is required to have bypass capacitors. The recommendation is to have 10 nF capacitors close to the die as possible and 1 µF capacitors where space permits. It is not recommended to use 100 pF capacitors due to parallel capacitor resonances with internally mounted capacitors.

When gate stages are tied together, it is recommended to have a small series resistance in the order of 10 Ω. Stages that have a similar function can be combined, that is stage one and two (amplification) and stages three and four (LO multiplication).

Due to the current used on drains, series resistance isn't recommended due to the resulting current drop across the resistor. Ferrite beads can be an alternate source used to isolate drain stages. These ferrite beads generally have an impedance of 100 Ω at 100 MHz. The requirement for these beads is dependent on the board layout and how much coupling arises from parallel traces.

If there are multiple capacitors in parallel to ground it is recommended that one of the capacitors has a small series resistor to dequeue the network to avoid parallel capacitor resonances.



Handling the Die

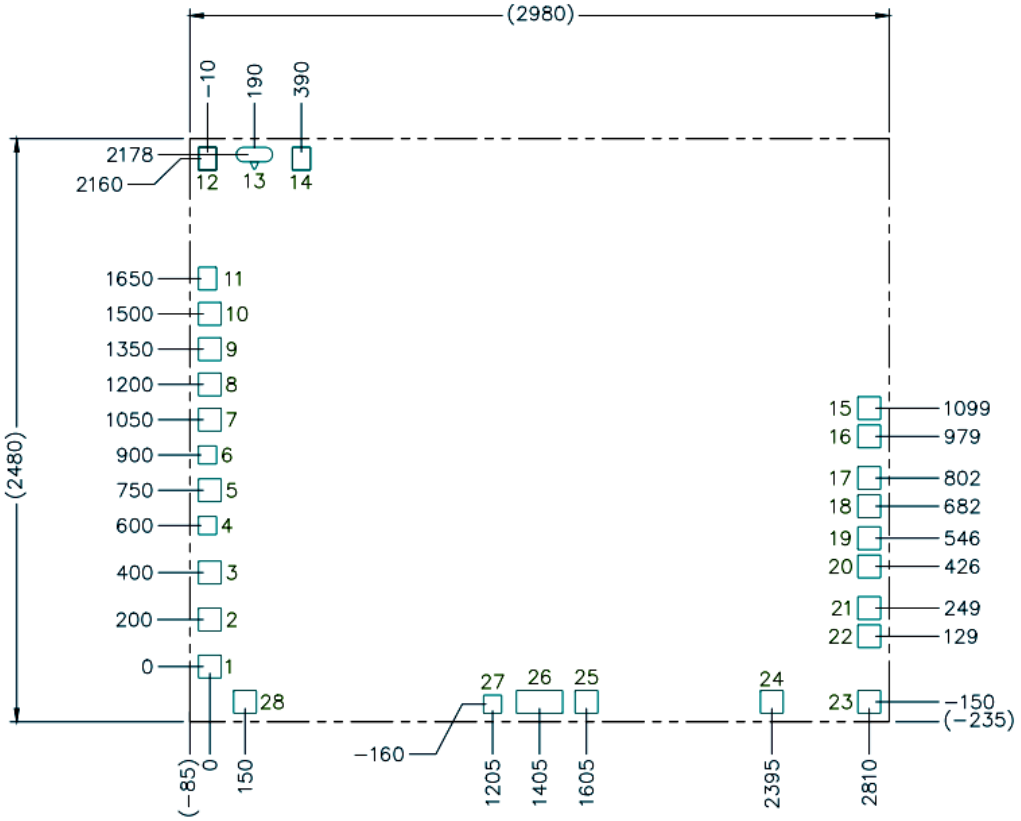
This MMIC has fragile exposed airbridges on its surface and must be handled on the edges only using a vacuum collet or suitable tweezers. Do not touch the surface of the chip with a vacuum collet, tweezers, or fingers.

Die Attach

For mounting the die either an electrically conductive epoxy, or an AuSn eutectic preform can be used.

If using eutectic, an 80% Au / 20% Sn preform is recommended. If using epoxy, a high thermal conductivity epoxy is required and a silver sintering type epoxy is recommended.

Layout Dimensions



BOND PAD SIZE μm					
PAD	SIZE (μm)	REF. DES.	PAD	SIZE (μm)	REF. DES.
1	97 SQ.	GND	18	97 SQ.	GND
2	97 SQ.	VD3	19	97 SQ.	GND
3	97 SQ.	VG4	20	97 SQ.	Q
4	77 SQ.	GND	21	97 SQ.	GND
5	97 SQ.	VD4	22	97 SQ.	Q*
6	77 SQ.	GND	23	97 SQ.	GND
7	97 SQ.	VD2	24	97 SQ.	VG5
8	97 SQ.	VG2	25	97 SQ.	GND
9	97 SQ.	VD1	26	197x97	LO
10	97 SQ.	VG1	27	77 SQ.	GND
11	77x97	GND	28	97 SQ.	VG3
12	77x97	GND			
13	154x62	RF			
14	77x97	GND			
15	97 SQ.	I*			
16	97 SQ.	GND			
17	97 SQ.	I			

NOTES:
1. UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS SHOWN ARE μm WITH A TOLERANCE OF ±5μm.
2. DIE THICKNESS IS 50μm ±20%
3. BOND/PAD BACKSIDE METALLIZATION: GOLD
4. DIE SIZE REFLECTS FINAL DIMENSIONS.