Downconverter
71 - 86 GHz

Features
- E-Band Downconverter
- Direct Down-Conversion with I/Q BW up to 4 GHz
- WR12 Interface for the RF Input
- LO×8 with Buffer
- 12 dB Conversion Gain
- 5 dB Noise Figure
- 2 dBm Input IP3
- RoHS* Compliant Surface Mount Package
- Size: 8.0 × 8.0 × 2.235 mm

Applications
- Point-to-Point

Description
The MADC-011021 is a surface mount E-band receiver. The module operates from 71 - 86 GHz and is designed to be used in direct conversion or heterodyne applications. The RF input is a WR12 interface.

The module provides 12 dB of conversion gain and a noise figure of 5 dB. The linear mixer topology allows for strong IIP3 performance (2 dBm) to be maintained up to the radio input levels recommended in the standards. The baseband is a quadrature balanced four line interface (I, I*, Q, Q*).

Other features include a local oscillator ×8 multiplier and buffer.

Each device is 100% RF tested to ensure performance compliance.

Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>MADC-011021</td>
<td>Parts shipped in tray</td>
</tr>
<tr>
<td>MADC-011021-TR0200</td>
<td>200 part reel</td>
</tr>
<tr>
<td>MADC-011021-TR0500</td>
<td>500 part reel</td>
</tr>
<tr>
<td>MADC-011021-001SMB</td>
<td>Evaluation Board</td>
</tr>
</tbody>
</table>

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DC-0022709
Downconverter
71 - 86 GHz

Electrical Specifications:
VD = 3 V, ID1,2,3,4 = 50, 160, 125, 100 mA, VG5 = -2.25 V,
PLO = -5 dBm, Backside Temperature (T_B) = +25°C

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions²</th>
<th>Units</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF Frequency</td>
<td>—</td>
<td>GHz</td>
<td>71</td>
<td>—</td>
<td>86</td>
</tr>
<tr>
<td>IF Bandwidth</td>
<td>—</td>
<td>GHz</td>
<td>DC</td>
<td>—</td>
<td>4</td>
</tr>
<tr>
<td>LO Frequency</td>
<td>—</td>
<td>GHz</td>
<td>8.625</td>
<td>—</td>
<td>11</td>
</tr>
<tr>
<td>LO Multiplication Factor</td>
<td>—</td>
<td></td>
<td>8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LO Input Power</td>
<td>IF = 21.4 MHz</td>
<td>dBm</td>
<td>—</td>
<td>-5</td>
<td>—</td>
</tr>
<tr>
<td>Conversion Gain</td>
<td>IF = 21.4 MHz</td>
<td>dB</td>
<td>—</td>
<td>-20</td>
<td>—</td>
</tr>
<tr>
<td>Image Rejection</td>
<td>IF = 700 MHz</td>
<td>dBc</td>
<td>—</td>
<td>5</td>
<td>8</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>IF = 700 MHz</td>
<td>dB</td>
<td>—</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LO×7, LO×9 at RF Port Leakage</td>
<td>No IF Applied</td>
<td>dBm</td>
<td>—</td>
<td>-50</td>
<td>—</td>
</tr>
<tr>
<td>LO×8 at RF Port Leakage</td>
<td>No IF Applied</td>
<td>dBm</td>
<td>—</td>
<td>-40</td>
<td>—</td>
</tr>
<tr>
<td>Input IP3</td>
<td>IF = 21.4 MHz, ΔIF = 4.6 MHz, Pin = -30 dBm per tone</td>
<td>dBm</td>
<td>—</td>
<td>2</td>
<td>—</td>
</tr>
<tr>
<td>C/I2 Two Tones</td>
<td>IF = 21.4 MHz, ΔIF = 4.6 MHz, Pin = -30 dBm per tone</td>
<td>dBc</td>
<td>—</td>
<td>55</td>
<td>—</td>
</tr>
<tr>
<td>C/I2 (IF/2)</td>
<td>IF = 21.4 MHz, Pin = -30 dBm</td>
<td>dBc</td>
<td>—</td>
<td>55</td>
<td>—</td>
</tr>
<tr>
<td>Input P1dB</td>
<td>IF = 21.4 MHz</td>
<td>dBm</td>
<td>—</td>
<td>-5</td>
<td>—</td>
</tr>
<tr>
<td>Return Loss</td>
<td>RF LO IF</td>
<td>dB</td>
<td>—</td>
<td>8</td>
<td>8</td>
</tr>
</tbody>
</table>

2. Graphs in datasheet use test conditions as shown above unless otherwise specified.

Biasing over Temperature
It is recommended to have a current controlled biasing method.
Temperature data presented here is at the following bias levels unless otherwise specified.
For graphs labelled ID12, stages 1 and 2 are combined to create ID1 + ID2; similarly for ID34.

<table>
<thead>
<tr>
<th>Pad Label</th>
<th>Current @ -40°C (mA)</th>
<th>Gate Voltage @ -40°C (V)</th>
<th>Current @ +25°C (mA)</th>
<th>Gate Voltage @ +25°C (V)</th>
<th>Current @ +85°C (mA)</th>
<th>Gate Voltage @ +85°C (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VD1</td>
<td>37.5</td>
<td>-0.55</td>
<td>50</td>
<td>-0.45</td>
<td>62.5</td>
<td>-0.35</td>
</tr>
<tr>
<td>VD2</td>
<td>112.5</td>
<td>-0.55</td>
<td>150</td>
<td>-0.45</td>
<td>187.5</td>
<td>-0.35</td>
</tr>
<tr>
<td>VD3</td>
<td>120</td>
<td>-0.38</td>
<td>120</td>
<td>-0.35</td>
<td>120</td>
<td>-0.32</td>
</tr>
<tr>
<td>VD4</td>
<td>100</td>
<td>-0.38</td>
<td>100</td>
<td>-0.35</td>
<td>100</td>
<td>-0.32</td>
</tr>
<tr>
<td>VG5</td>
<td>-3</td>
<td>-2.25</td>
<td>-3</td>
<td>-2.25</td>
<td>-3</td>
<td>-2.25</td>
</tr>
</tbody>
</table>
Absolute Maximum Ratings\textsuperscript{3,4}

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Absolute Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain Voltage</td>
<td>4.3 V</td>
</tr>
<tr>
<td>Gate Bias Voltage (VG1, 2, 3, 4)</td>
<td>-1.5 V &lt; VG &lt; 0.3 V</td>
</tr>
<tr>
<td>Gate Bias Voltage (VG5)</td>
<td>-5 V &lt; VG &lt; 0.3 V</td>
</tr>
<tr>
<td>RF Input Power</td>
<td>0 dBm</td>
</tr>
<tr>
<td>LO Input Power</td>
<td>+10 dBm</td>
</tr>
<tr>
<td>Junction Temperature\textsuperscript{5,6}</td>
<td>+150°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-55 to 150°C</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-40 to 85°C</td>
</tr>
</tbody>
</table>

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1B static sensitive devices.

3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. MACOM does not recommend sustained operation near these survivability limits.
5. Operating at nominal conditions with $T_J \leq 150^\circ C$ will ensure $MTTF > 1 \times 10^6$ hours.
6. Junction Temperature ($T_J$) = $T_b + \Theta_{jc} \times (V \times I)$, where $T_b$ is backside temperature of package and $\Theta_{jc}$ is thermal resistance of the device.

See table below for Junction Temperature for each stage of the module. Each stage must remain below 150°C.

<table>
<thead>
<tr>
<th>Pin Label</th>
<th>Thermal Resistance (°C/W)</th>
<th>Current @ +85°C (mA)</th>
<th>$T_J$ for $T_b$ = +85°C (°C)</th>
<th>Maximum Drain Current Rating (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VD1</td>
<td>139</td>
<td>63</td>
<td>111</td>
<td>130</td>
</tr>
<tr>
<td>VD2</td>
<td>54</td>
<td>187</td>
<td>115</td>
<td>220</td>
</tr>
<tr>
<td>VD3</td>
<td>75</td>
<td>120</td>
<td>112</td>
<td>300</td>
</tr>
<tr>
<td>VD4</td>
<td>115</td>
<td>100</td>
<td>120</td>
<td>190</td>
</tr>
</tbody>
</table>
Downconverter
71 - 86 GHz

Typical Performance Curves over Temperature

Conversion Gain at Nominal Bias at IF = 21.4 MHz

Conversion Gain vs. LNA Bias at IF = 21.4 MHz

Conversion Gain at Nominal Bias at IF = 700 MHz

Conversion at Fixed Current at IF = 21.4 MHz

Conversion Gain at Nominal Bias at IF = 4 GHz

Conversion Gain vs. LO Power at IF = 21.4 MHz
Downconverter
71 - 86 GHz

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MACOM-011021
Rev. V1

Typical Performance Curves over Temperature

**Noise Figure at Nominal Bias at IF = 700 MHz**

![Graph showing noise figure at nominal bias with temperature variations.](image)

**Noise Figure at Fixed Bias at IF = 700 MHz**

![Graph showing noise figure at fixed bias with temperature variations.](image)

**Noise Figure vs. LNA Bias at IF = 700 MHz, RF = 86 GHz**

-40°C
-25°C
+85°C

![Graph showing noise figure vs. LNA bias with temperature variations.](image)

**Noise Figure vs. LNA Bias at IF = 700 MHz, RF = 86 GHz**

-40°C
-25°C
+85°C

![Graph showing noise figure vs. LNA bias with temperature variations.](image)

**Noise Figure vs. LNA Bias at IF = 700 MHz, RF = 86 GHz**

-40°C
-25°C
+85°C

![Graph showing noise figure vs. LNA bias with temperature variations.](image)

**Noise Figure vs. LNA Bias at IF = 700 MHz, RF = 86 GHz**

-40°C
-25°C
+85°C

![Graph showing noise figure vs. LNA bias with temperature variations.](image)

**Noise Figure vs. LNA Bias at IF = 700 MHz, RF = 86 GHz**

-40°C
-25°C
+85°C

![Graph showing noise figure vs. LNA bias with temperature variations.](image)
Downconverter
71 - 86 GHz

Typical Performance Curves over Temperature

**Input Referred IP3 at Nominal Bias at IF = 21.4 MHz**

![Graph showing Input Referred IP3 vs. Frequency at IF = 21.4 MHz over temperature.]

**Input Referred IP3 vs. LNA Bias at IF = 21.4 MHz, RF = 86 GHz**

![Graph showing Input Referred IP3 vs. LNA Bias at IF = 21.4 MHz, RF = 86 GHz.]

**Input Referred IP3 at Nominal Bias at IF = 700 MHz**

![Graph showing Input Referred IP3 vs. Frequency at IF = 700 MHz over temperature.]

**Input Referred IP3 vs. LO Bias at IF = 21.4 MHz**

![Graph showing Input Referred IP3 vs. LO Bias at IF = 21.4 MHz.]

**Input Referred IP3 at Nominal Bias at IF = 4 GHz**

![Graph showing Input Referred IP3 vs. Frequency at IF = 4 GHz over temperature.]

**Input Referred IP3 vs. LO Power at IF = 21.4 MHz**

![Graph showing Input Referred IP3 vs. LO Power at IF = 21.4 MHz.]

7. $\Delta$IF is 11 MHz
Downconverter
71 - 86 GHz

Typical Performance Curves over Temperature

Conversion Gain to each IF vs. IF, RF = 71 GHz

Image Rejection at IF = 21.4 MHz

Conversion Gain to each IF vs. IF, RF = 86 GHz

Image Rejection at IF = 700 MHz

Image Rejection at IF = 4 GHz

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71 - 86 GHz

Typical Performance Curves over Temperature

P1dB at Nominal Bias at IF = 21.4 MHz

P1dB vs. LO Power at IF = 21.4 MHz, RF = 71 GHz

P1dB vs. LO Power at IF = 21.4 MHz, RF = 76 GHz

P1dB vs. LO Power at IF = 21.4 MHz, RF = 81 GHz

P1dB vs. LO Power at IF = 21.4 MHz, RF = 86 GHz
Typical Performance Curves over Temperature

Two-Tone C/I2 at Pin = -27 dBm total at IF = 21.4 MHz

Single-Tone C/I2 (IF/2) at Pin = -30 dBm at IF = 21.4 MHz

Single-Tone C/I2 (IF/2) at Pin = -30 dBm at IF = 700 MHz

Single-Tone C/I2 (IF/2) at Pin = -30 dBm at IF = 4 GHz

RF Return Loss

LO Return Loss
Downconverter
71 - 86 GHz

Typical Performance Curves over Temperature

RF Return Loss vs. VG12 Sweep, Temp = -40°C

RF Return Loss vs. VG12 Sweep, Temp = +25°C

RF Return Loss, VG12 Sweep, Temp = +85°C

IF Return Loss, ID12 = 150 mA, Temp = -40°C

IF Return Loss, ID12 = 200 mA, Temp = +25°C

IF Return Loss, ID12 = 250 mA, Temp = +85°C

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Typical Performance Curves over Temperature

**LO×6 Leakage at RF port with No IF**

![LO×6 Leakage Graph]

**LO×7 Leakage at RF port with No IF**

![LO×7 Leakage Graph]

**LO×8 Leakage at RF port with No IF**

![LO×8 Leakage Graph]

**LO×9 Leakage at RF port with No IF**

![LO×9 Leakage Graph]

**LO×10 Leakage at RF port with No IF**

![LO×10 Leakage Graph]
**Downconverter**

**71 - 86 GHz**

**Biasing Methods**
The datasheet presents two different methods for biasing. The first one is to actively biased with a fixed current. This provides a method that consistently groups packages between different manufacturing lots, however it will show variation in gain versus temperature.

The second method is also an active bias, however it is tuned over temperature to maintain constant gain level. This current compensation is a more complex method of biasing but enables consistent performances over both temperature and manufacturing lots.

**Bias Sequencing**
All gates should be pinched off (VG < -2 V) before the drain voltage (VD = 3 V) is applied. This requirement includes VG5 even though there is no external drain voltage. The gate voltages should then be adjusted as per bias table on Page 2. The current will change when LO is applied to stages three and four.

**LSB/USB Operation**

<table>
<thead>
<tr>
<th>USB</th>
<th>LSB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Isolated</td>
<td>Input</td>
</tr>
<tr>
<td>90°</td>
<td>0°</td>
</tr>
<tr>
<td>180°</td>
<td>0°</td>
</tr>
</tbody>
</table>

Q* Q I I*

**LSB USB**

0° 0°

Isolated

180° 0°

Input

180° 0°

**DC Bypassing**
each pin is required to have bypass capacitors. The recommendation is to have 10 nF capacitors close to the package as possible and 1 μF capacitors where space permits. It is not recommended to use 100 pF capacitors due to parallel capacitor resonances with internally mounted capacitors.

When gate stages are tied together, it is recommended to have a small series resistance in the order of 10 Ω. Stages that have a similar function can be combined, that is stage one and two (amplification) and stages three and four (LO multiplication).

Due to the current used on drains, series resistance isn’t recommended due to the resulting current drop across the resistor. Ferrite beads can be an alternate source used to isolate drain stages. These ferrite beads generally have an impedance of 100 Ω at 100 MHz. The requirement for these beads is dependent on the board layout and how much coupling arises from parallel traces.

If there are multiple capacitors in parallel to ground it is recommended that one of the capacitors has a small series resistor to dequeue the network to avoid parallel capacitor resonances.

**Package Alignment**
The SMD package is ideal for pick and place assembly. The package should self align. It is recommended that a solder stencil is used complying with Application Note S2083. To minimize solder flowing into waveguide area, stencil can be inset an additional 25 µm.

**Reflow Profile**
This package is capable of lead free reflow. The recommended reflow profile depends on the solder used however Application Note S2083 has guidelines that can be applied to this product.
Layout for Evaluation Board

PCB Layout Recommendations
The gerbers, DXF and Altium files for the evaluation board are available on request. It is recommended that VD2 and VD4 DC traces are separated as soon as possible to minimise on board coupling. A simple way to separate the two traces is to have them running on different PCB layers on the board. The image above is a capture of the evaluation board. It can be noted that each adjacent DC trace is alternating on different layers.
For optimum RF performance, all NCs should be terminated to ground.

The exposed paddle centered on the package bottom must be connected to RF, DC and thermal ground.
Downconverter
71 - 86 GHz

Layout Dimensions

Bottom Layer Viewed From The Top

Top View

Major dimensions provided are in millimeters [inches]
DXF of footprint can be provided on request
Reference Application Note M538/S2083 for lead-free solder reflow recommendations. Meets JEDEC moisture sensitivity level (MSL) 3 requirements.
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