5G GaN FEM Power Management Controller
Supply :-6V(Optional), +5V

MABC-11050B
Rev V4

Features

- Quad Output I²C programmable analogue outputs using 12bit DACs with rail to rail output voltage range
  - Output current capability +10mA / -6mA
  - Programmable gate-current limit
  - I²C clock rates up to 400kHz
- Internal and external temperature sensor supporting temperature compensation in application
- Built in sequencing with drain bias control support
- Sequenced auxiliary current source
- Fast Charge Capability
- Two 12bit Telemetry ADC inputs
- Internal EEPROM for autonomous operation
- General purpose GPIO interface
- Optional internal negative voltage generator, generating –5V from the positive 5V supply
- Supply voltage range –6V, 5V

Applications

- GaN FET bias Controller
- HEMT bias Controller
- Circuit Temperature Compensation

The MABC-11050 is a flexible bias generation and temperature supervision IC.

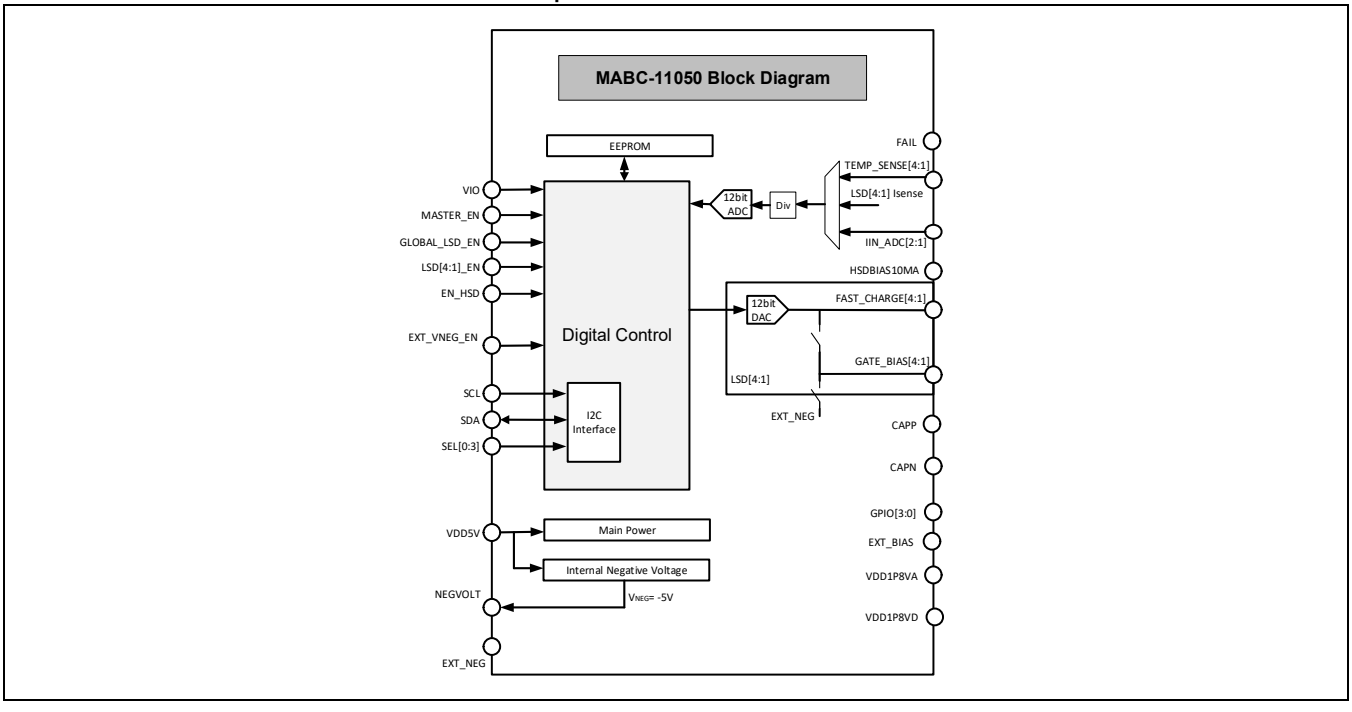
The MABC-11050 contains four highly integrated, temperature-controlled DACs that support a negative output range from -6V to 0V and are capable of handling large output currents. The four DACs can be programmed independently by four separate user-defined temperature-to-voltage functions stored in the internal EEPROM, allowing any temperature effects to be corrected without additional external circuitry. Each output can be switched to the load individually through the use of dedicated control pins.

The MABC-11050 provides bias sequencing for safe power up and power down. The drain voltage may be applied with a control signal via the internal drain bias control once the IC has powered up and correct biasing has been asserted.

Once powered up, the device operates autonomously, without intervention from the system controller, providing a complete solution for setting and compensating bias voltages and currents in control applications. Additionally, the device supports up to four thermistors placed closely to the PAs for more accurate temperature reading.

The digital interface allows control and monitoring of all four Low side drivers, gate current, and temperature of the PA. In addition, the drain current of the PA can be monitored via an external high-side current sense amplifier and an internal ADC.

Simplified Functional Schematic



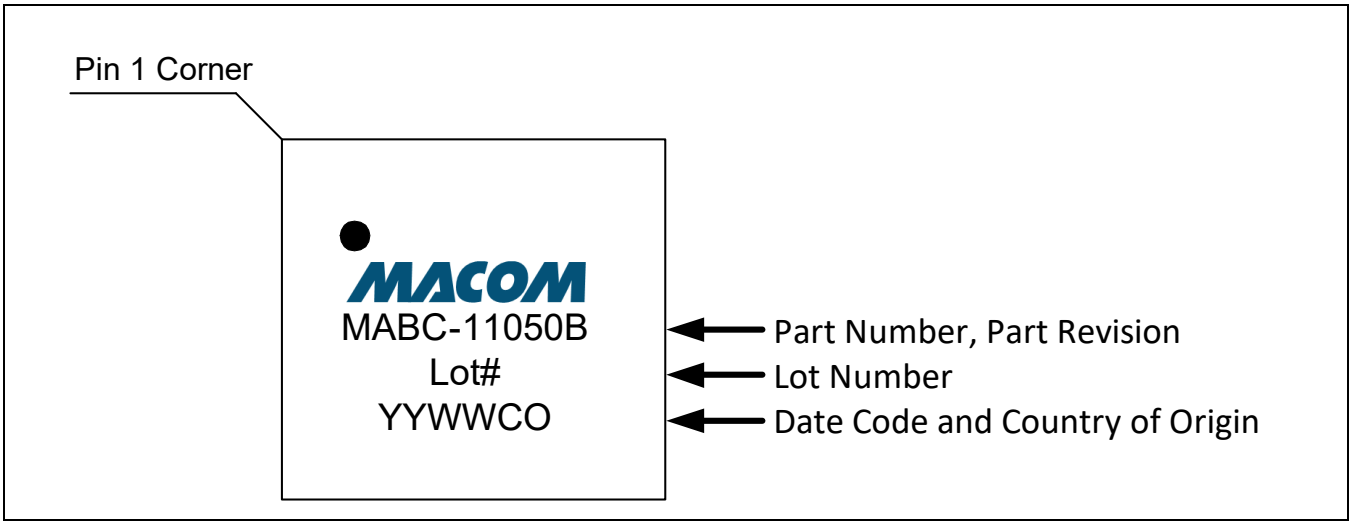
Ordering Information

Part Number	Package	Operating Temperature
MABC-11050B	6 x 6 mm PQFN48	-40°C to +125°C
MABC-11050B-SB2PPR	EVM Kit	-40°C to +125°C

Revision History

Revision	Level	Date	Description
V4	Release	Apr 2024	Updated Power-up and Power down Sequencing; Updated Electrical characteristics for sink current at off state.
V3	Release	Jul 2023	Updated pin39, 40 description; Updated Chapter 4
V2	Release	Oct 2022	Updated pinout and function description; Removed application chapter
V1	Release	May 2022	Updated pinout diagram and Electrical characteristics
V1P	Preliminary	March 2021	Updated Electrical characteristics
V1A	Advance	August 2020	Initial release

Figure 1-1. MABC-11050 Marking Diagram



1.0 Electrical Characteristics

Unless noted otherwise, specifications in this section are valid with VDD5V = 5 V, VDD1P8V = 1.8 V, EXT_NEG = -5 V, and an ambient temperature of 25°C.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Notes	Min.	Max.	Units
VDD5V	Positive Supply Voltage (5V)	1,2		5.5	V
VIO	Digital Power Supply	1,2		3.6	V
EXT_NEG	Negative Analog Voltage Input	1,2	-6.05		V
T_{sold}	Lead Soldering Temperature	1,2		260	°C
$T_{J,ABS}$	Junction Temperature	1,2,3,4		140	°C
C_ldo	Output Capacitor on Pin 43	5	1		uF
V_{HBM}	Human-body model		-2000	+2000	°C
V_{CDM}	Charged-device model		-500	+500	°C
T_{Store}	Storage Temperature	1,2,3,4		140	°C

NOTE:

1. Exceeding any one or a combination of these parameter limits may cause permanent damage to the device and cause the device to not function properly.
2. MACOM does not recommend sustained operation near these survivability limits
3. Operating with normal conditions with TJ ≤ 150°C will ensure MTTF > TBD hours.
4. Junction Temperature (TJ) = TC + θjc * (V * I) , Typical thermal resistance (θc) = TBD°C/W.θjc (Junction – Case) is the thermal resistance between the Junction and the Case. The temperature of the Case is defined as the temper-ature of exposed paddle.
5. If use internal LDO for 1.8V supply.

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units
VDD5V	Positive Supply Voltage (5V)		4.75	5	5.25	V
VIO	Digital Power Supply		1.65		3.6	V
EXT_NEG	Negative Analog Voltage Input		-6	-5	-4.5	V
I_{VDD5V}	Current consumption in low power mode (MASTER_EN = Low)				9	mA
	Charge pump enable (default setting)	1	--	26	--	mA
	Charge pump disabled	3	-	10	--	mA
I_{VIO}	Current consumption for VIO		0	0.5	1	mA
I_{NEG}	Supply Current from Negative Supply	4	-	16	--	mA
T_{Case}	Operating Junction Temperature	2	-40		115	°C

NOTE:

1. Quiescent current for charge pump is ~2mA/Mhz based on the working frequency. Pin 16 and 17 shorted. Mid code for all LSD,no load, the current on all 5V and VIO. With internal 1.8V Supply.Current sense of LSD off.
2. Tj, Junction temperature is based on Theta JC (bottom) = 2°C/W.
3. Charge pump is disabled. Pin 16 and Pin 17 is opened. Mid code and no load on LSD. Measure the current to all positive supply.With internal 1.8V Supply.
4. Typical current on EXT_NEG when for MABC11050 With internal 1.8V Supply.

Table 1-3. Electrical Characteristics

Symbol	Parameter	Notes	Min	Typ	Max	Unit
	Low Side Driver					
R_{STAB}	Stability Resistance			0.5		Ω
TLSD_RDY	Response time from power on to all LSD_rdy with load capacitor=10uF			10		msec
VCPRI	Output Voltage Ripple on charge pump	2		50		mV
VLDRI	Output Voltage Ripple on charge pump	1		0.2		mV
BW_LSD	-3 dB Bandwidth of LSD	3	72			KHz
Ccharge	Min Load drive capacitance (MABC11050)	4	1	10		uF
LSD_FC	90% fast-charge time @ 10nF load (MABC11050)	5		100	150	nsec
LSD_FC99	99% fast-charge time @ 10nF load (MABC11050)	5			500	nsec
C_RATIO	capacitor Ccharge/CRF ratio between FAST_CHARGEx pin and GATE_BIASx pin (MABC11050 only)			1000		nF/nF
CRF	Load capacitance on Gate_bias node (MABC11050)				10	nF
GERR_SOURCE_M1V	Gate Control Voltage Error Over iload sourcing current, process & mismatch variation @ -1V (MABC11050)		-61			mV
GERR_SOURCE_VNEG_PLUS_1V	Gate Control Voltage Error Over iload sourcing current, process & mismatch variation @ VNEG+1V (MABC11050)		-69			mV
GERR_SINK_M1V	Gate Control Voltage Error Over iload sinking current, process & mismatch variation @ -1V (MABC11050)				38	mV
GERR_SINK_VNEG_PLUS_1V	Gate Control Voltage Error Over iload sinking current, process & mismatch variation @ VNEG+1V (MABC11050)				49	mV
VLD_RES	Adjustable Gate Control Voltage Resolution (MABC11050)	6		1.7		mV

NOTE:

1. -10mA to 6mA load.
2. Cfly=1uF, Cout=22uF, load of charge pump<150mA.
3. Clsd=10uF.
4. Minimum capacitance required for on-chip OPAMP stability.
5. 10µF at FAST_CHARGEx /10nF at GATE_BIASx, measured from GLOBAL_LSD_EN or LSD_EN pin transitions to gate bias pin rising from -5V to -1V.
6. 12-bit DAC,depends on feedback resistor accuracy in note 4.
7. 0.1% resistor tolerance between the feedback resistor of LSD versus the resistor on ext_bias pin.

Table 1-3. Electrical Characteristics

Symbol	Parameter	Notes	Min	Typ	Max	Unit
LSD Drive Characteristics						
V_{GATE_INT}	Adjustable Gate Voltage using integrated charge-pump	0mA Sourced	1	-VDD5V	0	V
		10mA Sourced		-1		
		6mA Sunk		-4.2		
V_{GATE_EXT}	Adjustable Gate Voltage using external charge-pump	0mA Sourced	2	EXT_NEG	0	V
		10mA Sourced		-1		
		6mA Sunk		EXT_NEG+ 0.8		
V_{HRMN}	Headroom voltage from LSD_DRV/LSD_DAC to negative voltage	0mA Sourced		10		mV
		10mA Sourced	3	400		
		6mA Sunk		400		
V_{HRMP}	Headroom voltage from GND to LSD_DRV/LSD_DAC, source	0mA Sourced		10		mV
		10mA Sourced	3	400		
		6mA Sunk		400		

NOTE:
1. VDD5V = 5V; Rgate = 6Ω
2. External negative supply = EXT_NEG
3. Including bond wire loss, the chip need such minimum headroom for output to meet the spec

Table 1-3. Electrical Characteristics

Symbol	Parameter	Notes	Min	Typ	Max	Unit
LSD_DRV Current Characteristics						
ILIMIT	Adjustable Gate Voltage using integrated charge pump		20		140	mA
ILIMITRES	Current Limit Resolution			30		mA
ILIMITRES_ER	Current Limit Resolution Error			10		mA
LSD_SSD	Slow Shutdown Response Time	1		10		msec
LSD_LRT	Limiter response time (time constant)			20		usec
NOTE: 1. 10uF output capacitor.						
LSD_DRV Current Sense						
LSD_IRES	Gate Current Digitised Readout Resolution (12-bit)			24		uA
LSD_IRES_SINK_ER1	Gate Current Measurement Percentage Error	2	-10	0	10	%
LSD_IRES_SINK_ER2	Gate Current Measurement Current Error	3	-1000	0	1000	uA
LSD_IRES_SINK_ER3	Gate Current Measurement Current Error	4	-6	0	6	mA
LSD_IRES_SOURCE_ER1	Gate Current Measurement Percentage Error	2	-10	0	10	%
LSD_IRES_SOURCE_ER2	Gate Current Measurement Current Error	3	-1000	0	1000	uA
LSD_IRES_SOURCE_ER3	Gate Current Measurement Current Error	5	-10	0	10	mA
LSD_CUR_RT	Gate Current Measurement Time Error			750		usec
NOTE: 1. Max total gate current from each LSD drivers 2. System errors all added together, Absolute value of (LSD_CUR)>10mA, output range between (-1V, EXT_NEG+1V) 3. System errors all added together, Absolute value of (LSD_CUR)<10mA,output range between (-1V, EXT_NEG+1V) 4. System errors all added together, LSD_CUR=-6mA,output range between (-1V, EXT_NEG+1V) 5. System errors all added together, LSD_CUR=+10mA,output range between (-1V, EXT_NEG+1V).						
LSD Temperature Sense						
THERM_VRANGE	Input Voltage range for TEMP_SENSEx pins		0		2	V
Fail Alert						
FAIL_RT	Fail alert response time				2	msec

Table 1-3. Electrical Characteristics

Symbol	Parameter	Notes	Min	Typ	Max	Unit
HSD Driver Current Characteristics						
HSD_CUR_ON	Typical Current bias range for high side driver	1	3		10	mA
HSD_CUR_STEP	Eight Steps	1		1		mA
HSD_CUR_OFF	Current sunk at “OFF” state	2			0.1	uA
HSD_SW	HSD turn on time	3			10	msec
HSD_CAP	PFET capacitance allowed	4			20	uF
HSD_accuracy	Current accuracy		-5		5	%
NOTE: 1. Current sunk in on state 2. Current sunk in off state 3. Configurable; From EN_HSD pin to voltage on gate bias pin settle 4. no data sheet of PMIC, application note only						
ADC Electrical Specification						
ADC_RANGE	Input Range	--	0	--	1	V
ADC_RES	ADC resolution	--	--	0.244	--	mV
ADC_DNL	DNL		-1		1	LSB
ADC_INL	INL			10		LSB
ADC_IMP	Input impedance	--	600	--	--	KΩ
ADC_RT	Response time	--	--	1	--	msec
ADC_SR_single	Conversion time, single channel	1	--	0.05	--	msec
ADC_SR_Row	Conversion time, whole channel	2	--	0.75	--	msec
ADC_OFF	Input offset	--	--	1	--	mV
ADC_ERROR_FS	ADC error at full scale excitation	--	-1.5	--	1.5	%
NOTE: 1. Sample rate for each channel 2. Sample rate for whole channe						

Table 1-4. Control/Interface Logic Static Specifications (EN_HSD, GLOBAL_LSD_EN,MASTER_EN, EXT_VNEG_EN, LSDx_EN,GPIO0-3,FAIL, SDA, SCL)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units
VIH	Input Logic High Threshold		0.65*VIO			V
VIL	Input Logic Low Threshold				0.35*VIO	V
Vhyst1	hysteresis of Schmit trigger input(VIH-VIL)		0.05*VIO	0.1*VIO		V
VOH	VOH Output Logic High	1	VIO-0.4			V
VOL	VOL Output Logic Low	2,3			0.4	V
Tdhl	delay from pad to core, high to low	4		8	12	nS
Tdlh	delay from pad to core, low to high	4		8	12	nS
C_{IN}	I/O pins internal capacitance			1.5		pF
I2C_CAP	Board capacitance on I2C nodes	5		65		pF

NOTE:
1. With 3mA sinking load
2. with 3mA source load
3. Fail pin is open drain so only VOL applied to it
4. run with Trise=Tfall=6ns input signal, measure between middle points
5. Total capacitor on the bus should not be higher than 65pF

Table 1-5. I^2C Digital Level Margin

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units
VDD5V	I2C Digital Level	1	VDD5V-0.1V	VDD5V	VDD5V	V
N/C	I2C Digital Level	1	VDD5V-0.3V	4.5V	VDD5V-0.6	V
VIO	I2C Digital Level		1.4V	3.3V	3.63V	V
GND	I2C Digital Level		0V	0V	1.2V	V

Note:
1. Using a 0ohm resistor as a pull up to either VIO or VDD5V

2.0 Package Outline Drawing, Pinout Diagram, and Pin Descriptions

2.1 MABC-11050 Pinout

Figure 2-1. MABC-11050 Pinout

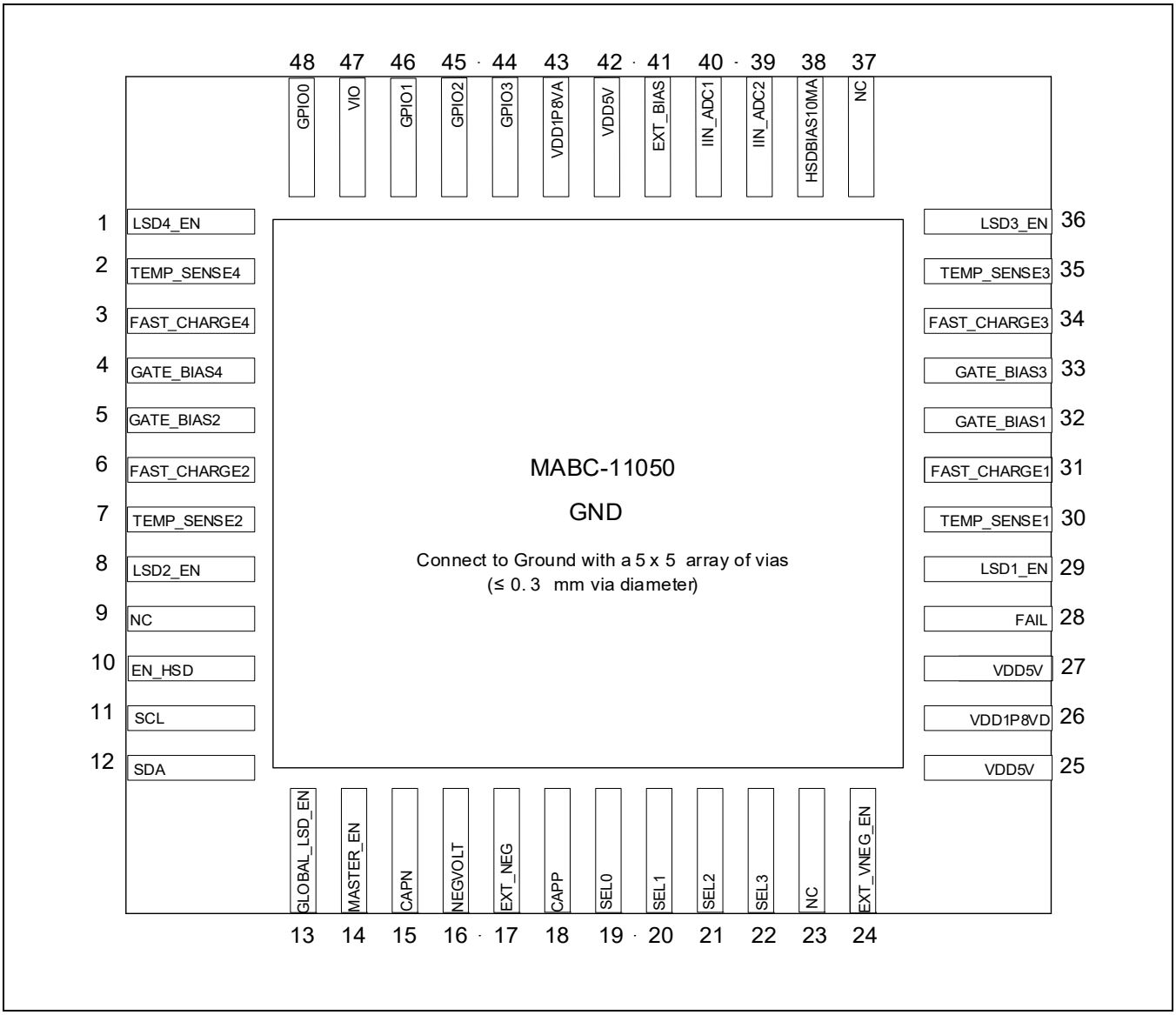


Table 2-1. Pin Configuration

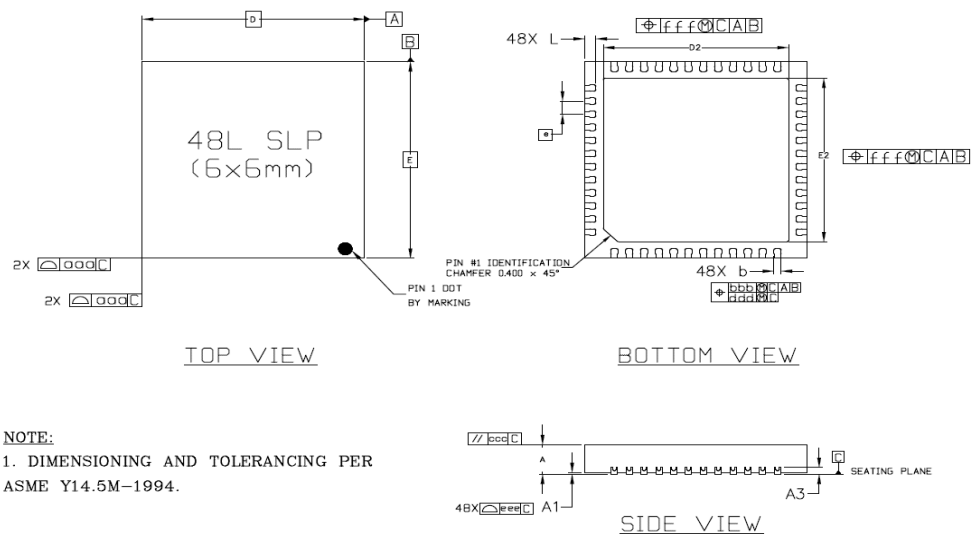
Pin Name	Pin Number	Type	Description
VDD5V	25, 27, 42	Power	5V Power Supply.
VIO	47	Power	GPIO power supply, 1.8V or 3.3V.
EXT_NEG	17	Power	External negative input power supply -6V to -4.5V.
IIN_ADC[2:1]	39, 40	Analog Input	Input to internal ADC.
EXT_BIAS	41	Analog Input	Connected to external 12.1Kohm 0.1% resistor to Ground.
CAPN	15	Analog Input	Negative terminal for Charge pump capacitor. A 10uF capacitor needed between CAPP and CAPN, 400mA
CAPP	18	Analog Input	Positive terminal for Charge pump capacitor. A 10uF capacitor needed between CAPP and CAPN, 400mA
TEMP_SENSE[4:1]	2, 35, 7, 30	Analog Input	LSD driver[4:1] positive pin for thermistor.
NEGVOLT	16	Analog Output	Negative voltage output, -5V typ. Connect to EXT_NEG if internal Charge Pump is used.
VDD1P8VA	43	Analog Output	1.8V internal supply, connect 4.7uF to Ground
VDD1P8VD	26	Analog Output	1.8V internal supply, connect 4.7uF to Ground
FAST_CHARGE[4:1]	3, 34, 6, 31	Analog Output	LSD DAC [4:1] output for fast charge output, +10mA/-6mA
GATE_BIAS[4:1]	4, 33, 5, 32	Analog Output	LSD gate driver [4:1] for gate bias output,+10mA/-10mA
HSDBIAS10mA	38	Analog Output	Predriver current bias pin, 10mA. NMOS Open Drain, cannot exceed +5VDC.
MASTER_EN	14	Digital Input	Master enable signal, internal 85K ohm pull-down. Referred to VIO. H: Normal operation. L: Device in Standby Mode.
EN_HSD	10	Digital Input	External enable pin to enable high side driver, Internal 85K ohm pull-down. Referred to VIO. H: HSD Enabled L: HSD Disabled
GLOBAL_LSD_EN	13	Digital Input	Global LSD Output Enabled, internal 60K ohm pull-up. H: LSD Drivers Enabled L: LSD Drivers Disabled
LSD[4:1]_EN	1, 36, 8, 29	Digital Input	Enable signal of LSD drivers, internal 60K ohm pull-up. This pins overrides pin GLOBAL_LSD_EN H: LSD Driver Enabled L: LSD Driver Disabled
EXT_NEG_EN	24	Digital Input	Enables internal negative supply voltage, internal 60K ohm pull-down. Referred to VIO. H: Internal negative voltage disabled, use external negative power supply to pin EXT_NEG L: Internal negative voltage enabled, internal Charge Pump is enabled.
GPIO[3:0]	44, 45, 46, 48	Digital I/O	General purpose I/O, internal 100k ohm pull up to VIO.

Table 2-1. Pin Configuration

Pin Name	Pin Number	Type	Description
Fail	28	Digital Output	Fail alarm status, Open drain, needs a 10k ohm external pull. Referred to VIO.
SCL	11	Digital Input	I2C Interface SLCK
SDA	12	Digital I/O	I2C Interface SDA
SEL[3:0]	22, 21, 20, 19	Digital Input	I2C slave address selection pin, internal 100k ohm pull-up to VDD5V.
NC	9, 23, 37	No connect	Do not connect, leave floating.

2.2 Package Outline Drawing

Figure 2-2. 6 x 6 mm PQFN48 Package Outline Drawing



Dimensional Ref.			
REF.	Min.	Nom	Max.
A	0.800	0.850	0.900
A1	0.000	—	0.050
A3	0.203 REF		
D	6.000 BSC		
E	6.000 BSC		
D2	4.050	5.000	5.050
E2	4.050	5.000	5.050
b	0.150	0.200	0.250
e	0.400 BSC		
L	0.250	0.300	0.350
Dimensional Tol.			
aaa	0.050		
bbb	0.100		
ccc	0.050		
ddd	0.050		
eee	0.080		
fff	0.050		

3.0 Functional Description

3.1 Overview

The MABC-11050 is a highly integrated Power Management Integrated Circuit (PMIC) which provides all the features necessary to safely and intelligently sequence and bias a multi-stage GaN Power Amplifier. It consists of a single High Side Driver (HSD), four Low Side Drivers (LSDs), an internal negative charge pump, four general purpose GPIO pins, an integrated temperature sensor, four external temperature sensors, and ADC.

At its core the MABC-11050 is a quad temperature-dependent low side bias generator and drivers (LSD) whose temperature-to-voltage transfer functions are user-defined. This device contains a digitized temperature sensor that addresses four independently programmable look-up tables (LUTs). The outputs of LUTs are sent on to their respective 12-bit DACs to produce four independent output voltages.

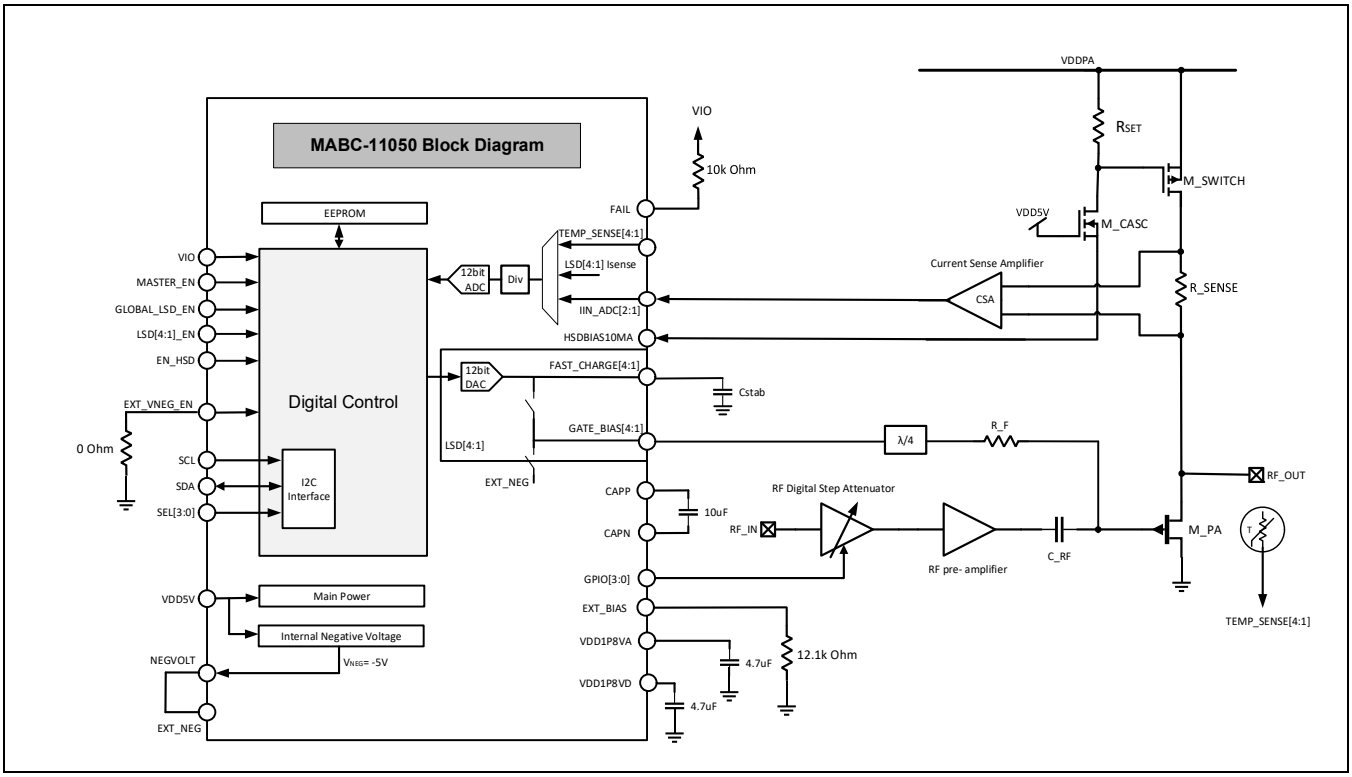
As well as providing four independent LSDs, the MABC-11050 also includes an high side driver. The HSD enables an off-chip pass gate, which can be used to correctly sequence all PA biasing.

In applications requiring rapid ON/OFF switching of the bias voltage, the MABC-11050 provides asynchronous control over its outputs. Dedicated digital input pins control analogue output switching. Each LSD can be independently controlled with its dedicated control pin or alternatively all four LSDs can be switched together by a single enable pin. When this pin is set to low then all four LSDs are turned off, and when this pin is set to high, then each LSD is controlled by its own enable control.

All aspects of the device functionality are controlled through internal registers. These registers, and the LUTs, are accessible through the I^2C-compatible interface.

The MABC-11050 can operate autonomously of the system controller, once LUT coefficients have been committed to its EEPROM's non-volatile memory. Upon power up the EEPROM content is automatically transferred to the operating memory, and the device begins to produce the required bias voltages.

Figure 3-1. Functional Block Description



3.2 Device Power up/down

3.2.1 Power up Sequence

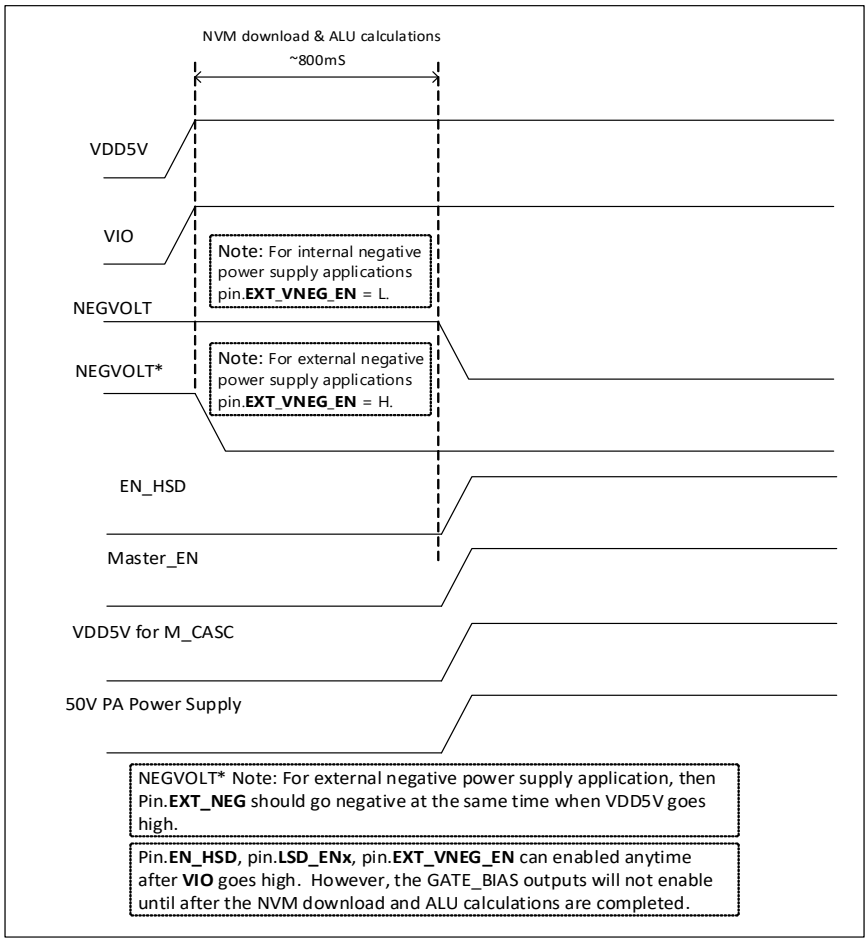
Figure 3-2 shows the recommended power up sequence

VIO should be become enabled at the same time that **VDD5V** is turned on.

If the external negative enable pin is low, the negative supply will turn on after about 800ms the **VDD5V** supplies are turned on.

If an external negative power supply applications, pin.**EXT_VNEG_EN** should be set to High and -5V should be applied to pin.**NEGVOLT** after VDD5V and VIO are enabled. The pin.**EXT_VNEG_EN** should be high and the negative supply will go negative after **VDD5V** is turned on.

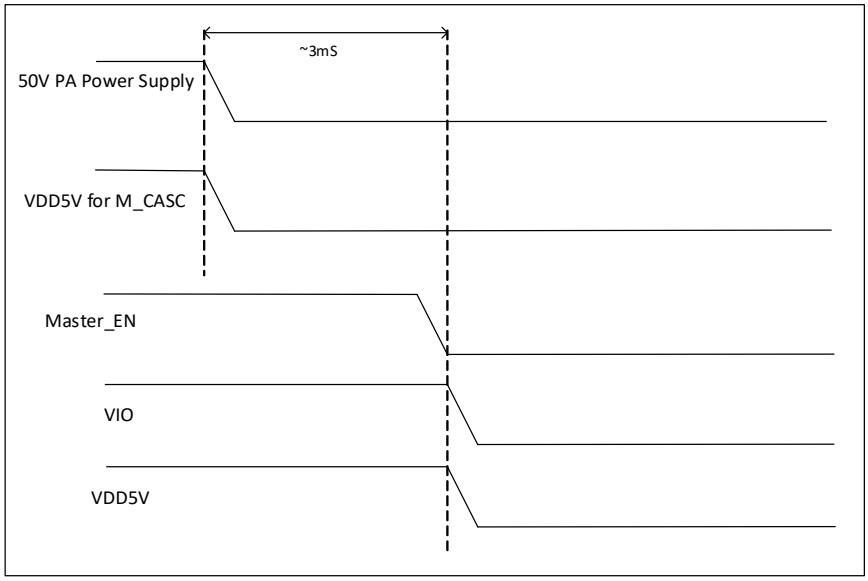
Figure 3-2. Power-up Sequencing



3.2.2 Power Down Sequence

It's recommended that the device is disabled with pin.MASTER_EN = LOW before VDD5V and VIO are turned off.

Figure 3-3. Power-down Sequencing



3.2.3 Initial Register Settings

The 50V supply for the GaN (VDD_GaN) should be turned on first, followed by the power up sequence for the MABC-11050(refer to 3.2.1) while pin.**EN_HSD** must be kept low. After power up, load the following passwords to the MABC-11050:

Password for Page0x00h: write Page 0x00h Register 0xFAh with value 0x20h;

Password for Page0x01h/02h: write Page 0x00h Register 0xFBh with value 0x19h;

Password for Page0x80h/ 0x81h: write Page 0x00h Register 0xFCh with value 0x07h;

Password for Page0x90h/91h/92h/93h: write Page 0x00h Register 0xFDh with value 0x04h;

Pin.**EN_HSD** and pin.**EN_LSD[1:4]** should be set to High to enable the LSDs.

3.2.4 Negative Charge Pump

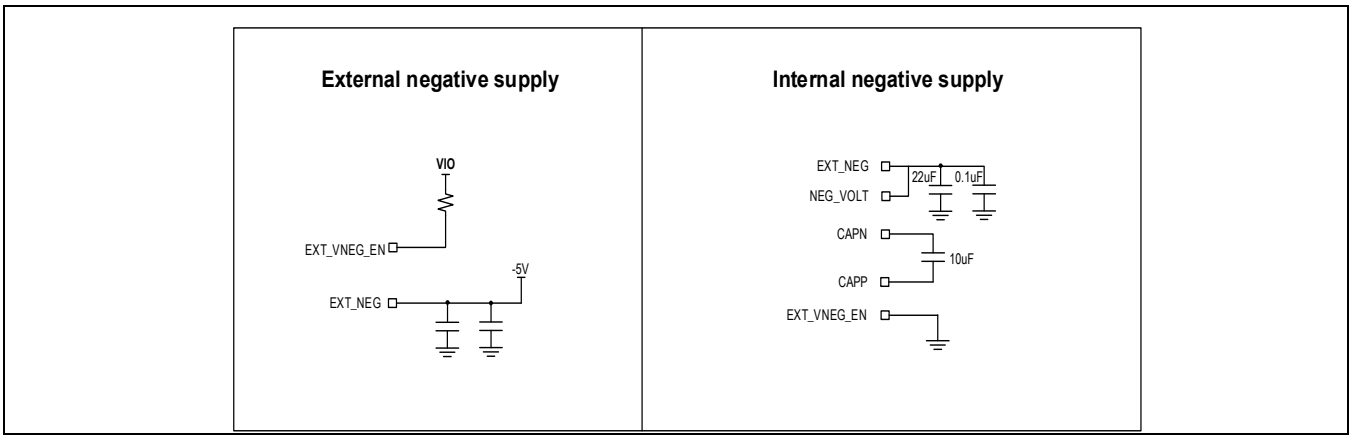
For applications where there is no negative voltage on the board, MABC-11050B includes a negative charge pump which can invert the positive supply voltage provided to **VDD5V** (the input to the charge pump). The negative pin.internal charge pump requires external bypassing of 22 uF on pin.**NEGVOLT**, and a 10uF fly-back capacitor

between **CAPN** and pin.**CAPP**. There is a dedicated external pin.**EXT_VNEG_EN**, which enables or disables the internal charge pump. In the case of using the negative charge pump, **NEGVOLT** and **EXT_NEG** need to be shorted on the PCB.

If an external negative voltage supply is to be used, VDD5V should be applied to the pin.**EXT_VNEG_EN** to disable the internal charge pump and pin.**NEGVOLT** should be connected to GND. If the external negative voltage is used as a supply for LSDs, the negative voltage should turn on at the same time when the **VDD5V** is applied. The pin.**MASTER_EN** will be pulled low at start-up, disabling the internal negative supply.

See Figure 3-4 for the application schematic.

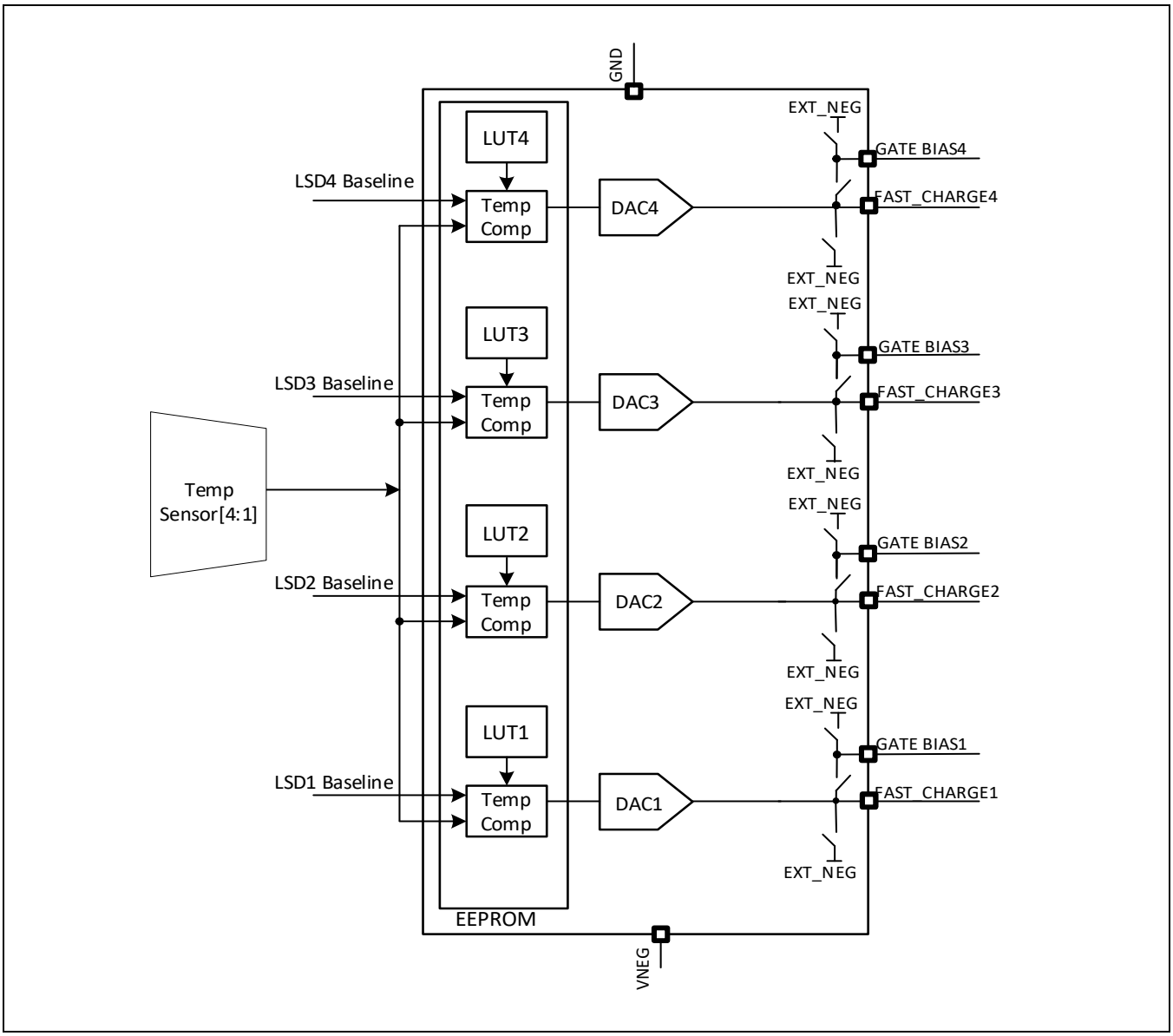
Figure 3-4. Internal and External Negative voltage supply application schematic



3.3 Low Side Driver (LSD)

The Low Side Driver is a DAC that provides a negative voltage for the gate of a GaN device. The Low Sides Drivers are compensated over temperature by means of Look-Up Tables (LUTs), which are stored in an on-chip EEPROM. The negative voltage can be an external power supply or an internal negative charge pump (refer to Section). The LSD can source up to 10mA and sink up to 6mA load with a configurable current limiting threshold.

Figure 3-5. LSD Block Diagram



3.3.1 12-bit DAC

Each LSD has a 12-bit resolution. The output range is equal to the 4*1.22*Rfb/Rext_bias where Rfb is an internal 12.4kohms, Rext_bias is an external 12.1k resistor to ground on pin.EXT_BIAS and 1.22mV is the DAC resolution. The typical output range is 0V to –5V with no resistive load.

For any input DAC word D_{in} in decimal, the ideal output voltage with no resistive load is given by the following equation:

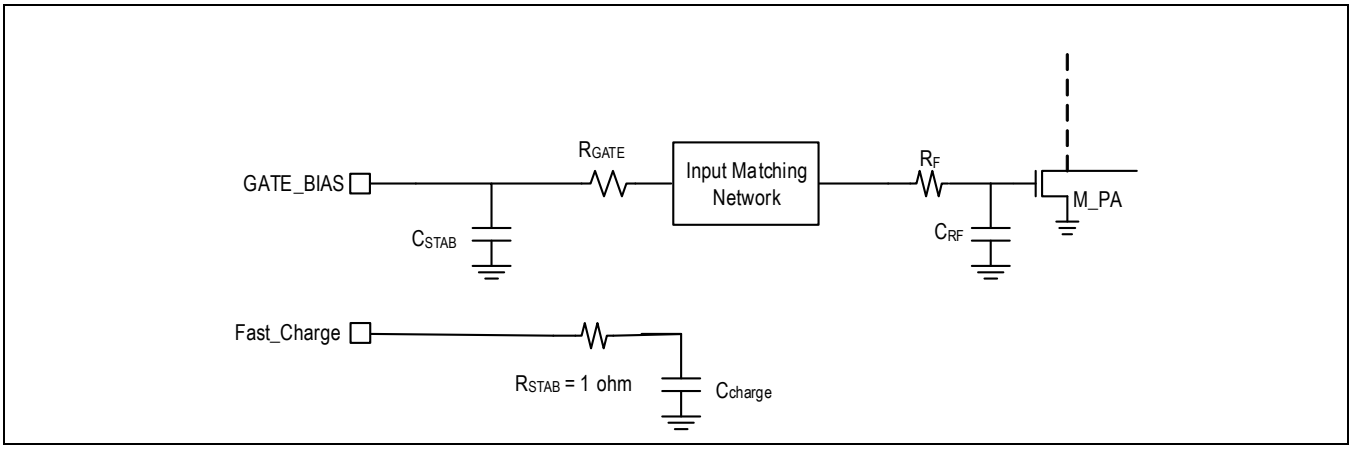
$$V_{OUT} = -5 \cdot \frac{D_{in}}{2^{12} - 1}(V)$$

The upper and lower voltage limits can be programmed by using two registers. For example, LSD1's upper limit is controlled by registers 0xAA Bits[7:0](MSB) and 0xAC Bits[7:4](LSB); LSD's bottom limit is controlled by registers 0xB0 Bits[7:0](MSB) and 0xB2 Bits[7:4](LSB)

The LSD is configured as below. The capacitor C_{STAB}, is a stability capacitor, typically around 1-10 µF. The current limiter is also set by the user.Current limit Resistor R_{GATE} should be between 5-10 Ω in value.

The specification for minimum capacitance on the **GATE_BIAS** nodes (C_{STAB}) is associated with the stability of the Low Side Driver. This capacitor also serves in decoupling the Low Side Driver from the RF gate. The default option is to open the integrated feedback resistor loop and use an external feedback resistor. This is done in order to allow the loop to correct the IR drop on resistor R_{GATE}.

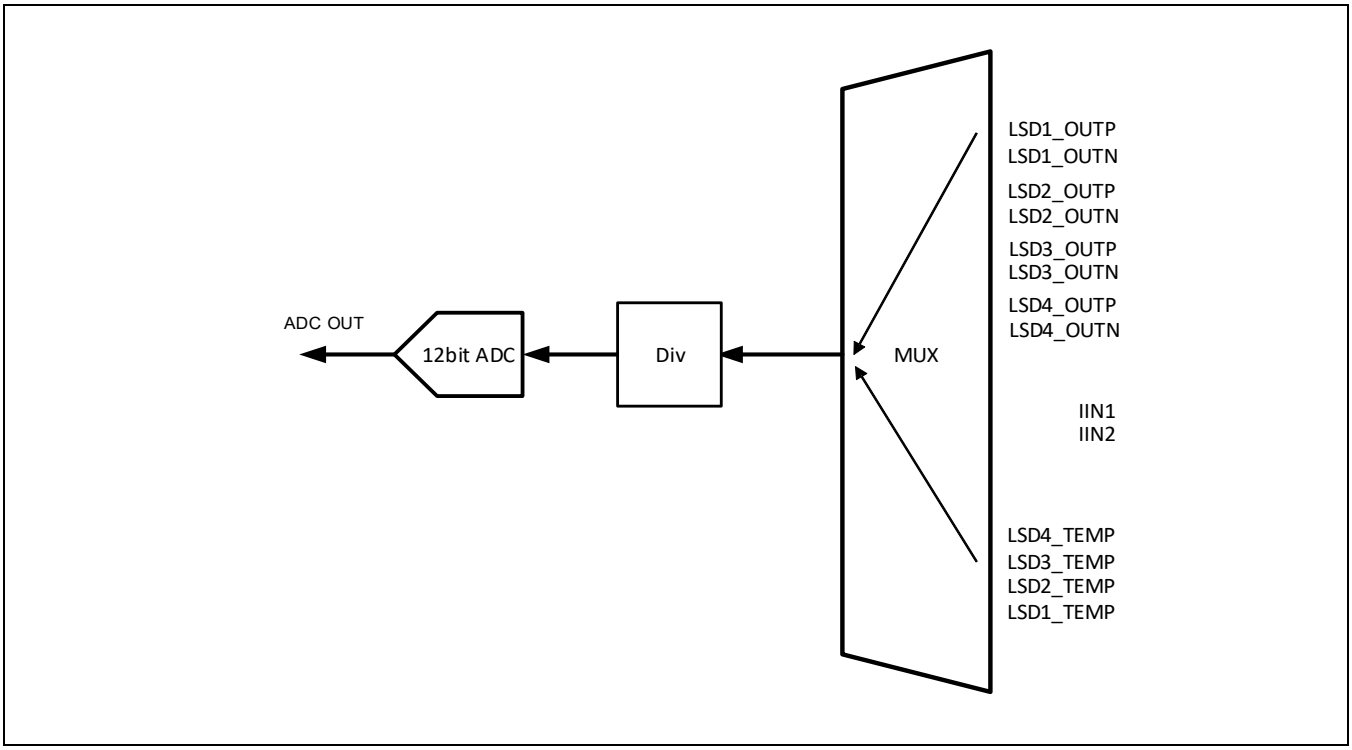
Figure 3-6. LSD_DAC_OUT Application Schematic



3.3.2 12-bit ADC

The device integrates a 12-bit SAR ADC which inputs are configurable by the I^2C. The ADC allows monitoring of the internal temperature sensor, 2 external input pins.**IIN_ADC[2:1]**, all four low side driver gate-currents and all four thermistor input pins.**TEMP_SENSE[4:1]**. The cycling mux has a frequency at 0.75ms.

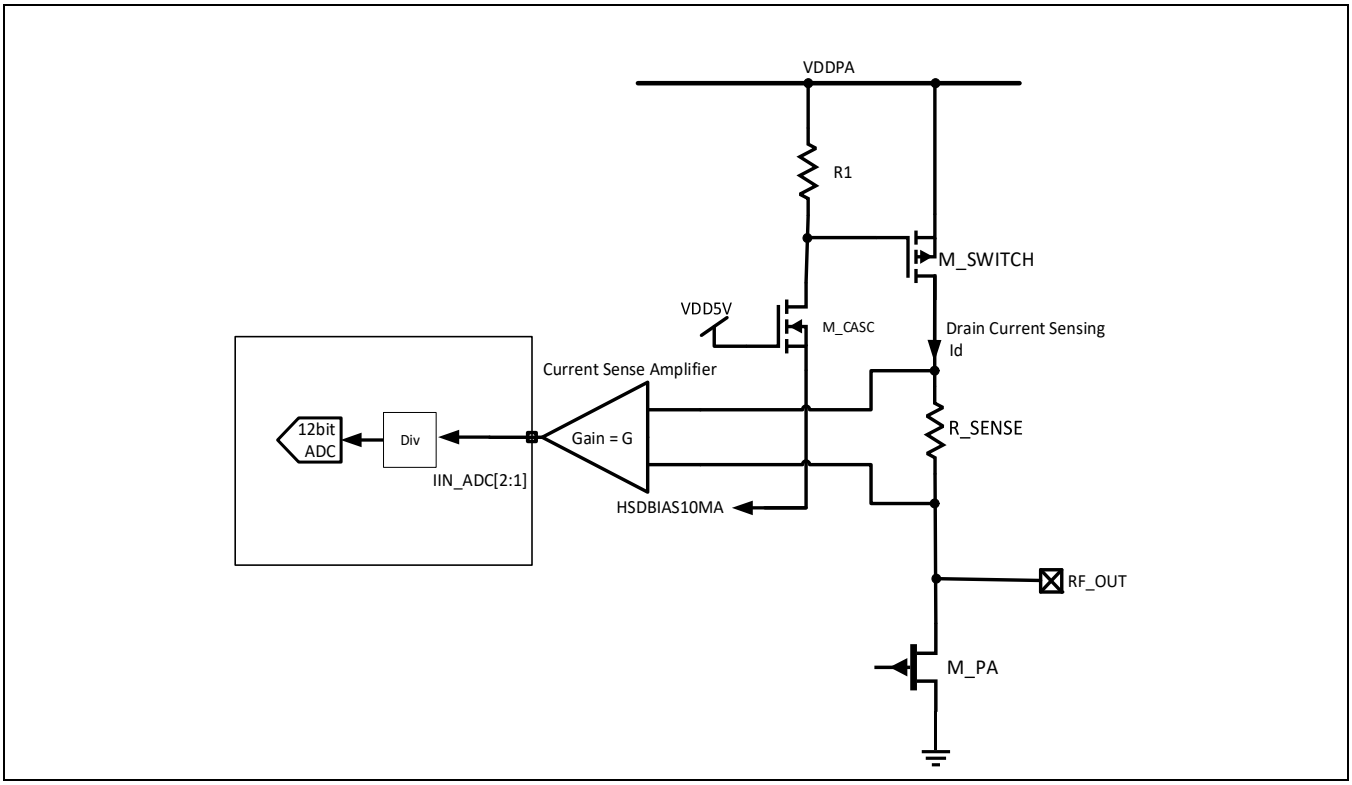
Figure 3-7. ADC Block Diagram



3.3.2.1 LSD Drain Current Sensing Using ADC

The drain current I_d comes out from M_Switch and fed to the 12-bit ADC. A drain current going through R_sense and current sense amplifier to generate the 12bits ADC code. The user needs to ensure that the voltage range at the output of the current-sense amplifier is within the specifications for the ADC input range **IIN_ADC1** and **IIN_ADC2**. This range corresponds to the range of currents, which are expected to be sensed. The voltage range for ADC is 0 to 1V, so I_d*R_Sense*G should not be larger than 1V. The resolution for 12-bit ADC is 2.44mV/LSB. The gain for CSA should be 0.5.

Figure 3-8. Drain Current Sensing Block Diagram

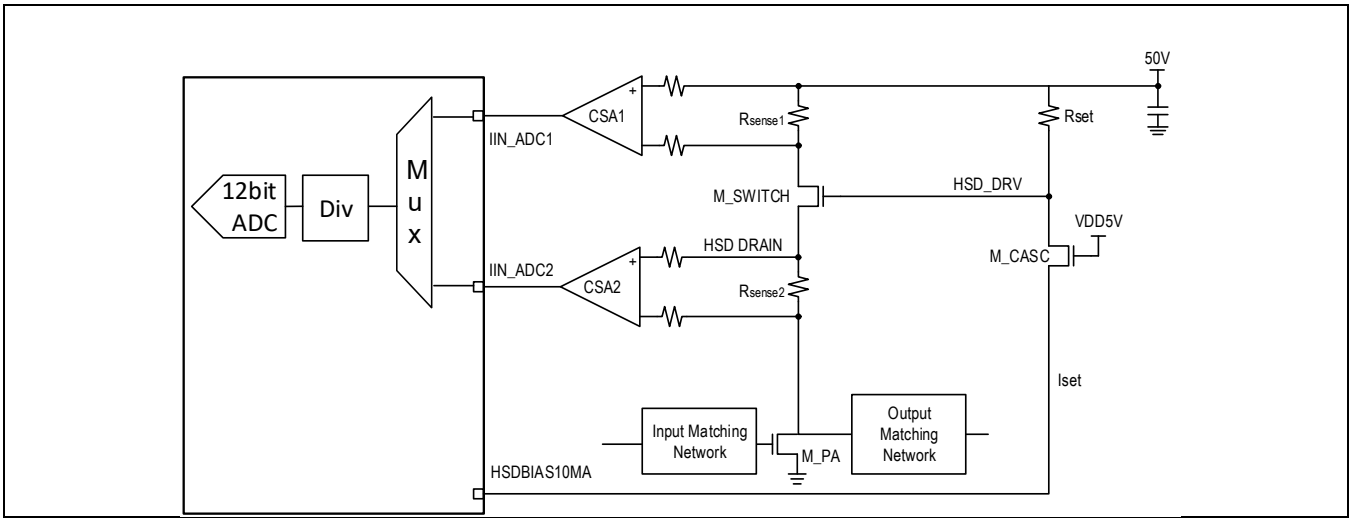


3.3.2.2 LSD Drain Current Sensing Example

A source-sense resistor, R_{sense2}, is placed on the board on the drain of M_SWITCH. This allows the monitoring of the PA current of the output stage, M_PA. An external current-sense amplifier is used to provide a voltage into the IC, which is fed to the ADC and converted to digital signal. A secondary resistor, R_{sense1}, is be placed at the drain of the first two amplifier stages to provide a more accurate current reading.(See Figure 3-9)

There is flexibility in the selection of the current-sense amplifiers and the current-sense resistors. The user needs to ensure that the voltage range at the output of the current-sense amplifier is within the specifications for the ADC input range **IIN_ADC1** and **IIN_ADC2**. This range corresponds to the range of currents, which are expected to be sensed.

Figure 3-9. LSD Drain Current Sensing Schematic



Example of LSD Current-Sense Resistors & Current-Sense Amplifiers

In the table Table 3-1, an example is given that includes a 0.1Ω sense resistor with a maximum drain current of 16 A, and a minimum drain current of 1A. Then the input range of current sense amplifier is Id * R_{sense} from 0.1V to 1.6V. And the gain required from current sense amplifier should be 0.5. The ADC voltage range is from 0V to 1V. As ADC is 12-bit, the voltage resolution is 2.44mV/LSB.

Table 3-1. Example Calculations for HSD Current-Sense Resistors and Current-Sense Amplifiers

Parameter	Variable	Equation	Value	Unit
Id_{MAX}	Id_{MAX}	--	16.00	A
Id_{MIN}	Id_{MIN}	--	1.00	A
Resistor	R_{sense}	--	0.10	Ω
CSA Input voltage for minimum current	$V_{MIN,CSA}$	Id_{MIN}*R_{sense}	0.10	V
CSA Input voltage for maximum current	$V_{MAX,CSA}$	Id_{MAX}*R_{sense}	1.60	v
CSA input voltage range	$V_{range,CSA}$	$V_{MAX,CSA}$-$V_{MIN,CSA}$	1.50	V
Gain required from CSA	$Gain_{CSA}$	$V_{range,ADC}$ / $V_{range,CSA}$	0.500	V/V
ADC minimum voltage	$V_{MIN,ADC}$	--	0	V
ADC maximum voltage	$V_{MAX,ADC}$	--	1.0	V
ADC input voltage range	$V_{range,ADC}$	$V_{MAX,ADC}$ - $V_{MIN,ADC}$	1.0	V
12-bit ADC - voltage resolution	V_{res}	($V_{range,ADC}$ / 2^12)*1000	2.44	mV
Recommend ADC minimum voltage	V_{MIN,ADC_r}	--	0.125	V
Recommend ADC maximum voltage	V_{MAX,ADC_r}	--	0.875	V

3.3.2.3 LSD Gate current sensing Using ADC

The gate current is sensed by integrated current sensors and fed to the 12-bit ADC via the multiplexer. A current reading is provided to the system in the range of –6 to 10 mA.

There are two currents stored for each measurement: the currents in the PMOS and the currents in the NMOS. The output current is the current in the PMOS minus the current in the NMOS. There are four channels of the LSD gate drive currents that are measured. The currents, which are 12 bits, are stored in two registers where the 8 most significant bits are measured in one register, and the four least significant bits are stored in another register.

For example, the 12 bits for the LSD1 PMOS are stored in the 2 registers named CHNL1_MSB and CHNL1_LSB. The 12 bits for the LSD1 NMOS are stored in the 2 registers named CHNL5_MSB and CHNL5_LSB. The total current sent to the LSD1 gate is the difference between the current stored in the 12-bit PMOS registers (I_{PMOS}) and the current stored in the 12-bit NMOS registers (I_{NMOS}).

The accurate current calculation takes into account an adjustment for the internal DAC current, the formula to calculate I_{load} is shown in Figure 3-10.

Figure 3-10. Formula for Calculating Gate Currents

$$I_{load}[mA] = I_{PMOS} - I_{NMOS}$$

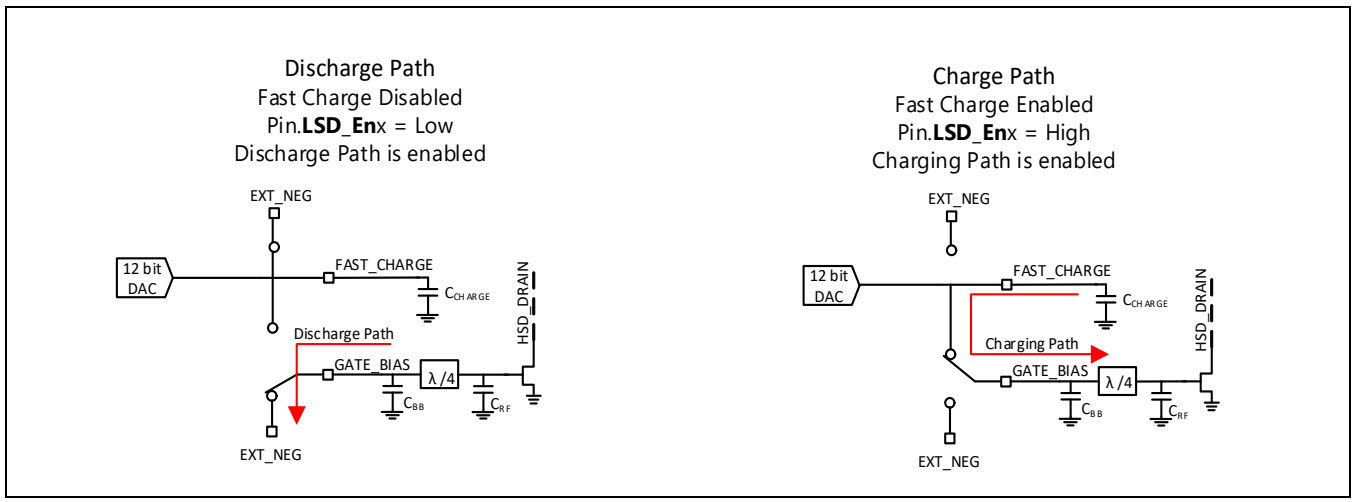
$$I_{NMOS} = -ADC\ Code \times 0.0311 - 1.43$$

$$I_{PMOS} = ADC\ Code \times 0.0311 - 1.45$$

3.3.3 Fast Charge

In 5G mode fast switching ON and OFF is required. In order to overcome this, we are using the circuit of Figure 3-11. The “FAST Charge Control” switches must be open before making the new connection”.

Figure 3-11. FAST_CHARGE circuit diagran



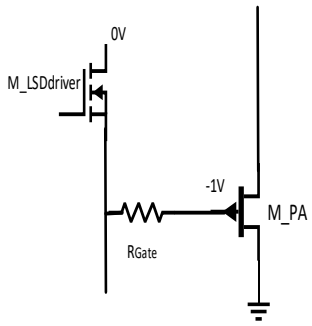
When the **FAST_CHARGE** circuit is disabled, the gate is connected to the negative supply, while the capacitor C_{BB} connected to node **GATE_BIAS** is charged according to the DAC input control. Once the circuit is enabled, the capacitor C_{CHARGE} quickly charges the capacitor C_{BB}, which provides the voltage to the gate. This is done due to the high capacitance ratio between C_{CHARGE} and C_{BB}. Note that the FAST_Charge control is internally generated and goes between 0V and 1.8V.

3.3.4 LSD Headroom

Resistor R_{GATE} should be between 5-10 Ω in value. R_{GATE} should be designed to allow for some gate voltage headroom (Figure 3-12).

- Example 1: With 10mA current and 4.99Ω R_{gate}, the voltage on gate resistor is 0.499V. As V_{gate} is 1V. There will be 0.501V on non-gate side of R_{gate}. With 0.4V max LSD headroom. The margin for headroom is 0.101V.
- Example 2: With 10mA current and 5.6Ω R_{gate}, the voltage on gate resistor is 0.56V. As V_{gate} is 1V. There will be 0.44V on non-gate side of R_{gate}. With 0.4V max LSD headroom. The margin for headroom is 0.04V.

Figure 3-12. LSD Headroom with 100 mA Sourced



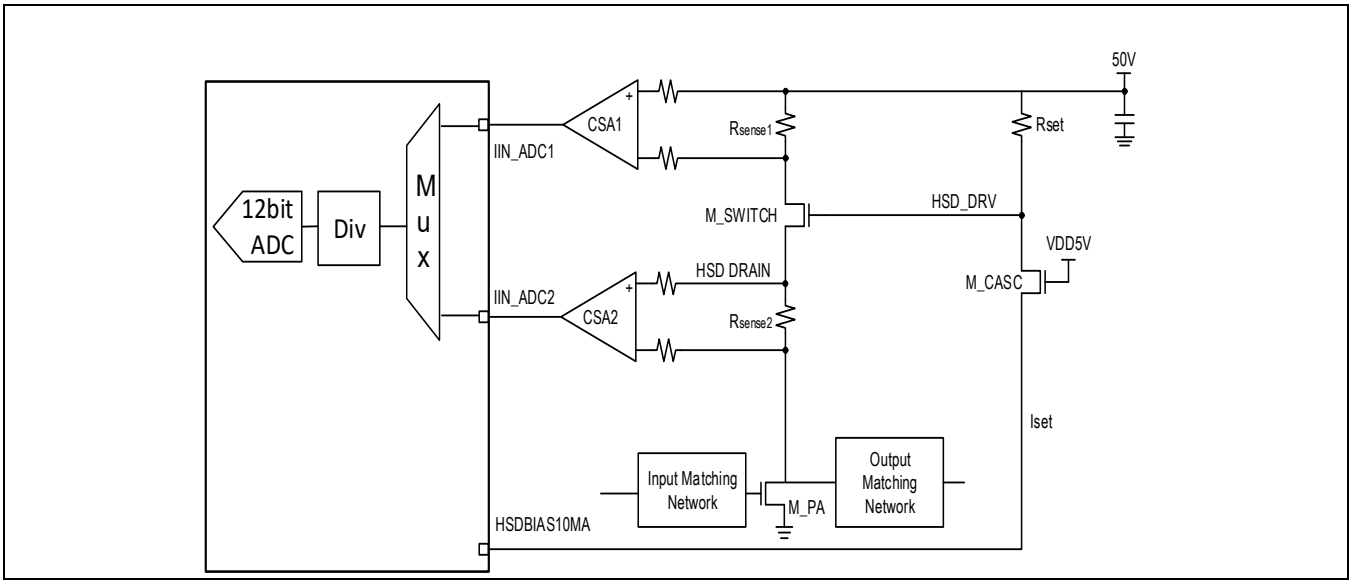
3.4 High Side Driver

EN_HSD is used to enable to high side driver. There is an internal pull-down for pin.**EN_HSD**, so that the high side driver is disabled during start-up.

The HSD provides the control for an external high voltage Pass Gate Power FET (M_SWITCH), typically used to connect the high voltage supply to the Power Amplifier stages. In addition to the pass gate, the MABC-11050 also requires an off chip resistor and FET M_CASC to protect it from the high drain voltage. To turn on the external pass gate FET, the HSD turns on a programmable current source I_{SET} at **HSDBIAS10MA**, which pulls a current through R_{SET} (see Figure 3-13), such that the **HSD_DRV** voltage is dropped by I_{SET}*R_{SET}. For example, if I_{SET} is 10mA and R_{SET} is 1k ohms leading to a voltage drop across R_{SET} of 10 V to turn on the pass gate FET(M_SWITCH). With the 10V drop across R_{SET} the voltage at the **HSD_DRV** location becomes 40V (a 10 V drop from 50V). Note that the resistor selection /required voltage drop is application specific.

When pin.**EN_HSD** is pulled high, a 10 mA current will be drawn from pin.**HSDBIAS10MA** and will turn on the M_CASC after t_{SWON} (Page 00h, Address 80h[7:4]). After the M_CASC is on, LSD will then provide the voltages from the internal LUT, based on the multiple temperature inputs. Setting the pin.**EN_HSD** down will turn the GaN device off. After a delay of t_{SWOFF} (Page 00h, Address 80h[3:0]), the M2 will turn off.

Figure 3-13. High Side Driver Schematic



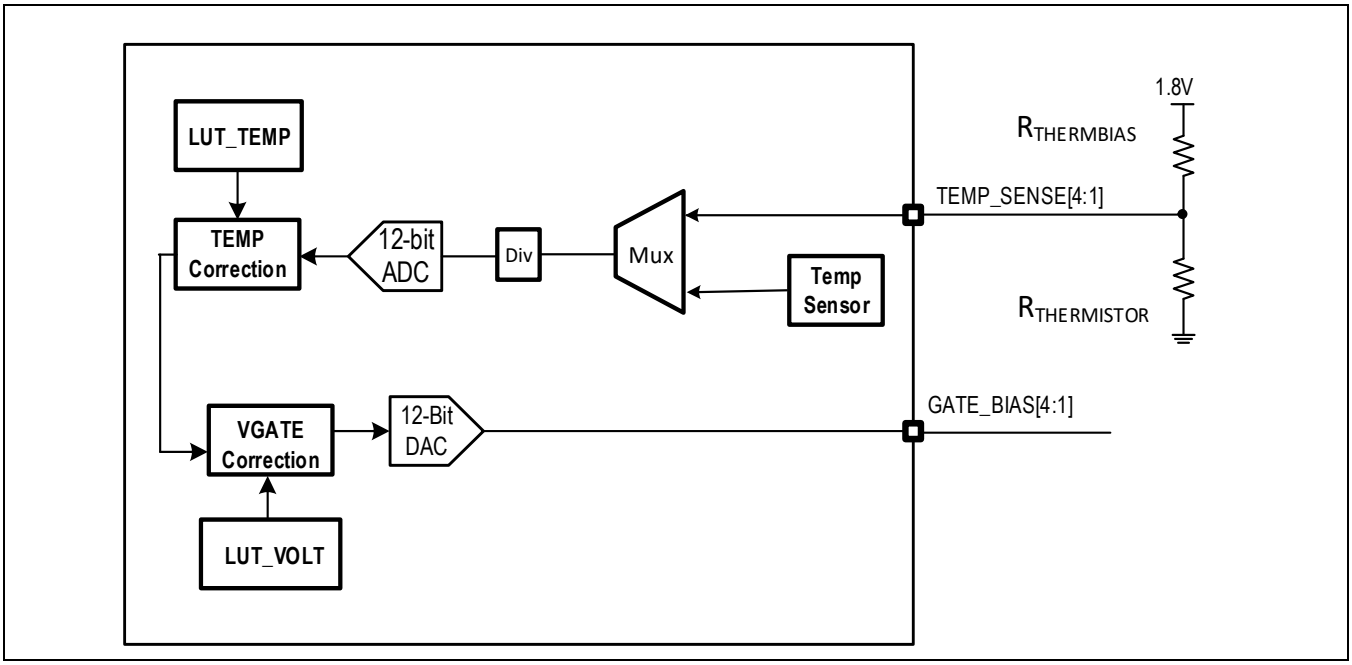
3.5 Look up Table

The current going to the power amplifier has to be carefully sustain over temperature. For this compensation, the MABC-11050 features two Look Up Tables that compensates for nonlinearities in the external thermistor used and the gate current going to the Power Amplifier. The LSD_DAC_OUT temperature compensation using an external thermistor will be done in two steps as follows:

1. Temperature LUT, reg.LUT_TEMP: Compensates for the external thermistor or internal temperature sensor nonlinearities .
2. Gate Bias LUT, reg.LUT_VOLT: Provides a current vs. temperature profile to the power amplifier, user defined.

Figure 3-14 shows the temperature compensation circuitry using an external thermistor.

Figure 3-14. LSD_DAC_OUT Temperature Compensation using an external thermistor



3.5.1 Look Up Table for Temperature

The temperature linearizion uses the 256 words stored in the TEMP LUT (Register page 0x80h and 0x81h). For example, given the temperature range from –40°C to 120°C with 256 steps, the step size is 0.625°C. When using an external thermistor, the ADC codes must be re-defined over temperature by LSDx_TEMP output voltage and mapped to the LUT_TEMP having a resolution up to 0.625°C/ADC code. The temperature readings are taken either from an integrated temperature sensor or an external thermistor placed close to the power amplifier device(s).

Two different methods are specified for temperature sensing and readout. In both cases, a 12-bit temperature reading is obtained based on a total range of 160^{o}C, -40^{o}C to +120^{o}C, 0.04^{o}C steps. Note that, in the case of the external thermistor, the temperature calibration is done using 8 bits, i.e. every 256 steps, while a linear interpolation is performed between the 1/256 steps. The MABC-11050 will monitor the four pins.**LSD_TEMP[4:1]** and continue to update each temperature reading from the temperature calibration registers for each LSD temperature sensor based on the voltage reading.

Note: If no thermistor is used, pins.**TEMP_SENSE[4:1]** should be tied to **VIO**. This would prevent over temperature faults from occurring.

The temperature BASELINE at which extracted LUT_TEMP is defined in LUT_TEMP_BS_MSB and LUT_TEMP_BS_LSB as 12bit data from -40C to 120C. LSDx_TS_BS_MSB/LSB give the ADC reading of LSDx_TEMP pin as the BASE value. LUT_TEMP_BS_ADDRESS give the address in the LUT_TEMP that BASE is stored. The overall transfer function is stored in the LUT as a set of unsigned 12-bit increments from the base value, that is, each LUT location stores the value of the decrement Δ1 per 0.625C.

3.5.2 Look Up Table for Voltage

The gate voltage temperature calibration uses only the 6 most significant bits of the 12-bit temperature reading. which is typically defined for a temperature range from -40^{o}C to 120^{o}C, therefore the step is typically 2.5C and a total of 64 steps within the voltage look-up table. This range can be adjusted, according to the users' needs, and the MABC-11050 is functional and operational within the required range of the use case. Between each 2.5C step within the VOLT LUT, a linear interpolation is applied using the remaining 6 bits of the temperature reading. The linear interpolation step is 0.04^{o}C.

3.5.2.1 Offset voltage correction

The calibration procedure described above is using look-up values from VOLT LUT, which have been measured over temperature and are assumed to be the same for all devices of the same type. When a new device is used in the system, these look-up values need updating. Also each GaN device needs to be calibrated for V_{th} offset. This is one more look-up value, unique for each GaN device, which is added to the gate voltage correction values of its family.

3.5.2.2 Register Settings to use LUT Voltage

- Enable look up tables by writing Page0x02h, Register0x08h Bit[2] with Value 1.
- Load the desired settings to each page and register.
- Terminate NVM control and reflect the changes by writing Page0x02h, Register0x08h Bit[2] with Value 0.

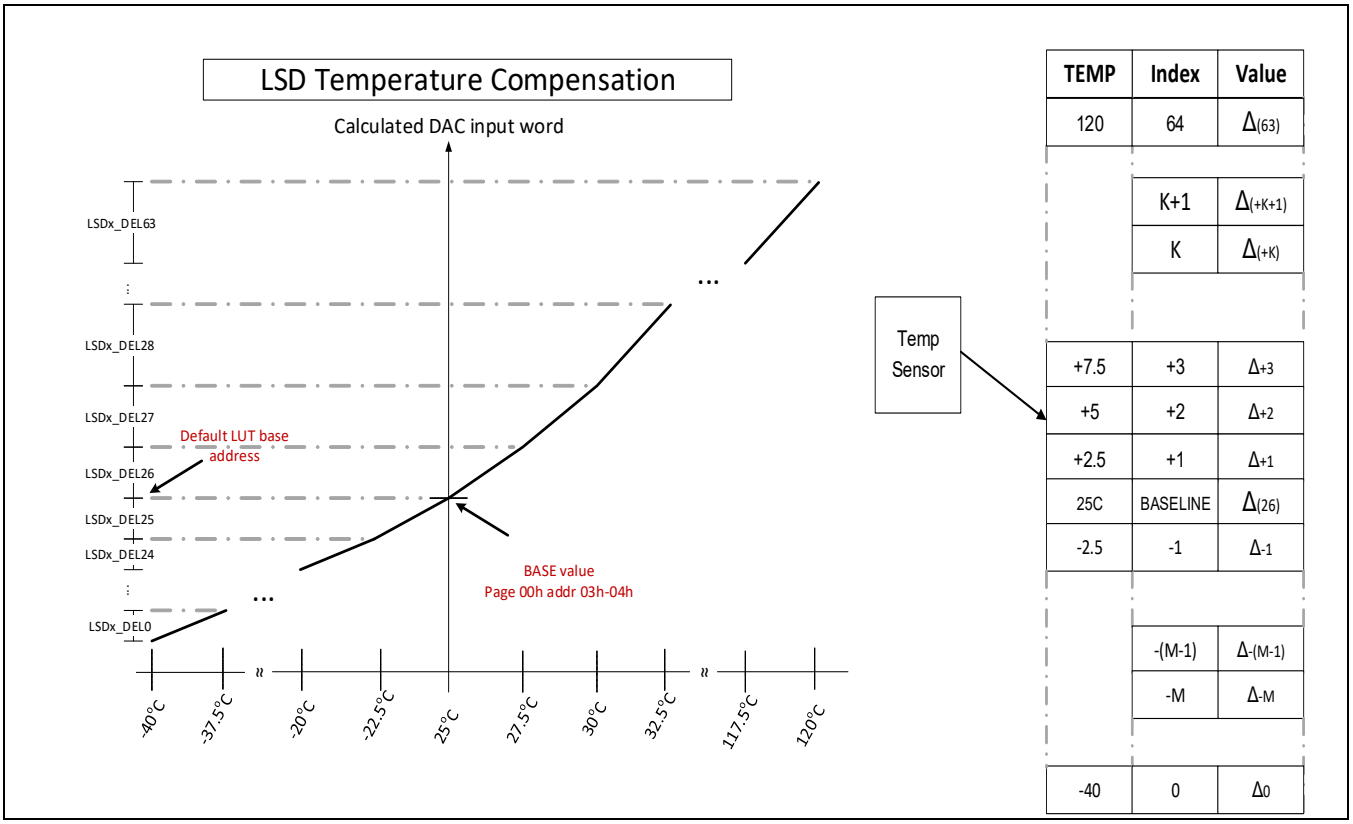
3.5.2.3 LUT Voltage Calculation

In order to minimize the storage requirements, MABC-11050 LUTs are indexed in 2.5°C increments. Also, the stored values are only the increments, or first derivatives (Δs) of the modeled transfer function. The internal ALU reconstructs the original transfer function by integrating the coefficients stored in the LUTs. The errors due to the coarseness of the temperature quantization are significantly reduced through the use of linear interpolation, which is also implemented in the ALU. ALU output will be limited to{000, FFF}. Consider the example shown in Figure 3-15 The target output vs temperature is shown in the top graph. VDACx is a smooth, monotonic function with, ideally, infinite precision. The LUT stores only the increments, or the rise, within each 2.5°C interval.

In order to recreate the original transfer function, the series of increments must be summed together and added to the constant BASE value. This process must also be referenced to the common temperature point. This reference temperature is called BASELINE and is defined in TS_PTAT_BS_TEMP<11:0> and LUT_TEMP_BS_TEMP<11:0> depends on internal (TS_PTAT, TS_VBG) or external temperature sensor (TS1/2/3/4)used.

MABC-11050 has VOLT LUTs for each LSD driver defined in page 90h/91h/92h/93h. The VOLT LUTs start from the BASE address and extend to 64 steps. Each step of data shows the differential DAC code between previous temperature and current temperature. The base voltage value in hexadecimal is calculated by: Dec to Hex[Gate Voltage/1.22mV];The base temp value in hexadecimal is calculated by: Dec to Hex[(Temp(°C)+40°C) /0.625°C]. For more details, please contact MACOM team.

Figure 3-15. LUT Voltage Table



3.6 Addition features

3.6.1 EEPROM Programming Procedure

The following are the instructions to program the EEPROM.

1. Enable Look up table: write Page 0x02h Register 0x08h with value 0x04h.
2. Clear the trim and the test bits: write Page 0x00h Register 0x7Fh with value 0x00h; write Page 0x01h Register 0x00h with value 0x00h; write Page 0x01h Register 0x01h with value 0x00h; write Page 0x01h Register 0x02h with value 0x00h;
3. Write password to enable each page: write Page 0x00h Register 0xFAh with value 0x20h; write Page 0x00h Register 0xFBh with value 0x19h; write Page 0x00h Register 0xFCh with value 0x07h; write Page 0x00h Register 0xFDh with value 0x04h;
4. Enable look up table: write Page 0x02h Register 08h with value 0x04h.
5. Write the desired setting to each page and registers.
6. To permanently program in the settings: write Page 0x02h Register 0x03h with value 0xFFh; write Page 0x02h Register 0x06h with value 0x01h; write Page 0x02h Register 0x08h with value 0x00h

3.6.2 GPIO pins

There are four general purpose CMOS output pins, **GPIO[3:0]**, available to the user. They can be used to adjust the attenuation setting of a Digital Step Attenuator (DSA), which can be used to control the gain in a power amplifier lineup or they can be used in order to set the phase of a digital phase shifter. Since the step attenuator is set during initial calibration, the GPIO signal can be treated as low frequency, such as 1 KHz.

The status of the GPIO pins will be controlled by the internal GPIO_CTRL0 register.

The logic level of these pins is determined by pin **VIO**. Depending on the voltage provided at pin **VIO**, the logic level can be between 1.8 and 3.3V.

3.6.3 Internal Temperature Sensor

There is an internal temperature sensor available. There is a set alarm threshold value (“TS_PTAT_OT_S_THD”) and reset alarm threshold value (“TS_PTAT_OT_R_THD”) based on the internal temperature sensor. If an alarm does assert, the faults can be can also be masked (disabled) using “ALARM_MASK2” (Page 02h, Address A5h).

Set bit [4] to 1 to mask “TS_PTAT_Alarm”.

3.6.4 External Temperature Sensors

External temperature sensor pins (**TEMP_SENSE[4:1]**) are available for users to place thermistors to monitor external temperature. The threshold set value (“TEMP[4:1]_OT_THD”) and reset value (“TEMP[4:1]_OT_R_THD”) must be programmed into the chip based on the thermistor characteristics. If the temperature exceeds the threshold temperature, the over-temperature alarm asserts (sets). If the temperature falls below the reset temperature threshold, the alarm de-asserts (resets).

If an alarm does assert, the faults can be can also be masked (disabled) using “ALARM_MASK2” (Page 02h, Address A5h).:

- Set bit [3] to 1 to mask “LSD4_TS_Alarm”.
- Set bit [2] to 1 to mask “LSD3_TS_Alarm”.
- Set bit [1] to 1 to mask “LSD2_TS_Alarm”.
- Set bit [0] to 1 to mask “LSD1_TS_Alarm”.

3.6.5 Fail Alert

A fail alert mechanism provides an output to alert the system that there are certain operating conditions found to be outside the defined acceptable range. There are two types of alarms, the real-time and latched alarm. The difference between the alarms is a reset is required to clear the latch alarm. The real time alarm outputs are used so that faults are captured as they occur. Latched alarms assert when an alarm event occurs and must be reset to check if the alarm event is still occurring. Below is a summary of the alarm types on the MABC-11050

The **FAIL** pin output is active low to indicate an alarm condition. This alert can be used by the system in order to turn off the power amplifier and protect it from being damaged. The polarity of the alarm bit can be changed by using the “Fail_flip_polar” register bit (Page 00h, Address A2h[4]). If this bit is change to “1”, the Fail alarm output will become active high to indicate an alarm condition.

The **FAIL** pin is open drain, and is internally pulled down so that the FAIL pin is low at turn-on. The “Fail_out_cmos” register bit (**Page 00h, Address A2h[5**]) can be used to convert this pin from open-drain, “0”, to a CMOS output < “1”. When the **FAIL** pin is open-drain, a 4.7k external pull-up resistor to VIO is required but a CMOS output does not require an external pull up resistor.

The “FAIL_PIN_MODE” register bit (Page 00h, Address A2h[0]) controls the behavior of the **FAIL** pin between. Trigger lock and interrupt mode. The duration that the **FAIL** pin is indicates an alarm condition is defined by “Fail_interrupt_duration” **(Page 00h, Register A2h[3:1]**) and can be set between 12 and 84 clock cycles.

“alarm_clear” is used to clear all the latched alarms in the following registers, “TEMP_ALARM”, “ALARM0”, and “ALARM1”, by setting this bit “1” and then back to “0

- “ALARM_MASK0” is used to mask (disable) all the alarm statuses in the “ALARM0” register (Page 00h, reg.A3h).
- “ALARM_MASK1” is used to mask (disable) all the alarm statuses in the “ALARM1” register(Page 00h, reg.A4h).
- “ALARM_MASK2” is used to mask (disable) all the alarm statuses in the “TEMP_ALARM” register(Page 00h, reg.A5h).
- “ALARM_MASK3” is used to mask (disable) all the alarm statuses in the “TEMP_ALARM” register(Page 00h, reg.A6h).

The logic block diagram of the fail circuitry can be found in Figure 3-16.

3.6.5.1 Drain Current Alarms

The drain current limit is predefined. If the drain current seen at **IIN_ADC1** or **IIN_ADC2** exceeds the current limit, the alarm bit will assert.

- “iin1_cl_lt”, Page 02h, Address 3Fh[7], is associated to the **IIN_ADC1** pin.
- “iin2_cl_lt”, Page 02h, Address 3Fh[6], is associated to the **IIN_ADC2** pin.

3.6.5.2 Gate Current Alarms

The gate current limit is predefined. If the gate current seen at the GATE_BIAS pin exceeds the predefined limit, the alarm bit will assert.

- “lsd1_cl_rt”, Page 02h, Address 40h[6], is associated to the **GATE_BIAS1** pin.
- “lsd2_cl_rt”, Page 02h, Address 40h[5], is associated to the **GATE_BIAS2** pin.

- “lsd3_cl_rt”, Page 02h, Address 40h[4], is associated to the **GATE_BIAS3** pin.
- “lsd4_cl_rt”, Page 02h, Address 40h[3], is associated to the **GATE_BIAS4** pin.

3.6.5.2.1 Voltage Alarms

There are four under-voltage alarms addressing all four voltage supply pins, **V_NEG**, **VDD5A**, **VDD1P8VA**, and **VDD1P8VD**. If the predefined threshold is less negative for **V_NEG** or less positive for the other three supplies, the resulting fault condition will disable the **GATE_BIAS** and HSD. There is a predefined amount of hysteresis and low pass filtering to prevent false triggering of the fault condition.

V_NEG is monitored by the alarm bit “neg_uv_rt”. This alarm bit will go high,“1”, when V_NEG is less negative than the voltage threshold defined by “vneg_rdy_vth”.

VDD5A is monitored by “undervoltage_alarm_rt”. This alarm bit will go high,“1”, when VDD5A is less positive than the voltage threshold defined by “UV_alarm_vth”.

VDD1P8VA is monitored by the alarm bit “v1p8a_uv_rt”. This alarm bit will go high,“1”, when VDD1P8VA is less positive than 1.44V.

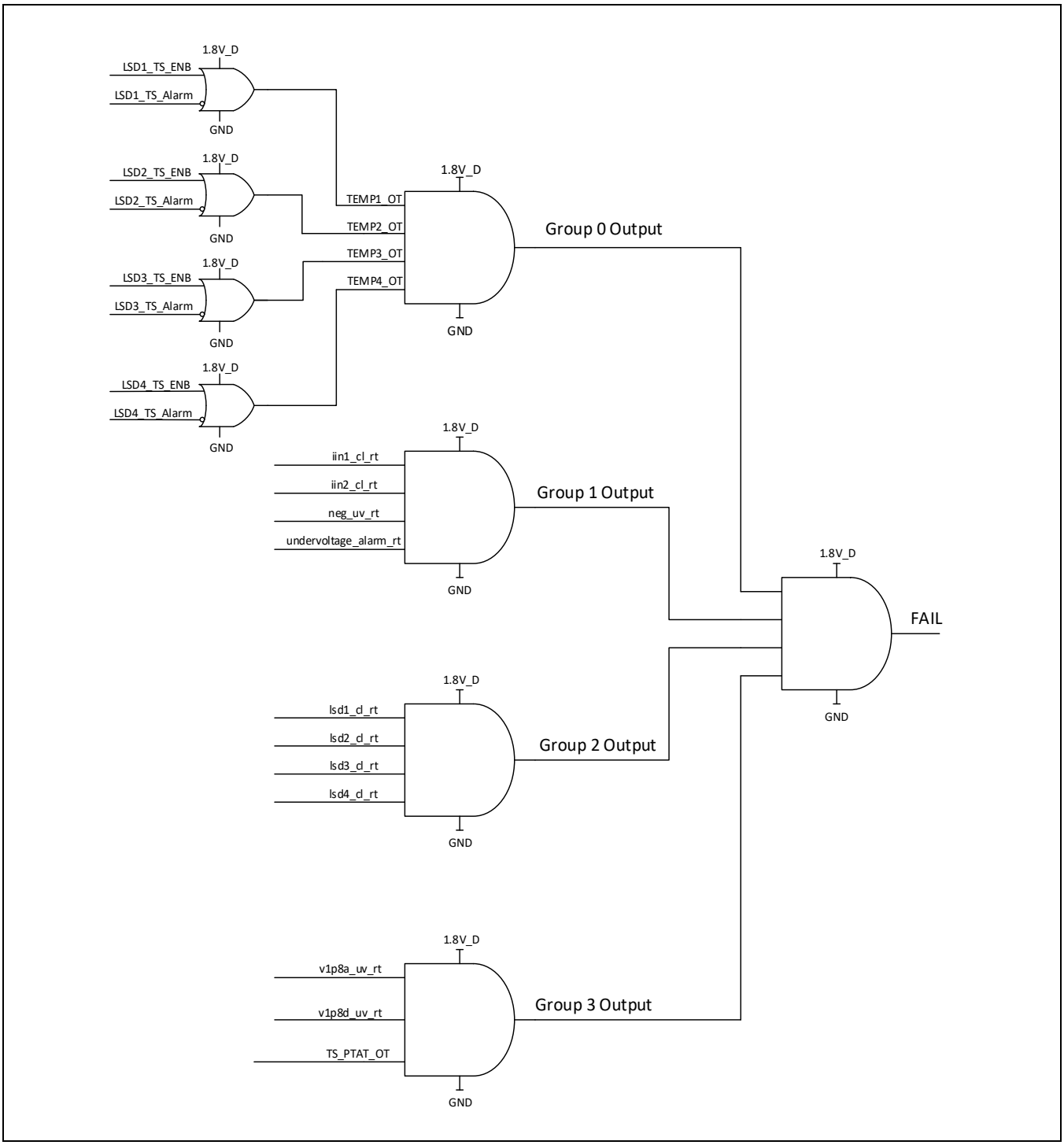
VDD1P8VD is monitored by the alarm bit “v1p8d_uv_rt”. The alarm bit will go high,“1”, when VDD1P8VD is less positive than 1.44V.

3.6.5.3 Thermal Shutdown

The thermal shutdown circuitry uses a BJT on the die. VBE on the BJT is compared with predefined voltages to sense if the temperature has reached the shutdown thresholds of 130°C, 140°C, or 150°C. If the temperature has reached the selected thermal shutdown temperature, the low side drivers (LSDs) and high side driver (HSD) will be disabled.

There is an option to disable thermal shutdown for HTOL testing. “OT_Shutdown_Threshold” by setting both bits in page 00h, address 93h[5:4]) = 1.

Figure 3-16. Fail Circuitry Logic



3.7 Digital Interface

Using the **SEL[3:0]** pin, a static I^2C address can be used to identify individual MABC-11050 devices in a system so that a controller can write to or read from each device. There are three available addresses for each device (Table 3-3). There is also a broadcast address common to all devices so a controller can communicate with all devices at the same time.

Table 3-2. I^2C Timing Characteristics

Symbol	Parameter	Notes	Min	Typ	Max	Unit
fscl	Clock Frequency, SCL				400	KHz
tlow	Clock Pulse Width Low		160			ns
thigh	Clock Pulse Width High		60			ns
tAA	Clock Low to Data Out Valid		0		70	ns
tHD,STA	Start Hold Time		160			ns
tSU,STA	Start Set-up Time		160			ns
tHD,DAT	Data In Hold Time		0			ns
RPULL-UP	Outputs (SDA,SCL) internal pull-up resistor value to VIO			250		KΩ
tSU,STO	Stop Set-up Time		160			ns
tDH	Data Out Hold Time		5			ns

Figure 3-17. I^2C Timing Characteristics

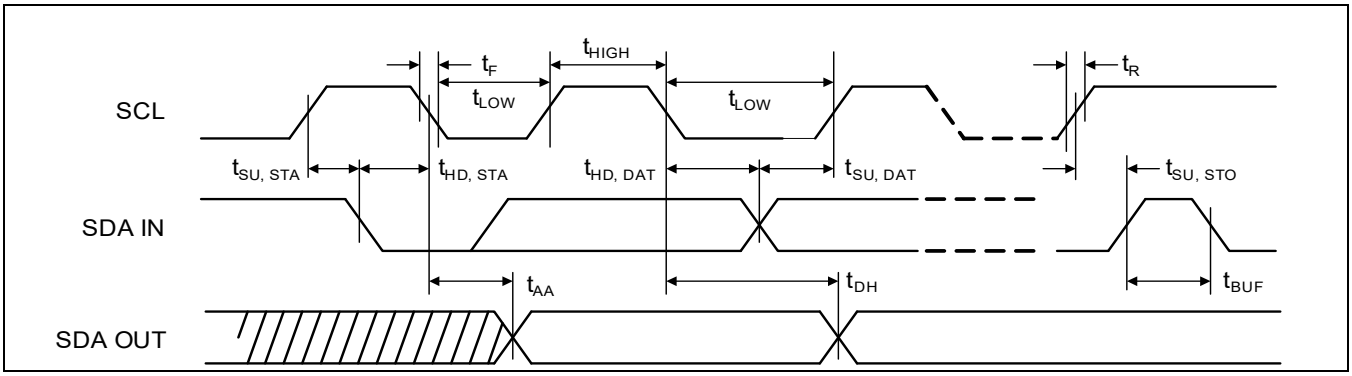


Table 3-3. I^2C Address Table

I2C Address (Hex)		Input Setting				I2C Address (Hex)		Input Setting			
MSB	LSB	SEL3	SEL2	SEL1	SEL0	MSB	LSB	SEL3	SEL2	SEL1	SEL0
0	0	RESERVED				1	D	GND	VIO	VDD5V	VIO
0	1	GND	GND	GND	VIO	1	E				N/C
0	2				N/C	1	F				VDD5V
0	3				VDD5V	2	0		N/C	GND	GND
0	4			VIO	GND	2	1				VIO
0	5				VIO	2	2				N/C
0	6				N/C	2	3				VDD5V
0	7				VDD5V	2	4			VIO	GND
0	8			N/C	GND	2	5				VIO
0	9				VIO	2	6				N/C
0	A				N/C	2	7				VDD5V
0	B				VDD5V	2	8			N/C	GND
0	C			VDD5V	GND	2	9				VIO
0	D				VIO	2	A				N/C
0	E				N/C	2	B				VDD5V
0	F				VDD5V	2	C			VDD5V	GND
1	0		VIO	GND	GND	2	D				VIO
1	1				VIO	2	E				N/C
1	2				N/C	2	F				VDD5V
1	3				VDD5V	3	0		VDD5V	GND	GND
1	4			VIO	GND	3	1				VIO
1	5				VIO	3	2				N/C
1	6				N/C	3	3				VDD5V
1	7				VDD5V	3	4			VIO	GND
1	8			N/C	GND	3	5				VIO
1	9				VIO	3	6				N/C
1	A				N/C	3	7				VDD5V
1	B				VDD5V	3	8			N/C	GND
1	C			VDD5V	GND	3	9				VIO

Table 3-3. I^2C Address Table

I2C Address (Hex)		Input Setting				I2C Address (Hex)		Input Setting			
MSB	LSB	SEL3	SEL2	SEL1	SEL0	MSB	LSB	SEL3	SEL2	SEL1	SEL0
3	A	GND	VDD5V	N/C	N/C	5	7	VIO	VIO	VIO	VDD5V
3	B				VDD5V	5	8			N/C	GND
3	C			VDD5V	GND	5	9				VIO
3	D				VIO	5	A				N/C
3	E				N/C	5	B				VDD5V
3	F				VDD5V	5	C			VDD5V	GND
4	0	VIO	GND	GND	GND	5	D				VIO
4	1				VIO	5	E				N/C
4	2				N/C	5	F				VDD5V
4	3				VDD5V	6	0		N/C	GND	GND
4	4			VIO	GND	6	1				VIO
4	5				VIO	6	2				N/C
4	6				N/C	6	3				VDD5V
4	7				VDD5V	6	4			VIO	GND
4	8			N/C	GND	6	5				VIO
4	9				VIO	6	6				N/C
4	A				N/C	6	7				VDD5V
4	B				VDD5V	6	8			N/C	GND
4	C			VDD5V	GND	6	9				VIO
4	D				VIO	6	A				N/C
4	E				N/C	6	B				VDD5V
4	F				VDD5V	6	C			VDD5V	GND
5	0		VIO	GND	GND	6	D				VIO
5	1				VIO	6	E				N/C
5	2				N/C	6	F				VDD5V
5	3				VDD5V	7	0		VDD5V	GND	GND
5	4			VIO	GND	7	1				VIO
5	5	Reserved				7	2				N/C
5	6	VIO	VIO	VIO	N/C	7	3				VDD5V

Table 3-3. I^2C Address Table

I2C Address (Hex)		Input Setting				I2C Address (Hex)		Input Setting			
MSB	LSB	SEL3	SEL2	SEL1	SEL0	MSB	LSB	SEL3	SEL2	SEL1	SEL0
7	4	VIO	VDD5V	VIO	GND	7	C	VIO	VDD5V	VDD5V	GND
7	5				VIO	7	D				VIO
7	6				N/C	7	E				N/C
7	7				VDD5V	7	F				VDD5V

Note:
1. Using a 0ohm resistor as a pull up to either VIO or VDD5V
2. For Broadcast I2C Address, please contact MACOM for details.

Table 3-4. I^2C Digital Level Margin

Digital level	Voltage Level Range	
	Min	Max
VDD5V	VDD5V-0.1V	VDD5V
N/C	VDD5V-0.3V	VDD5V-0.6
VIO	1.4V	3.63V
GND	0V	1.2V

4.0 Control Registers Map and Descriptions

4.1 Register Map General Overview

The MABC-11050 has a lot of functions that can be controlled via registers, the register map is divided with several register pages to help distribute these functions as described in the following

Register Map Description Summary

Function		Comment
Low Side Driver	00h	LSD Control, DAC, ADC mux, Alarm Masks
EEPROM	01h	EEPROM, user defined information
Global	02h	Global control, ADC, Alarm calibration
Look Up Table for Temperature	80h	LUT Temp[0:127]
	81h	LUT Temp[128:255]
Look Up Table for Voltage	90h	LSD1 LUT Voltage[0:63]
	91h	LSD2 LUT Voltage[0:63]
	92h	LSD3 LUT Voltage[0:63]
	93h	LSD4 LUT Voltage[0:63]

NOTES:

- After power up or software reset, the default page in 00h.
- Write the password to switch pages (refer to section3-2-1 for password)
- Write page number to register0xFE to select page. Register 0xFEis accessible from any page.

Table 4-1 shows the register map for the MABC-11050. Should any reserved registers or bits need to be written, use with their default value listed. Registers not listed in Table 4-1 are reserved with default value of 00h.

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
00h	00h	CHECKSUMSEED	checksumseed<7:0>								55h	R/W
00h	03h	LSD1_LUTV_BS_LSB	*RSVD*		LSD1_BYPASS	LSD1_POL	LSD1_BASE<3:0>				10h	R/W
00h	04h	LSD1_LUTV_BS_MSB	LSD1_BASE<11:4>								99h	R/W
00h	05h	LSD1_LUTV_BS_ADD	LSD1_LUTV_BS_ADD<7:0>								1Ah	R/W
00h	06h	LSD2_LUTV_BS_LSB	*RSVD*		LSD2_BYPASS	LSD2_POL	LSD2_BASE<3:0>				10h	R/W
00h	07h	LSD2_LUTV_BS_MSB	LSD2_BASE<11:4>								99h	R/W

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
00h	08h	LSD2_LUTV_BS_ADD	LSD2_LUTV_BS_ADD<7:0>								1Ah	R/W
00h	09h	LSD3_LUTV_BS_LSB	*RSVD*		LSD3_BYPASS	LSD3_POL	LSD3_BASE<3:0>				10h	R/W
00h	0Ah	LSD3_LUTV_BS_MSB	LSD3_BASE<11:4>								99h	R/W
00h	0Bh	LSD3_LUTV_BS_ADD	LSD3_LUTV_BS_ADD<7:0>								1Ah	R/W
00h	0Ch	LSD4_LUTV_BS_LSB	*RSVD*		LSD4_BYPASS	LSD4_POL	LSD4_BASE<3:0>				10h	R/W
00h	0Dh	LSD4_LUTV_BS_MSB	LSD4_BASE<11:4>								99h	R/W
00h	0Eh	LSD4_LUTV_BS_ADD	LSD4_LUTV_BS_ADD<7:0>								1Ah	R/W
00h	0Fh	LUT_TEMP_BS_MSB	LUT_TEMP_BS_TEMP<11:4>								68h	R/W
00h	10h	LUT_TEMP_BS_LSB	LUT_TEMP_BS_TEMP<3:0>				*RSVD*				00h	R/W
00h	11h	LUT_TEMP_BS_ADDRESS	LUT_TEMP_BS_ADD<7:0>								97h	R/W
00h	12h	LSD1_TS_BS_MSB	LSD1_TS_BS<11:4>								89h	R/W
00h	13h	LSD2_TS_BS_MSB	LSD2_TS_BS<11:4>								89h	R/W
00h	14h	LSD12_TS_BS_LSB	LSD2_TS_BS<3:0>				LSD1_TS_BS<3:0>				22h	R/W
00h	15h	LSD3_TS_BS_MSB	LSD3_TS_BS<11:4>								89h	R/W
00h	16h	LSD4_TS_BS_MSB	LSD4_TS_BS<11:4>								89h	R/W
00h	17h	LSD34_TS_BS_LSB	LSD4_TS_BS<3:0>				LSD3_TS_BS<3:0>				22h	R/W
00h	1Fh	VER_CTRL	*RSVD*				VERSION<3:0>				64h	R/W
00h	33h	ADC_CHNL_ENABLE0	EN_LSD3_OUTN	EN_LSD2_OUTN	EN_LSD1_OUTN	EN_LSD4_OUTP	EN_LSD3_OUTP	EN_LSD2_OUTP	EN_LSD1_OUTP	*RSVD*	FFh	R/W
00h	5Bh	ADC_MANU_CTRL1	mux_sel_I	mux_sel_v	adc_iext_sel	adc_override	adc_tiagain<1:0>		adc_vdiv<1:0>		00h	R/W
00h	65h	LSD1_CTRL0	LSD1_CL<2>	LSD1_CL<1>	LSD1_CL<0>	*RSVD*		LSD1_5G_O-PAMP_EN	LSD1_5G_ENB	LSD1_REG_EN	8Bh	R/W
00h	66h	LSD1_CTRL1	*RSVD*	LSD1_CSP_EN	LSD1_CSN_EN	*RSVD*	LSD1_Rset<1:0>		*RSVD*		00h	R/W
00h	67h	LSD2_CTRL0	LSD2_CL<2>	LSD2_CL<1>	LSD2_CL<0>	*RSVD*		LSD2_5G_O-PAMP_EN	LSD2_5G_ENB	LSD2_REG_EN	8Bh	R/W
00h	68h	LSD2_CTRL1	*RSVD*	LSD2_CSP_EN	LSD2_CSN_EN	*RSVD*	LSD2_Rset<1:0>		*RSVD*		00h	R/W
00h	69h	LSD3_CTRL0	LSD3_CL<2>	LSD3_CL<1>	LSD3_CL<0>	*RSVD*		LSD3_5G_O-PAMP_EN	LSD3_5G_ENB	LSD3_REG_EN	8Bh	R/W
00h	6Ah	LSD3_CTRL1	*RSVD*	LSD3_CSP_EN	LSD3_CSN_EN	*RSVD*	LSD3_Rset<1:0>		*RSVD*		00h	R/W
00h	6Bh	LSD4_CTRL0	LSD4_CL<2>	LSD4_CL<1>	LSD4_CL<0>	*RSVD*		LSD4_5G_O-PAMP_EN	LSD4_5G_ENB	LSD4_REG_EN	8Bh	R/W
00h	6Ch	LSD4_CTRL1	*RSVD*	LSD4_CSP_EN	LSD4_CSN_EN	*RSVD*	LSD4_Rset<1:0>		*RSVD*		00h	R/W
00h	6Dh	OVERRIDE_CTRL	DAC_ORD <3:0>				TEMP_ORD <3:0>				00h	R/W
00h	6Eh	DAC_LSD1_MSB	DAC_LSD1<11:4>								00h	R/W
00h	6Fh	DAC_LSD1_LSB	DAC_LSD1<3:0>				*RSVD*				00h	R/W
00h	70h	DAC_LSD1_ORD_MSB	DAC_LSD1_ORD<11:4>								FFh	R/W
00h	71h	DAC_LSD1_ORD_LSB	DAC_LSD1_ORD<3:0>				*RSVD*				F0h	R/W
00h	72h	DAC_LSD2_MSB	DAC_LSD2<11:4>								00h	R/W

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
00h	73h	DAC_LSD2_LSB	DAC_LSD2 <3:0>				*RSVD*				00h	R/W
00h	74h	DAC_LSD2_ORD_MSB	DAC_LSD2_ORD<11:4>								FFh	R/W
00h	75h	DAC_LSD2_ORD_LSB	DAC_LSD2_ORD<3:0>				*RSVD*				F0h	R/W
00h	76h	DAC_LSD3_MSB	DAC_LSD3<11:4>								00h	R/W
00h	77h	DAC_LSD3_LSB	DAC_LSD3<3:0>				*RSVD*				00h	R/W
00h	78h	DAC_LSD3_ORD_MSB	DAC_LSD3_ORD<11:4>								FFh	R/W
00h	79h	DAC_LSD3_ORD_LSB	DAC_LSD3_ORD<3:0>				*RSVD*				F0h	R/W
00h	7Ah	DAC_LSD4_MSB	DAC_LSD4<11:4>								00h	R/W
00h	7Bh	DAC_LSD4_LSB	DAC_LSD4<3:0>				*RSVD*				00h	R/W
00h	7Ch	DAC_LSD4_ORD_MSB	DAC_LSD4_ORD<11:4>								FFh	R/W
00h	7Dh	DAC_LSD4_ORD_LSB	DAC_LSD4_ORD<3:0>				*RSVD*				F0h	R/W
00h	7Eh	PREDRIVER_CTRL0	Pre_driver_current<3:0>				Tswoff_infinity	HSD_driver_current<2:0>			57h	R/W
00h	7Fh	GPIO_CTRL0	*RSVD*				gpio_status<3:0>				00h	R/W
00h	80h	HSD_Timing	ton<1:0>		tswon<1:0>		tswoff<1:0>		toff<1:0>		D3h	R/W
00h	93h	ALARM_CTRL0	UV_alarm_Vth		OT_Shutdown_threshold		vneg_rdy_vth		*RSVD*		A0h	R/W
00h	94h	IIN1_THRESHOLD	IIN1_THRESHOLD<7:0>								F8h	R/W
00h	95h	IIN2_THRESHOLD	IIN2_THRESHOLD<7:0>								F8h	R/W
00h	96h	TEMP1_OT_S_THD	TEMP1_OT_THD<7:0>								F8h	R/W
00h	97h	TEMP1_OT_R_THD	TEMP1_OT_R_THD<7:0>								F0h	R/W
00h	98h	TEMP2_OT_S_THD	TEMP2_OT_THD<7:0>								F8h	R/W
00h	99h	TEMP2_OT_R_THD	TEMP2_OT_R_THD<7:0>								F0h	R/W
00h	9Ah	TEMP3_OT_S_THD	TEMP3_OT_THD<7:0>								F8h	R/W
00h	9Bh	TEMP3_OT_R_THD	TEMP3_OT_R_THD<7:0>								F0h	R/W
00h	9Ch	TEMP4_OT_S_THD	TEMP4_OT_THD<7:0>								F8h	R/W
00h	9Dh	TEMP4_OT_R_THD	TEMP4_OT_R_THD<7:0>								F0h	R/W
00h	9Eh	TS_VBG_OT_THD	TS_VBG_OT_S_THD<7:0>								F8h	R/W
00h	9Fh	TS_VBG_OT_R_THD	TS_VBG_OT_R_THD<7:0>								F0h	R/W
00h	A0h	TS_PTAT_OT_THD	TS_PTAT_OT_S_THD<7:0>								F8h	R/W
00h	A1h	TS_PTAT_OT_R_THD	TS_PTAT_OT_R_THD<7:0>								F0h	R/W
00h	A2h	FAIL_CTRL	alarm_clear	ts_autocalib	Fail_out_cmos	Fail_flip_polar	Fail_interrupt_duration			FAIL_PIN_-MODE	81h	R/W
00h	A3h	ALARM_MASK0	Alarmmask0<7:0>								00h	R/W
00h	A4h	ALARM_MASK1	Alarmmask1<7:0>								00h	R/W
00h	A5h	ALARM_MASK2	Alarmmask2<7:0>								23h	R/W
00h	A6h	ALARM_MASK3	Alarmmask3<7:0>								03h	R/W
00h	A7h	RSVD0	RSVD0<7:0>								00h	R/W
00h	AAh	UPLIMIT_LSD1_MSB	UPLIMIT_LSD1<11:4>								FFh	R/W

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
00h	ABh	UPLIMIT_LSD2_MSB	UPLIMIT_LSD2<11:4>								FFh	R/W
00h	ACh	UPLIMIT_LSD12_LSB	UPLIMIT_LSD1<3:0>				UPLIMIT_LSD2<3:0>				FFh	R/W
00h	ADh	UPLIMIT_LSD3_MSB	UPLIMIT_LSD3<11:4>								FFh	R/W
00h	AEh	UPLIMIT_LSD4_MSB	UPLIMIT_LSD4<11:4>								FFh	R/W
00h	AFh	UPLIMIT_LSD34_LSB	UPLIMIT_LSD3<3:0>				UPLIMIT_LSD4<3:0>				FFh	R/W
00h	B0h	BTLIMIT_LSD1_MSB	BTLIMIT_LSD1<11:4>								00h	R/W
00h	B1h	BTLIMIT_LSD2_MSB	BTLIMIT_LSD2<11:4>								00h	R/W
00h	B2h	BTLIMIT_LSD12_LSB	BTLIMIT_LSD1<3:0>				BTLIMIT_LSD2<3:0>				00h	R/W
00h	B3h	BTLIMIT_LSD3_MSB	BTLIMIT_LSD3<11:4>								00h	R/W
00h	B4h	BTLIMIT_LSD4_MSB	BTLIMIT_LSD4<11:4>								00h	R/W
00h	B5h	BTLIMIT_LSD34_LSB	BTLIMIT_LSD3<3:0>				BTLIMIT_LSD4<3:0>				00h	R/W
00h	B6h	LUT_VOLT_CTRL	*RSVD*				LUTVOLT_TEMP_SEL<3:0>				08h	R/W
00h	B7h	I2C_CONTROL	*RSVD*	i2c_add_reg							80h	R/W
00h	B8h	I2C_ALLCALL	*RSVD*	i2c_allcall_adr<6:0>							55h	R/W
00h	E0h	NVM_BURN_COUNT1	NVM_BURN_COUNT<7:0>								00h	R/W
00h	E1h	NVM_BURN_COUNT2	NVM_BURN_COUNT<15:8>								00h	R/W
00h	FAh	PASSWORD0	PASSWORD0<7:0>								00h	R/W
00h	FBh	PASSWORD1	PASSWORD1<7:0>								00h	R/W
00h	FCh	PASSWORD2	PASSWORD2<7:0>								00h	R/W
00h	FDh	PASSWORD3	PASSWORD3<7:0>								00h	R/W
00h	FEh	PAGE	Page<7:0>								00h	R/W
02h	00h	CHIPID	CHIPID								47h	R/W
02h	01h	REVID	REVID								03h	R/W
02h	02h	SOFT_RESET	SOFT_RESET								00h	R/W
02h	09h	I2C_ANA	I2C_allcall_dis	I2c_ana<6:0>							41h	R/W
02h	0Fh	CHNL0_MSB	ADC_I_LSD_ADJUST<11:4>								00h	R/W
02h	10h	CHNL0_LSB	*RSVD*				Access_ctrl<3:0>				00h	R/W
02h	11h	CHNL1_MSB	ADC_LSD1_OUTP<11:4>								00h	R/W
02h	12h	CHNL1_LSB	ADC_LSD1_OUTP<3:0>				*RSVD*				00h	R/W
02h	13h	CHNL2_MSB	ADC_LSD2_OUTP<11:4>								00h	R/W
02h	14h	CHNL2_LSB	ADC_LSD2_OUTP<3:0>				*RSVD*				00h	R/W
02h	15h	CHNL3_MSB	ADC_LSD3_OUTP<11:4>								00h	R/W
02h	16h	CHNL3_LSB	ADC_LSD3_OUTP<3:0>				*RSVD*				00h	R/W
02h	17h	CHNL4_MSB	ADC_LSD4_OUTP<11:4>								00h	R/W
02h	18h	CHNL4_LSB	ADC_LSD4_OUTP<3:0>				*RSVD*				00h	R/W
02h	19h	CHNL5_MSB	ADC_LSD1_OUTN<11:4>								00h	R/W

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
02h	1Ah	CHNL5_LSB	ADC_LSD1_OUTN<3:0>				*RSVD*				00h	R/W
02h	1Bh	CHNL6_MSB	ADC_LSD2_OUTN<11:4>								00h	R/W
02h	1Ch	CHNL6_LSB	ADC_LSD2_OUTN<3:0>				*RSVD*				00h	R/W
02h	1Dh	CHNL7_MSB	ADC_LSD3_OUTN<11:4>								00h	R/W
02h	1Eh	CHNL7_LSB	ADC_LSD3_OUTN<3:0>				*RSVD*				00h	R/W
02h	1Fh	CHNL8_MSB	ADC_LSD4_OUTN<11:4>								00h	R/W
02h	20h	CHNL8_LSB	ADC_LSD4_OUTN<3:0>				*RSVD*				00h	R/W
02h	27h	CHNL12_MSB	ADC_IIN1<11:4>								00h	R/W
02h	28h	CHNL12_LSB	ADC_IIN1<3:0>				*RSVD*				00h	R/W
02h	29h	CHNL13_MSB	ADC_IIN2<11:4>								00h	R/W
02h	2Ah	CHNL13_LSB	ADC_IIN2<3:0>				*RSVD*				00h	R/W
02h	2Fh	CHNL16_MSB	ADC_LSD4_TEMP<11:4>								00h	R/W
02h	30h	CHNL16_LSB	ADC_LSD4_TEMP<3:0>				*RSVD*				00h	R/W
02h	31h	CHNL17_MSB	ADC_LSD3_TEMP<11:4>								00h	R/W
02h	32h	CHNL17_LSB	ADC_LSD3_TEMP<3:0>				*RSVD*				00h	R/W
02h	33h	CHNL18_MSB	ADC_LSD2_TEMP<11:4>								00h	R/W
02h	34h	CHNL18_LSB	ADC_LSD2_TEMP<3:0>				*RSVD*				00h	R/W
02h	35h	CHNL19_MSB	ADC_LSD1_TEMP<11:4>								00h	R/W
02h	36h	CHNL19_LSB	ADC_LSD1_TEMP<3:0>				*RSVD*				00h	R/W
02h	39h	CHNL21_MSB	ADC_EXT_VNEG<11:4>								00h	R/W
02h	3Ah	CHNL21_LSB	ADC_EXT_VNEG<3:0>				*RSVD*				00h	R/W
02h	3Fh	TEMP_ALARM	iin1_cl_lt	iin2_cl_lt	TS_VBG_Alarm	TS_PTAT_Alarm	LSD4_TS_Alarm	LSD3_TS_Alarm	LSD2_TS_Alarm	LSD1_TS_Alarm	00h	R/W
02h	40h	ALARM0	neg_uv_rt	lsd1_cl_rt	lsd2_cl_rt	lsd3_cl_rt	lsd4_cl_rt	v1p8d_uv_rt	v1p8a_uv_rt	undervolt-age_alarm_rt	00h	R/W
02h	41h	ALARM1	neg_uv_lt	lsd1_cl_lt	lsd2_cl_lt	lsd3_cl_lt	lsd4_cl_lt	v1p8d_uv_lt	v1p8a_uv_lt	undervolt-age_alarm_lt	00h	R/W
02h	42h	ALARM_LUT_TEMP	lsd4_lut_-temp_p	lsd4_lut_-temp_n	lsd3_lut_-temp_p	lsd3_lut_-temp_n	lsd2_lut_-temp_p	lsd2_lut_-temp_n	lsd1_lut_-temp_p	lsd1_lut_-temp_n	00h	R/W
02h	43h	ALARM_LUT_VOLT	lsd4_lut_volt_p	lsd4_lut_volt_n	lsd3_lut_volt_p	lsd3_lut_-volt_n	lsd2_lut_volt_p	lsd2_lut_volt_n	lsd1_lut_volt_p	lsd1_lut_volt_n	00h	R/W
02h	46h	OFFCHIP_TEMP_MSB	offchip_temp<11:4>								00h	R/W
02h	47h	OFFCHIP_TEMP_LSB	offchip_temp<3:0>				*RSVD*				00h	R/W
02h	48h	CAL_TS1_MSB	cal_ts1<11:4>								00h	R/W
02h	49h	CAL_TS1_LSB	cal_ts1<3:0>				*RSVD*				00h	R/W
02h	4Ah	CAL_TS2_MSB	cal_ts2<11:4>								00h	R/W
02h	4Bh	CAL_TS2_LSB	cal_ts2<3:0>				*RSVD*				00h	R/W
02h	4Ch	CAL_TS3_MSB	cal_ts3<11:4>								00h	R/W
02h	4Dh	CAL_TS3_LSB	cal_ts3<3:0>				*RSVD*				00h	R/W

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
02h	4Eh	CAL_TS4_MSB	cal_ts4<11:4>								00h	R/W
02h	4Fh	CAL_TS4_LSB	cal_ts4<3:0>				*RSVD*				00h	R/W
02h	50h	CAL_INT_BG_MSB	cal_int_TS_VBG<11:4>								00h	R/W
02h	51h	CAL_INT_BG_LSB	cal_int_TS_VBG<3:0>				*RSVD*				00h	R/W
02h	52h	CAL_INT_PTAT_MSB	cal_int_ts_ptat<11:4>								00h	R/W
02h	53h	CAL_INT_PTAT_LSB	cal_int_ts_ptat<3:0>				*RSVD*				00h	R/W
01h	62h	POWER_MSB	POWER_MSB								00h	R/W
01h	6Ch	VENDOR_CODE	VENDOR_CODE								00h	R/W
01h	6Dh	UNI_MOD_TYP_NO1	UNI_MOD_TYP_NO1								00h	R/W
01h	6Eh	UNI_MOD_TYP_NO2	UNI_MOD_TYP_NO2								00h	R/W
01h	6Fh	POWER_LSB	POWER_LSB								00h	R/W
01h	70h	DL_FREQ_LOW1	DL_FREQ_LOW1								00h	R/W
01h	71h	DL_FREQ_LOW2	DL_FREQ_LOW2								00h	R/W
01h	72h	DL_FREQ_HIGH1	DL_FREQ_HIGH1								00h	R/W
01h	73h	DL_FREQ_HIGH2	DL_FREQ_HIGH2								00h	R/W
01h	74h	CODE_YEAR	CODE_YEAR								00h	R/W
01h	75h	CODE_WEEK	CODE_WEEK								00h	R/W
01h	76h	MODULE_NAME1	MODULE_NAME1								00h	R/W
01h	77h	MODULE_NAME2	MODULE_NAME2								00h	R/W
01h	78h	MODULE_NAME3	MODULE_NAME3								00h	R/W
01h	79h	MODULE_NAME4	MODULE_NAME4								00h	R/W
01h	7Ah	MODULE_NAME5	MODULE_NAME5								00h	R/W
01h	7Bh	MODULE_NAME6	MODULE_NAME6								00h	R/W
01h	7Ch	MODULE_NAME7	MODULE_NAME7								00h	R/W
01h	7Dh	MODULE_NAME8	MODULE_NAME8								00h	R/W
01h	7Eh	MODULE_NAME9	MODULE_NAME9								00h	R/W
01h	7Fh	MODULE_NAME10	MODULE_NAME10								00h	R/W
01h	FAh	PASSWORD0	PASSWORD0<7:0>								00h	R/W
01h	FBh	PASSWORD1	PASSWORD1<7:0>								00h	R/W
01h	FCh	PASSWORD2	PASSWORD2<7:0>								00h	R/W
01h	FDh	PASSWORD3	PASSWORD3<7:0>								00h	R/W
01h	FEh	PAGE	page<7:0>								00h	R/W
80h	00h	LUT_TEMP0	LUT_TEMP0[7:0]								00h	R/W
80h	01h	LUT_TEMP1	LUT_TEMP1[7:0]								00h	R/W
80h	02h	LUT_TEMP2	LUT_TEMP2[7:0]								00h	R/W
80h	03h	LUT_TEMP3	LUT_TEMP3[7:0]								00h	R/W

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
80h	04h	LUT_TEMP4	LUT_TEMP4[7:0]								00h	R/W
80h	05h	LUT_TEMP5	LUT_TEMP5[7:0]								00h	R/W
80h	06h	LUT_TEMP6	LUT_TEMP6[7:0]								00h	R/W
80h	07h	LUT_TEMP7	LUT_TEMP7[7:0]								00h	R/W
80h	08h	LUT_TEMP8	LUT_TEMP8[7:0]								00h	R/W
80h	09h	LUT_TEMP9	LUT_TEMP9[7:0]								00h	R/W
80h	0Ah	LUT_TEMP10	LUT_TEMP10[7:0]								00h	R/W
80h	0Bh	LUT_TEMP11	LUT_TEMP11[7:0]								00h	R/W
80h	0Ch	LUT_TEMP12	LUT_TEMP12[7:0]								00h	R/W
80h	0Dh	LUT_TEMP13	LUT_TEMP13[7:0]								00h	R/W
80h	0Eh	LUT_TEMP14	LUT_TEMP14[7:0]								00h	R/W
80h	0Fh	LUT_TEMP15	LUT_TEMP15[7:0]								00h	R/W
80h	10h	LUT_TEMP16	LUT_TEMP16[7:0]								00h	R/W
80h	11h	LUT_TEMP17	LUT_TEMP17[7:0]								00h	R/W
80h	12h	LUT_TEMP18	LUT_TEMP18[7:0]								00h	R/W
80h	13h	LUT_TEMP19	LUT_TEMP19[7:0]								00h	R/W
80h	14h	LUT_TEMP20	LUT_TEMP20[7:0]								00h	R/W
80h	15h	LUT_TEMP21	LUT_TEMP21[7:0]								00h	R/W
80h	16h	LUT_TEMP22	LUT_TEMP22[7:0]								00h	R/W
80h	17h	LUT_TEMP23	LUT_TEMP23[7:0]								00h	R/W
80h	18h	LUT_TEMP24	LUT_TEMP24[7:0]								00h	R/W
80h	19h	LUT_TEMP25	LUT_TEMP25[7:0]								00h	R/W
80h	1Ah	LUT_TEMP26	LUT_TEMP26[7:0]								00h	R/W
80h	1Bh	LUT_TEMP27	LUT_TEMP27[7:0]								00h	R/W
80h	1Ch	LUT_TEMP28	LUT_TEMP28[7:0]								00h	R/W
80h	1Dh	LUT_TEMP29	LUT_TEMP29[7:0]								00h	R/W
80h	1Eh	LUT_TEMP30	LUT_TEMP30[7:0]								00h	R/W
80h	1Fh	LUT_TEMP31	LUT_TEMP31[7:0]								00h	R/W
80h	20h	LUT_TEMP32	LUT_TEMP32[7:0]								00h	R/W
80h	21h	LUT_TEMP33	LUT_TEMP33[7:0]								00h	R/W
80h	22h	LUT_TEMP34	LUT_TEMP34[7:0]								00h	R/W
80h	23h	LUT_TEMP35	LUT_TEMP35[7:0]								00h	R/W
80h	24h	LUT_TEMP36	LUT_TEMP36[7:0]								00h	R/W
80h	25h	LUT_TEMP37	LUT_TEMP37[7:0]								00h	R/W
80h	26h	LUT_TEMP38	LUT_TEMP38[7:0]								00h	R/W
80h	27h	LUT_TEMP39	LUT_TEMP39[7:0]								00h	R/W

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
80h	28h	LUT_TEMP40	LUT_TEMP40[7:0]								00h	R/W
80h	29h	LUT_TEMP41	LUT_TEMP41[7:0]								00h	R/W
80h	2Ah	LUT_TEMP42	LUT_TEMP42[7:0]								00h	R/W
80h	2Bh	LUT_TEMP43	LUT_TEMP43[7:0]								00h	R/W
80h	2Ch	LUT_TEMP44	LUT_TEMP44[7:0]								00h	R/W
80h	2Dh	LUT_TEMP45	LUT_TEMP45[7:0]								00h	R/W
80h	2Eh	LUT_TEMP46	LUT_TEMP46[7:0]								00h	R/W
80h	2Fh	LUT_TEMP47	LUT_TEMP47[7:0]								00h	R/W
80h	30h	LUT_TEMP48	LUT_TEMP48[7:0]								00h	R/W
80h	31h	LUT_TEMP49	LUT_TEMP49[7:0]								00h	R/W
80h	32h	LUT_TEMP50	LUT_TEMP50[7:0]								00h	R/W
80h	33h	LUT_TEMP51	LUT_TEMP51[7:0]								00h	R/W
80h	34h	LUT_TEMP52	LUT_TEMP52[7:0]								00h	R/W
80h	35h	LUT_TEMP53	LUT_TEMP53[7:0]								00h	R/W
80h	36h	LUT_TEMP54	LUT_TEMP54[7:0]								00h	R/W
80h	37h	LUT_TEMP55	LUT_TEMP55[7:0]								00h	R/W
80h	38h	LUT_TEMP56	LUT_TEMP56[7:0]								00h	R/W
80h	39h	LUT_TEMP57	LUT_TEMP57[7:0]								00h	R/W
80h	3Ah	LUT_TEMP58	LUT_TEMP58[7:0]								00h	R/W
80h	3Bh	LUT_TEMP59	LUT_TEMP59[7:0]								00h	R/W
80h	3Ch	LUT_TEMP60	LUT_TEMP60[7:0]								00h	R/W
80h	3Dh	LUT_TEMP61	LUT_TEMP61[7:0]								00h	R/W
80h	3Eh	LUT_TEMP62	LUT_TEMP62[7:0]								00h	R/W
80h	3Fh	LUT_TEMP63	LUT_TEMP63[7:0]								00h	R/W
80h	40h	LUT_TEMP64	LUT_TEMP64[7:0]								00h	R/W
80h	41h	LUT_TEMP65	LUT_TEMP65[7:0]								00h	R/W
80h	42h	LUT_TEMP66	LUT_TEMP66[7:0]								00h	R/W
80h	43h	LUT_TEMP67	LUT_TEMP67[7:0]								00h	R/W
80h	44h	LUT_TEMP68	LUT_TEMP68[7:0]								00h	R/W
80h	45h	LUT_TEMP69	LUT_TEMP69[7:0]								00h	R/W
80h	46h	LUT_TEMP70	LUT_TEMP70[7:0]								00h	R/W
80h	47h	LUT_TEMP71	LUT_TEMP71[7:0]								00h	R/W
80h	48h	LUT_TEMP72	LUT_TEMP72[7:0]								00h	R/W
80h	49h	LUT_TEMP73	LUT_TEMP73[7:0]								00h	R/W
80h	4Ah	LUT_TEMP74	LUT_TEMP74[7:0]								00h	R/W
80h	4Bh	LUT_TEMP75	LUT_TEMP75[7:0]								00h	R/W

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
80h	4Ch	LUT_TEMP76	LUT_TEMP76[7:0]								00h	R/W
80h	4Dh	LUT_TEMP77	LUT_TEMP77[7:0]								00h	R/W
80h	4Eh	LUT_TEMP78	LUT_TEMP78[7:0]								00h	R/W
80h	4Fh	LUT_TEMP79	LUT_TEMP79[7:0]								00h	R/W
80h	50h	LUT_TEMP80	LUT_TEMP80[7:0]								00h	R/W
80h	51h	LUT_TEMP81	LUT_TEMP81[7:0]								00h	R/W
80h	52h	LUT_TEMP82	LUT_TEMP82[7:0]								00h	R/W
80h	53h	LUT_TEMP83	LUT_TEMP83[7:0]								00h	R/W
80h	54h	LUT_TEMP84	LUT_TEMP84[7:0]								00h	R/W
80h	55h	LUT_TEMP85	LUT_TEMP85[7:0]								00h	R/W
80h	56h	LUT_TEMP86	LUT_TEMP86[7:0]								00h	R/W
80h	57h	LUT_TEMP87	LUT_TEMP87[7:0]								00h	R/W
80h	58h	LUT_TEMP88	LUT_TEMP88[7:0]								00h	R/W
80h	59h	LUT_TEMP89	LUT_TEMP89[7:0]								00h	R/W
80h	5Ah	LUT_TEMP90	LUT_TEMP90[7:0]								00h	R/W
80h	5Bh	LUT_TEMP91	LUT_TEMP91[7:0]								00h	R/W
80h	5Ch	LUT_TEMP92	LUT_TEMP92[7:0]								00h	R/W
80h	5Dh	LUT_TEMP93	LUT_TEMP93[7:0]								00h	R/W
80h	5Eh	LUT_TEMP94	LUT_TEMP94[7:0]								00h	R/W
80h	5Fh	LUT_TEMP95	LUT_TEMP95[7:0]								00h	R/W
80h	60h	LUT_TEMP96	LUT_TEMP96[7:0]								00h	R/W
80h	61h	LUT_TEMP97	LUT_TEMP97[7:0]								00h	R/W
80h	62h	LUT_TEMP98	LUT_TEMP98[7:0]								00h	R/W
80h	63h	LUT_TEMP99	LUT_TEMP99[7:0]								00h	R/W
80h	64h	LUT_TEMP100	LUT_TEMP100[7:0]								00h	R/W
80h	65h	LUT_TEMP101	LUT_TEMP101[7:0]								00h	R/W
80h	66h	LUT_TEMP102	LUT_TEMP102[7:0]								00h	R/W
80h	67h	LUT_TEMP103	LUT_TEMP103[7:0]								00h	R/W
80h	68h	LUT_TEMP104	LUT_TEMP104[7:0]								00h	R/W
80h	69h	LUT_TEMP105	LUT_TEMP105[7:0]								00h	R/W
80h	6Ah	LUT_TEMP106	LUT_TEMP106[7:0]								00h	R/W
80h	6Bh	LUT_TEMP107	LUT_TEMP107[7:0]								00h	R/W
80h	6Ch	LUT_TEMP108	LUT_TEMP108[7:0]								00h	R/W
80h	6Dh	LUT_TEMP109	LUT_TEMP109[7:0]								00h	R/W
80h	6Eh	LUT_TEMP110	LUT_TEMP110[7:0]								00h	R/W
80h	6Fh	LUT_TEMP111	LUT_TEMP111[7:0]								00h	R/W

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
80h	70h	LUT_TEMP112	LUT_TEMP112[7:0]								00h	R/W
80h	71h	LUT_TEMP113	LUT_TEMP113[7:0]								00h	R/W
80h	72h	LUT_TEMP114	LUT_TEMP114[7:0]								00h	R/W
80h	73h	LUT_TEMP115	LUT_TEMP115[7:0]								00h	R/W
80h	74h	LUT_TEMP116	LUT_TEMP116[7:0]								00h	R/W
80h	75h	LUT_TEMP117	LUT_TEMP117[7:0]								00h	R/W
80h	76h	LUT_TEMP118	LUT_TEMP118[7:0]								00h	R/W
80h	77h	LUT_TEMP119	LUT_TEMP119[7:0]								00h	R/W
80h	78h	LUT_TEMP120	LUT_TEMP120[7:0]								00h	R/W
80h	79h	LUT_TEMP121	LUT_TEMP121[7:0]								00h	R/W
80h	7Ah	LUT_TEMP122	LUT_TEMP122[7:0]								00h	R/W
80h	7Bh	LUT_TEMP123	LUT_TEMP123[7:0]								00h	R/W
80h	7Ch	LUT_TEMP124	LUT_TEMP124[7:0]								00h	R/W
80h	7Dh	LUT_TEMP125	LUT_TEMP125[7:0]								00h	R/W
80h	7Eh	LUT_TEMP126	LUT_TEMP126[7:0]								00h	R/W
80h	7Fh	LUT_TEMP127	LUT_TEMP127[7:0]								00h	R/W
80h	FAh	PASSWORD0	PASSWORD0<7:0>								00h	R/W
80h	FBh	PASSWORD1	PASSWORD1<7:0>								00h	R/W
80h	FCh	PASSWORD2	PASSWORD2<7:0>								00h	R/W
80h	FDh	PASSWORD3	PASSWORD3<7:0>								00h	R/W
80h	FEh	PAGE	page[7:0]								00h	R/W
81h	00h	LUT_TEMP128	LUT_TEMP128[7:0]								00h	R/W
81h	01h	LUT_TEMP129	LUT_TEMP129[7:0]								00h	R/W
81h	02h	LUT_TEMP130	LUT_TEMP130[7:0]								00h	R/W
81h	03h	LUT_TEMP131	LUT_TEMP131[7:0]								00h	R/W
81h	04h	LUT_TEMP132	LUT_TEMP132[7:0]								00h	R/W
81h	05h	LUT_TEMP133	LUT_TEMP133[7:0]								00h	R/W
81h	06h	LUT_TEMP134	LUT_TEMP134[7:0]								00h	R/W
81h	07h	LUT_TEMP135	LUT_TEMP135[7:0]								00h	R/W
81h	08h	LUT_TEMP136	LUT_TEMP136[7:0]								00h	R/W
81h	09h	LUT_TEMP137	LUT_TEMP137[7:0]								00h	R/W
81h	0Ah	LUT_TEMP138	LUT_TEMP138[7:0]								00h	R/W
81h	0Bh	LUT_TEMP139	LUT_TEMP139[7:0]								00h	R/W
81h	0Ch	LUT_TEMP140	LUT_TEMP140[7:0]								00h	R/W
81h	0Dh	LUT_TEMP141	LUT_TEMP141[7:0]								00h	R/W
81h	0Eh	LUT_TEMP142	LUT_TEMP142[7:0]								00h	R/W

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
81h	0Fh	LUT_TEMP143	LUT_TEMP143[7:0]								00h	R/W
81h	10h	LUT_TEMP144	LUT_TEMP144[7:0]								00h	R/W
81h	11h	LUT_TEMP145	LUT_TEMP145[7:0]								00h	R/W
81h	12h	LUT_TEMP146	LUT_TEMP146[7:0]								00h	R/W
81h	13h	LUT_TEMP147	LUT_TEMP147[7:0]								00h	R/W
81h	14h	LUT_TEMP148	LUT_TEMP148[7:0]								00h	R/W
81h	15h	LUT_TEMP149	LUT_TEMP149[7:0]								00h	R/W
81h	16h	LUT_TEMP150	LUT_TEMP150[7:0]								00h	R/W
81h	17h	LUT_TEMP151	LUT_TEMP151[7:0]								00h	R/W
81h	18h	LUT_TEMP152	LUT_TEMP152[7:0]								00h	R/W
81h	19h	LUT_TEMP153	LUT_TEMP153[7:0]								00h	R/W
81h	1Ah	LUT_TEMP154	LUT_TEMP154[7:0]								00h	R/W
81h	1Bh	LUT_TEMP155	LUT_TEMP155[7:0]								00h	R/W
81h	1Ch	LUT_TEMP156	LUT_TEMP156[7:0]								00h	R/W
81h	1Dh	LUT_TEMP157	LUT_TEMP157[7:0]								00h	R/W
81h	1Eh	LUT_TEMP158	LUT_TEMP158[7:0]								00h	R/W
81h	1Fh	LUT_TEMP159	LUT_TEMP159[7:0]								00h	R/W
81h	20h	LUT_TEMP160	LUT_TEMP160[7:0]								00h	R/W
81h	21h	LUT_TEMP161	LUT_TEMP161[7:0]								00h	R/W
81h	22h	LUT_TEMP162	LUT_TEMP162[7:0]								00h	R/W
81h	23h	LUT_TEMP163	LUT_TEMP163[7:0]								00h	R/W
81h	24h	LUT_TEMP164	LUT_TEMP164[7:0]								00h	R/W
81h	25h	LUT_TEMP165	LUT_TEMP165[7:0]								00h	R/W
81h	26h	LUT_TEMP166	LUT_TEMP166[7:0]								00h	R/W
81h	27h	LUT_TEMP167	LUT_TEMP167[7:0]								00h	R/W
81h	28h	LUT_TEMP168	LUT_TEMP168[7:0]								00h	R/W
81h	29h	LUT_TEMP169	LUT_TEMP169[7:0]								00h	R/W
81h	2Ah	LUT_TEMP170	LUT_TEMP170[7:0]								00h	R/W
81h	2Bh	LUT_TEMP171	LUT_TEMP171[7:0]								00h	R/W
81h	2Ch	LUT_TEMP172	LUT_TEMP172[7:0]								00h	R/W
81h	2Dh	LUT_TEMP173	LUT_TEMP173[7:0]								00h	R/W
81h	2Eh	LUT_TEMP174	LUT_TEMP174[7:0]								00h	R/W
81h	2Fh	LUT_TEMP175	LUT_TEMP175[7:0]								00h	R/W
81h	30h	LUT_TEMP176	LUT_TEMP176[7:0]								00h	R/W
81h	31h	LUT_TEMP177	LUT_TEMP177[7:0]								00h	R/W
81h	32h	LUT_TEMP178	LUT_TEMP178[7:0]								00h	R/W

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
81h	33h	LUT_TEMP179	LUT_TEMP179[7:0]								00h	R/W
81h	34h	LUT_TEMP180	LUT_TEMP180[7:0]								00h	R/W
81h	35h	LUT_TEMP181	LUT_TEMP181[7:0]								00h	R/W
81h	36h	LUT_TEMP182	LUT_TEMP182[7:0]								00h	R/W
81h	37h	LUT_TEMP183	LUT_TEMP183[7:0]								00h	R/W
81h	38h	LUT_TEMP184	LUT_TEMP184[7:0]								00h	R/W
81h	39h	LUT_TEMP185	LUT_TEMP185[7:0]								00h	R/W
81h	3Ah	LUT_TEMP186	LUT_TEMP186[7:0]								00h	R/W
81h	3Bh	LUT_TEMP187	LUT_TEMP187[7:0]								00h	R/W
81h	3Ch	LUT_TEMP188	LUT_TEMP188[7:0]								00h	R/W
81h	3Dh	LUT_TEMP189	LUT_TEMP189[7:0]								00h	R/W
81h	3Eh	LUT_TEMP190	LUT_TEMP190[7:0]								00h	R/W
81h	3Fh	LUT_TEMP191	LUT_TEMP191[7:0]								00h	R/W
81h	40h	LUT_TEMP192	LUT_TEMP192[7:0]								00h	R/W
81h	41h	LUT_TEMP193	LUT_TEMP193[7:0]								00h	R/W
81h	42h	LUT_TEMP194	LUT_TEMP194[7:0]								00h	R/W
81h	43h	LUT_TEMP195	LUT_TEMP195[7:0]								00h	R/W
81h	44h	LUT_TEMP196	LUT_TEMP196[7:0]								00h	R/W
81h	45h	LUT_TEMP197	LUT_TEMP197[7:0]								00h	R/W
81h	46h	LUT_TEMP198	LUT_TEMP198[7:0]								00h	R/W
81h	47h	LUT_TEMP199	LUT_TEMP199[7:0]								00h	R/W
81h	48h	LUT_TEMP200	LUT_TEMP200[7:0]								00h	R/W
81h	49h	LUT_TEMP201	LUT_TEMP201[7:0]								00h	R/W
81h	4Ah	LUT_TEMP202	LUT_TEMP202[7:0]								00h	R/W
81h	4Bh	LUT_TEMP203	LUT_TEMP203[7:0]								00h	R/W
81h	4Ch	LUT_TEMP204	LUT_TEMP204[7:0]								00h	R/W
81h	4Dh	LUT_TEMP205	LUT_TEMP205[7:0]								00h	R/W
81h	4Eh	LUT_TEMP206	LUT_TEMP206[7:0]								00h	R/W
81h	4Fh	LUT_TEMP207	LUT_TEMP207[7:0]								00h	R/W
81h	50h	LUT_TEMP208	LUT_TEMP208[7:0]								00h	R/W
81h	51h	LUT_TEMP209	LUT_TEMP209[7:0]								00h	R/W
81h	52h	LUT_TEMP210	LUT_TEMP210[7:0]								00h	R/W
81h	53h	LUT_TEMP211	LUT_TEMP211[7:0]								00h	R/W
81h	54h	LUT_TEMP212	LUT_TEMP212[7:0]								00h	R/W
81h	55h	LUT_TEMP213	LUT_TEMP213[7:0]								00h	R/W
81h	56h	LUT_TEMP214	LUT_TEMP214[7:0]								00h	R/W

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
81h	57h	LUT_TEMP215	LUT_TEMP215[7:0]								00h	R/W
81h	58h	LUT_TEMP216	LUT_TEMP216[7:0]								00h	R/W
81h	59h	LUT_TEMP217	LUT_TEMP217[7:0]								00h	R/W
81h	5Ah	LUT_TEMP218	LUT_TEMP218[7:0]								00h	R/W
81h	5Bh	LUT_TEMP219	LUT_TEMP219[7:0]								00h	R/W
81h	5Ch	LUT_TEMP220	LUT_TEMP220[7:0]								00h	R/W
81h	5Dh	LUT_TEMP221	LUT_TEMP221[7:0]								00h	R/W
81h	5Eh	LUT_TEMP222	LUT_TEMP222[7:0]								00h	R/W
81h	5Fh	LUT_TEMP223	LUT_TEMP223[7:0]								00h	R/W
81h	60h	LUT_TEMP224	LUT_TEMP224[7:0]								00h	R/W
81h	61h	LUT_TEMP225	LUT_TEMP225[7:0]								00h	R/W
81h	62h	LUT_TEMP226	LUT_TEMP226[7:0]								00h	R/W
81h	63h	LUT_TEMP227	LUT_TEMP227[7:0]								00h	R/W
81h	64h	LUT_TEMP228	LUT_TEMP228[7:0]								00h	R/W
81h	65h	LUT_TEMP229	LUT_TEMP229[7:0]								00h	R/W
81h	66h	LUT_TEMP230	LUT_TEMP230[7:0]								00h	R/W
81h	67h	LUT_TEMP231	LUT_TEMP231[7:0]								00h	R/W
81h	68h	LUT_TEMP232	LUT_TEMP232[7:0]								00h	R/W
81h	69h	LUT_TEMP233	LUT_TEMP233[7:0]								00h	R/W
81h	6Ah	LUT_TEMP234	LUT_TEMP234[7:0]								00h	R/W
81h	6Bh	LUT_TEMP235	LUT_TEMP235[7:0]								00h	R/W
81h	6Ch	LUT_TEMP236	LUT_TEMP236[7:0]								00h	R/W
81h	6Dh	LUT_TEMP237	LUT_TEMP237[7:0]								00h	R/W
81h	6Eh	LUT_TEMP238	LUT_TEMP238[7:0]								00h	R/W
81h	6Fh	LUT_TEMP239	LUT_TEMP239[7:0]								00h	R/W
81h	70h	LUT_TEMP240	LUT_TEMP240[7:0]								00h	R/W
81h	71h	LUT_TEMP241	LUT_TEMP241[7:0]								00h	R/W
81h	72h	LUT_TEMP242	LUT_TEMP242[7:0]								00h	R/W
81h	73h	LUT_TEMP243	LUT_TEMP243[7:0]								00h	R/W
81h	74h	LUT_TEMP244	LUT_TEMP244[7:0]								00h	R/W
81h	75h	LUT_TEMP245	LUT_TEMP245[7:0]								00h	R/W
81h	76h	LUT_TEMP246	LUT_TEMP246[7:0]								00h	R/W
81h	77h	LUT_TEMP247	LUT_TEMP247[7:0]								00h	R/W
81h	78h	LUT_TEMP248	LUT_TEMP248[7:0]								00h	R/W
81h	79h	LUT_TEMP249	LUT_TEMP249[7:0]								00h	R/W
81h	7Ah	LUT_TEMP250	LUT_TEMP250[7:0]								00h	R/W

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
81h	7Bh	LUT_TEMP251	LUT_TEMP251[7:0]								00h	R/W
81h	7Ch	LUT_TEMP252	LUT_TEMP252[7:0]								00h	R/W
81h	7Dh	LUT_TEMP253	LUT_TEMP253[7:0]								00h	R/W
81h	7Eh	LUT_TEMP254	LUT_TEMP254[7:0]								00h	R/W
81h	7Fh	LUT_TEMP255	LUT_TEMP255[7:0]								00h	R/W
81h	FAh	PASSWORD0	PASSWORD0<7:0>								00h	R/W
81h	FBh	PASSWORD1	PASSWORD1<7:0>								00h	R/W
81h	FCh	PASSWORD2	PASSWORD2<7:0>								00h	R/W
81h	FDh	PASSWORD3	PASSWORD3<7:0>								00h	R/W
81h	FEh	PAGE	page[7:0]								00h	R/W
90h	00h	LSD1_DEL0	LSD1_DEL0[7:0]								00h	R/W
90h	01h	LSD1_DEL1	LSD1_DEL1[7:0]								00h	R/W
90h	02h	LSD1_DEL2	LSD1_DEL2[7:0]								00h	R/W
90h	03h	LSD1_DEL3	LSD1_DEL3[7:0]								00h	R/W
90h	04h	LSD1_DEL4	LSD1_DEL4[7:0]								00h	R/W
90h	05h	LSD1_DEL5	LSD1_DEL5[7:0]								00h	R/W
90h	06h	LSD1_DEL6	LSD1_DEL6[7:0]								00h	R/W
90h	07h	LSD1_DEL7	LSD1_DEL7[7:0]								00h	R/W
90h	08h	LSD1_DEL8	LSD1_DEL8[7:0]								00h	R/W
90h	09h	LSD1_DEL9	LSD1_DEL9[7:0]								00h	R/W
90h	0Ah	LSD1_DEL10	LSD1_DEL10[7:0]								00h	R/W
90h	0Bh	LSD1_DEL11	LSD1_DEL11[7:0]								00h	R/W
90h	0Ch	LSD1_DEL12	LSD1_DEL12[7:0]								00h	R/W
90h	0Dh	LSD1_DEL13	LSD1_DEL13[7:0]								00h	R/W
90h	0Eh	LSD1_DEL14	LSD1_DEL14[7:0]								00h	R/W
90h	0Fh	LSD1_DEL15	LSD1_DEL15[7:0]								00h	R/W
90h	10h	LSD1_DEL16	LSD1_DEL16[7:0]								00h	R/W
90h	11h	LSD1_DEL17	LSD1_DEL17[7:0]								00h	R/W
90h	12h	LSD1_DEL18	LSD1_DEL18[7:0]								00h	R/W
90h	13h	LSD1_DEL19	LSD1_DEL19[7:0]								00h	R/W
90h	14h	LSD1_DEL20	LSD1_DEL20[7:0]								00h	R/W
90h	15h	LSD1_DEL21	LSD1_DEL21[7:0]								00h	R/W
90h	16h	LSD1_DEL22	LSD1_DEL22[7:0]								00h	R/W
90h	17h	LSD1_DEL23	LSD1_DEL23[7:0]								00h	R/W
90h	18h	LSD1_DEL24	LSD1_DEL24[7:0]								00h	R/W
90h	19h	LSD1_DEL25	LSD1_DEL25[7:0]								00h	R/W

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
90h	1Ah	LSD1_DEL26	LSD1_DEL26[7:0]								00h	R/W
90h	1Bh	LSD1_DEL27	LSD1_DEL27[7:0]								00h	R/W
90h	1Ch	LSD1_DEL28	LSD1_DEL28[7:0]								00h	R/W
90h	1Dh	LSD1_DEL29	LSD1_DEL29[7:0]								00h	R/W
90h	1Eh	LSD1_DEL30	LSD1_DEL30[7:0]								00h	R/W
90h	1Fh	LSD1_DEL31	LSD1_DEL31[7:0]								00h	R/W
90h	20h	LSD1_DEL32	LSD1_DEL32[7:0]								00h	R/W
90h	21h	LSD1_DEL33	LSD1_DEL33[7:0]								00h	R/W
90h	22h	LSD1_DEL34	LSD1_DEL34[7:0]								00h	R/W
90h	23h	LSD1_DEL35	LSD1_DEL35[7:0]								00h	R/W
90h	24h	LSD1_DEL36	LSD1_DEL36[7:0]								00h	R/W
90h	25h	LSD1_DEL37	LSD1_DEL37[7:0]								00h	R/W
90h	26h	LSD1_DEL38	LSD1_DEL38[7:0]								00h	R/W
90h	27h	LSD1_DEL39	LSD1_DEL39[7:0]								00h	R/W
90h	28h	LSD1_DEL40	LSD1_DEL40[7:0]								00h	R/W
90h	29h	LSD1_DEL41	LSD1_DEL41[7:0]								00h	R/W
90h	2Ah	LSD1_DEL42	LSD1_DEL42[7:0]								00h	R/W
90h	2Bh	LSD1_DEL43	LSD1_DEL43[7:0]								00h	R/W
90h	2Ch	LSD1_DEL44	LSD1_DEL44[7:0]								00h	R/W
90h	2Dh	LSD1_DEL45	LSD1_DEL45[7:0]								00h	R/W
90h	2Eh	LSD1_DEL46	LSD1_DEL46[7:0]								00h	R/W
90h	2Fh	LSD1_DEL47	LSD1_DEL47[7:0]								00h	R/W
90h	30h	LSD1_DEL48	LSD1_DEL48[7:0]								00h	R/W
90h	31h	LSD1_DEL49	LSD1_DEL49[7:0]								00h	R/W
90h	32h	LSD1_DEL50	LSD1_DEL50[7:0]								00h	R/W
90h	33h	LSD1_DEL51	LSD1_DEL51[7:0]								00h	R/W
90h	34h	LSD1_DEL52	LSD1_DEL52[7:0]								00h	R/W
90h	35h	LSD1_DEL53	LSD1_DEL53[7:0]								00h	R/W
90h	36h	LSD1_DEL54	LSD1_DEL54[7:0]								00h	R/W
90h	37h	LSD1_DEL55	LSD1_DEL55[7:0]								00h	R/W
90h	38h	LSD1_DEL56	LSD1_DEL56[7:0]								00h	R/W
90h	39h	LSD1_DEL57	LSD1_DEL57[7:0]								00h	R/W
90h	3Ah	LSD1_DEL58	LSD1_DEL58[7:0]								00h	R/W
90h	3Bh	LSD1_DEL59	LSD1_DEL59[7:0]								00h	R/W
90h	3Ch	LSD1_DEL60	LSD1_DEL60[7:0]								00h	R/W
90h	3Dh	LSD1_DEL61	LSD1_DEL61[7:0]								00h	R/W

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
90h	3Eh	LSD1_DEL62	LSD1_DEL62[7:0]								00h	R/W
90h	3Fh	LSD1_DEL63	LSD1_DEL63[7:0]								00h	R/W
90h	FAh	PASSWORD0	PASSWORD0<7:0>								00h	R/W
90h	FBh	PASSWORD1	PASSWORD1<7:0>								00h	R/W
90h	FCh	PASSWORD2	PASSWORD2<7:0>								00h	R/W
90h	FDh	PASSWORD3	PASSWORD3<7:0>								00h	R/W
90h	FEh	PAGE	page[7:0]								00h	R/W
91h	00h	LSD2_DEL0	LSD2_DEL0[7:0]								00h	R/W
91h	01h	LSD2_DEL1	LSD2_DEL1[7:0]								00h	R/W
91h	02h	LSD2_DEL2	LSD2_DEL2[7:0]								00h	R/W
91h	03h	LSD2_DEL3	LSD2_DEL3[7:0]								00h	R/W
91h	04h	LSD2_DEL4	LSD2_DEL4[7:0]								00h	R/W
91h	05h	LSD2_DEL5	LSD2_DEL5[7:0]								00h	R/W
91h	06h	LSD2_DEL6	LSD2_DEL6[7:0]								00h	R/W
91h	07h	LSD2_DEL7	LSD2_DEL7[7:0]								00h	R/W
91h	08h	LSD2_DEL8	LSD2_DEL8[7:0]								00h	R/W
91h	09h	LSD2_DEL9	LSD2_DEL9[7:0]								00h	R/W
91h	0Ah	LSD2_DEL10	LSD2_DEL10[7:0]								00h	R/W
91h	0Bh	LSD2_DEL11	LSD2_DEL11[7:0]								00h	R/W
91h	0Ch	LSD2_DEL12	LSD2_DEL12[7:0]								00h	R/W
91h	0Dh	LSD2_DEL13	LSD2_DEL13[7:0]								00h	R/W
91h	0Eh	LSD2_DEL14	LSD2_DEL14[7:0]								00h	R/W
91h	0Fh	LSD2_DEL15	LSD2_DEL15[7:0]								00h	R/W
91h	10h	LSD2_DEL16	LSD2_DEL16[7:0]								00h	R/W
91h	11h	LSD2_DEL17	LSD2_DEL17[7:0]								00h	R/W
91h	12h	LSD2_DEL18	LSD2_DEL18[7:0]								00h	R/W
91h	13h	LSD2_DEL19	LSD2_DEL19[7:0]								00h	R/W
91h	14h	LSD2_DEL20	LSD2_DEL20[7:0]								00h	R/W
91h	15h	LSD2_DEL21	LSD2_DEL21[7:0]								00h	R/W
91h	16h	LSD2_DEL22	LSD2_DEL22[7:0]								00h	R/W
91h	17h	LSD2_DEL23	LSD2_DEL23[7:0]								00h	R/W
91h	18h	LSD2_DEL24	LSD2_DEL24[7:0]								00h	R/W
91h	19h	LSD2_DEL25	LSD2_DEL25[7:0]								00h	R/W
91h	1Ah	LSD2_DEL26	LSD2_DEL26[7:0]								00h	R/W
91h	1Bh	LSD2_DEL27	LSD2_DEL27[7:0]								00h	R/W
91h	1Ch	LSD2_DEL28	LSD2_DEL28[7:0]								00h	R/W

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
91h	1Dh	LSD2_DEL29	LSD2_DEL29[7:0]								00h	R/W
91h	1Eh	LSD2_DEL30	LSD2_DEL30[7:0]								00h	R/W
91h	1Fh	LSD2_DEL31	LSD2_DEL31[7:0]								00h	R/W
91h	20h	LSD2_DEL32	LSD2_DEL32[7:0]								00h	R/W
91h	21h	LSD2_DEL33	LSD2_DEL33[7:0]								00h	R/W
91h	22h	LSD2_DEL34	LSD2_DEL34[7:0]								00h	R/W
91h	23h	LSD2_DEL35	LSD2_DEL35[7:0]								00h	R/W
91h	24h	LSD2_DEL36	LSD2_DEL36[7:0]								00h	R/W
91h	25h	LSD2_DEL37	LSD2_DEL37[7:0]								00h	R/W
91h	26h	LSD2_DEL38	LSD2_DEL38[7:0]								00h	R/W
91h	27h	LSD2_DEL39	LSD2_DEL39[7:0]								00h	R/W
91h	28h	LSD2_DEL40	LSD2_DEL40[7:0]								00h	R/W
91h	29h	LSD2_DEL41	LSD2_DEL41[7:0]								00h	R/W
91h	2Ah	LSD2_DEL42	LSD2_DEL42[7:0]								00h	R/W
91h	2Bh	LSD2_DEL43	LSD2_DEL43[7:0]								00h	R/W
91h	2Ch	LSD2_DEL44	LSD2_DEL44[7:0]								00h	R/W
91h	2Dh	LSD2_DEL45	LSD2_DEL45[7:0]								00h	R/W
91h	2Eh	LSD2_DEL46	LSD2_DEL46[7:0]								00h	R/W
91h	2Fh	LSD2_DEL47	LSD2_DEL47[7:0]								00h	R/W
91h	30h	LSD2_DEL48	LSD2_DEL48[7:0]								00h	R/W
91h	31h	LSD2_DEL49	LSD2_DEL49[7:0]								00h	R/W
91h	32h	LSD2_DEL50	LSD2_DEL50[7:0]								00h	R/W
91h	33h	LSD2_DEL51	LSD2_DEL51[7:0]								00h	R/W
91h	34h	LSD2_DEL52	LSD2_DEL52[7:0]								00h	R/W
91h	35h	LSD2_DEL53	LSD2_DEL53[7:0]								00h	R/W
91h	36h	LSD2_DEL54	LSD2_DEL54[7:0]								00h	R/W
91h	37h	LSD2_DEL55	LSD2_DEL55[7:0]								00h	R/W
91h	38h	LSD2_DEL56	LSD2_DEL56[7:0]								00h	R/W
91h	39h	LSD2_DEL57	LSD2_DEL57[7:0]								00h	R/W
91h	3Ah	LSD2_DEL58	LSD2_DEL58[7:0]								00h	R/W
91h	3Bh	LSD2_DEL59	LSD2_DEL59[7:0]								00h	R/W
91h	3Ch	LSD2_DEL60	LSD2_DEL60[7:0]								00h	R/W
91h	3Dh	LSD2_DEL61	LSD2_DEL61[7:0]								00h	R/W
91h	3Eh	LSD2_DEL62	LSD2_DEL62[7:0]								00h	R/W
91h	3Fh	LSD2_DEL63	LSD2_DEL63[7:0]								00h	R/W
91h	FAh	PASSWORD0	PASSWORD0<7:0>								00h	R/W

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
91h	FBh	PASSWORD1	PASSWORD1<7:0>								00h	R/W
91h	FCh	PASSWORD2	PASSWORD2<7:0>								00h	R/W
91h	FDh	PASSWORD3	PASSWORD3<7:0>								00h	R/W
91h	FEh	PAGE	page[7:0]								00h	R/W
92h	00h	LSD3_DEL0	LSD3_DEL0[7:0]								00h	R/W
92h	01h	LSD3_DEL1	LSD3_DEL1[7:0]								00h	R/W
92h	02h	LSD3_DEL2	LSD3_DEL2[7:0]								00h	R/W
92h	03h	LSD3_DEL3	LSD3_DEL3[7:0]								00h	R/W
92h	04h	LSD3_DEL4	LSD3_DEL4[7:0]								00h	R/W
92h	05h	LSD3_DEL5	LSD3_DEL5[7:0]								00h	R/W
92h	06h	LSD3_DEL6	LSD3_DEL6[7:0]								00h	R/W
92h	07h	LSD3_DEL7	LSD3_DEL7[7:0]								00h	R/W
92h	08h	LSD3_DEL8	LSD3_DEL8[7:0]								00h	R/W
92h	09h	LSD3_DEL9	LSD3_DEL9[7:0]								00h	R/W
92h	0Ah	LSD3_DEL10	LSD3_DEL10[7:0]								00h	R/W
92h	0Bh	LSD3_DEL11	LSD3_DEL11[7:0]								00h	R/W
92h	0Ch	LSD3_DEL12	LSD3_DEL12[7:0]								00h	R/W
92h	0Dh	LSD3_DEL13	LSD3_DEL13[7:0]								00h	R/W
92h	0Eh	LSD3_DEL14	LSD3_DEL14[7:0]								00h	R/W
92h	0Fh	LSD3_DEL15	LSD3_DEL15[7:0]								00h	R/W
92h	10h	LSD3_DEL16	LSD3_DEL16[7:0]								00h	R/W
92h	11h	LSD3_DEL17	LSD3_DEL17[7:0]								00h	R/W
92h	12h	LSD3_DEL18	LSD3_DEL18[7:0]								00h	R/W
92h	13h	LSD3_DEL19	LSD3_DEL19[7:0]								00h	R/W
92h	14h	LSD3_DEL20	LSD3_DEL20[7:0]								00h	R/W
92h	15h	LSD3_DEL21	LSD3_DEL21[7:0]								00h	R/W
92h	16h	LSD3_DEL22	LSD3_DEL22[7:0]								00h	R/W
92h	17h	LSD3_DEL23	LSD3_DEL23[7:0]								00h	R/W
92h	18h	LSD3_DEL24	LSD3_DEL24[7:0]								00h	R/W
92h	19h	LSD3_DEL25	LSD3_DEL25[7:0]								00h	R/W
92h	1Ah	LSD3_DEL26	LSD3_DEL26[7:0]								00h	R/W
92h	1Bh	LSD3_DEL27	LSD3_DEL27[7:0]								00h	R/W
92h	1Ch	LSD3_DEL28	LSD3_DEL28[7:0]								00h	R/W
92h	1Dh	LSD3_DEL29	LSD3_DEL29[7:0]								00h	R/W
92h	1Eh	LSD3_DEL30	LSD3_DEL30[7:0]								00h	R/W
92h	1Fh	LSD3_DEL31	LSD3_DEL31[7:0]								00h	R/W

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
92h	20h	LSD3_DEL32	LSD3_DEL32[7:0]								00h	R/W
92h	21h	LSD3_DEL33	LSD3_DEL33[7:0]								00h	R/W
92h	22h	LSD3_DEL34	LSD3_DEL34[7:0]								00h	R/W
92h	23h	LSD3_DEL35	LSD3_DEL35[7:0]								00h	R/W
92h	24h	LSD3_DEL36	LSD3_DEL36[7:0]								00h	R/W
92h	25h	LSD3_DEL37	LSD3_DEL37[7:0]								00h	R/W
92h	26h	LSD3_DEL38	LSD3_DEL38[7:0]								00h	R/W
92h	27h	LSD3_DEL39	LSD3_DEL39[7:0]								00h	R/W
92h	28h	LSD3_DEL40	LSD3_DEL40[7:0]								00h	R/W
92h	29h	LSD3_DEL41	LSD3_DEL41[7:0]								00h	R/W
92h	2Ah	LSD3_DEL42	LSD3_DEL42[7:0]								00h	R/W
92h	2Bh	LSD3_DEL43	LSD3_DEL43[7:0]								00h	R/W
92h	2Ch	LSD3_DEL44	LSD3_DEL44[7:0]								00h	R/W
92h	2Dh	LSD3_DEL45	LSD3_DEL45[7:0]								00h	R/W
92h	2Eh	LSD3_DEL46	LSD3_DEL46[7:0]								00h	R/W
92h	2Fh	LSD3_DEL47	LSD3_DEL47[7:0]								00h	R/W
92h	30h	LSD3_DEL48	LSD3_DEL48[7:0]								00h	R/W
92h	31h	LSD3_DEL49	LSD3_DEL49[7:0]								00h	R/W
92h	32h	LSD3_DEL50	LSD3_DEL50[7:0]								00h	R/W
92h	33h	LSD3_DEL51	LSD3_DEL51[7:0]								00h	R/W
92h	34h	LSD3_DEL52	LSD3_DEL52[7:0]								00h	R/W
92h	35h	LSD3_DEL53	LSD3_DEL53[7:0]								00h	R/W
92h	36h	LSD3_DEL54	LSD3_DEL54[7:0]								00h	R/W
92h	37h	LSD3_DEL55	LSD3_DEL55[7:0]								00h	R/W
92h	38h	LSD3_DEL56	LSD3_DEL56[7:0]								00h	R/W
92h	39h	LSD3_DEL57	LSD3_DEL57[7:0]								00h	R/W
92h	3Ah	LSD3_DEL58	LSD3_DEL58[7:0]								00h	R/W
92h	3Bh	LSD3_DEL59	LSD3_DEL59[7:0]								00h	R/W
92h	3Ch	LSD3_DEL60	LSD3_DEL60[7:0]								00h	R/W
92h	3Dh	LSD3_DEL61	LSD3_DEL61[7:0]								00h	R/W
92h	3Eh	LSD3_DEL62	LSD3_DEL62[7:0]								00h	R/W
92h	3Fh	LSD3_DEL63	LSD3_DEL63[7:0]								00h	R/W
92h	FAh	PASSWORD0	PASSWORD0<7:0>								00h	R/W
92h	FBh	PASSWORD1	PASSWORD1<7:0>								00h	R/W
92h	FCh	PASSWORD2	PASSWORD2<7:0>								00h	R/W
92h	FDh	PASSWORD3	PASSWORD3<7:0>								00h	R/W

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
92h	FEh	PAGE	page[7:0]								00h	R/W
93h	00h	LSD4_DEL0	LSD4_DEL0[7:0]								00h	R/W
93h	01h	LSD4_DEL1	LSD4_DEL1[7:0]								00h	R/W
93h	02h	LSD4_DEL2	LSD4_DEL2[7:0]								00h	R/W
93h	03h	LSD4_DEL3	LSD4_DEL3[7:0]								00h	R/W
93h	04h	LSD4_DEL4	LSD4_DEL4[7:0]								00h	R/W
93h	05h	LSD4_DEL5	LSD4_DEL5[7:0]								00h	R/W
93h	06h	LSD4_DEL6	LSD4_DEL6[7:0]								00h	R/W
93h	07h	LSD4_DEL7	LSD4_DEL7[7:0]								00h	R/W
93h	08h	LSD4_DEL8	LSD4_DEL8[7:0]								00h	R/W
93h	09h	LSD4_DEL9	LSD4_DEL9[7:0]								00h	R/W
93h	0Ah	LSD4_DEL10	LSD4_DEL10[7:0]								00h	R/W
93h	0Bh	LSD4_DEL11	LSD4_DEL11[7:0]								00h	R/W
93h	0Ch	LSD4_DEL12	LSD4_DEL12[7:0]								00h	R/W
93h	0Dh	LSD4_DEL13	LSD4_DEL13[7:0]								00h	R/W
93h	0Eh	LSD4_DEL14	LSD4_DEL14[7:0]								00h	R/W
93h	0Fh	LSD4_DEL15	LSD4_DEL15[7:0]								00h	R/W
93h	10h	LSD4_DEL16	LSD4_DEL16[7:0]								00h	R/W
93h	11h	LSD4_DEL17	LSD4_DEL17[7:0]								00h	R/W
93h	12h	LSD4_DEL18	LSD4_DEL18[7:0]								00h	R/W
93h	13h	LSD4_DEL19	LSD4_DEL19[7:0]								00h	R/W
93h	14h	LSD4_DEL20	LSD4_DEL20[7:0]								00h	R/W
93h	15h	LSD4_DEL21	LSD4_DEL21[7:0]								00h	R/W
93h	16h	LSD4_DEL22	LSD4_DEL22[7:0]								00h	R/W
93h	17h	LSD4_DEL23	LSD4_DEL23[7:0]								00h	R/W
93h	18h	LSD4_DEL24	LSD4_DEL24[7:0]								00h	R/W
93h	19h	LSD4_DEL25	LSD4_DEL25[7:0]								00h	R/W
93h	1Ah	LSD4_DEL26	LSD4_DEL26[7:0]								00h	R/W
93h	1Bh	LSD4_DEL27	LSD4_DEL27[7:0]								00h	R/W
93h	1Ch	LSD4_DEL28	LSD4_DEL28[7:0]								00h	R/W
93h	1Dh	LSD4_DEL29	LSD4_DEL29[7:0]								00h	R/W
93h	1Eh	LSD4_DEL30	LSD4_DEL30[7:0]								00h	R/W
93h	1Fh	LSD4_DEL31	LSD4_DEL31[7:0]								00h	R/W
93h	20h	LSD4_DEL32	LSD4_DEL32[7:0]								00h	R/W
93h	21h	LSD4_DEL33	LSD4_DEL33[7:0]								00h	R/W
93h	22h	LSD4_DEL34	LSD4_DEL34[7:0]								00h	R/W

Table 4-1. Register Summary

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
93h	23h	LSD4_DEL35	LSD4_DEL35[7:0]								00h	R/W
93h	24h	LSD4_DEL36	LSD4_DEL36[7:0]								00h	R/W
93h	25h	LSD4_DEL37	LSD4_DEL37[7:0]								00h	R/W
93h	26h	LSD4_DEL38	LSD4_DEL38[7:0]								00h	R/W
93h	27h	LSD4_DEL39	LSD4_DEL39[7:0]								00h	R/W
93h	28h	LSD4_DEL40	LSD4_DEL40[7:0]								00h	R/W
93h	29h	LSD4_DEL41	LSD4_DEL41[7:0]								00h	R/W
93h	2Ah	LSD4_DEL42	LSD4_DEL42[7:0]								00h	R/W
93h	2Bh	LSD4_DEL43	LSD4_DEL43[7:0]								00h	R/W
93h	2Ch	LSD4_DEL44	LSD4_DEL44[7:0]								00h	R/W
93h	2Dh	LSD4_DEL45	LSD4_DEL45[7:0]								00h	R/W
93h	2Eh	LSD4_DEL46	LSD4_DEL46[7:0]								00h	R/W
93h	2Fh	LSD4_DEL47	LSD4_DEL47[7:0]								00h	R/W
93h	30h	LSD4_DEL48	LSD4_DEL48[7:0]								00h	R/W
93h	31h	LSD4_DEL49	LSD4_DEL49[7:0]								00h	R/W
93h	32h	LSD4_DEL50	LSD4_DEL50[7:0]								00h	R/W
93h	33h	LSD4_DEL51	LSD4_DEL51[7:0]								00h	R/W
93h	34h	LSD4_DEL52	LSD4_DEL52[7:0]								00h	R/W
93h	35h	LSD4_DEL53	LSD4_DEL53[7:0]								00h	R/W
93h	36h	LSD4_DEL54	LSD4_DEL54[7:0]								00h	R/W
93h	37h	LSD4_DEL55	LSD4_DEL55[7:0]								00h	R/W
93h	38h	LSD4_DEL56	LSD4_DEL56[7:0]								00h	R/W
93h	39h	LSD4_DEL57	LSD4_DEL57[7:0]								00h	R/W
93h	3Ah	LSD4_DEL58	LSD4_DEL58[7:0]								00h	R/W
93h	3Bh	LSD4_DEL59	LSD4_DEL59[7:0]								00h	R/W
93h	3Ch	LSD4_DEL60	LSD4_DEL60[7:0]								00h	R/W
93h	3Dh	LSD4_DEL61	LSD4_DEL61[7:0]								00h	R/W
93h	3Eh	LSD4_DEL62	LSD4_DEL62[7:0]								00h	R/W
93h	3Fh	LSD4_DEL63	LSD4_DEL63[7:0]								00h	R/W
93h	FAh	PASSWORD0	PASSWORD0<7:0>								00h	R/W
93h	FBh	PASSWORD1	PASSWORD1<7:0>								00h	R/W

Page: 00h
Address: 00h
Default: 55h
Description: checksumseed

Bit(s)	Name	Description	Default	Type
7:0	checksumseed<7:0>		01010101b	R/W

Page: 00h
Address: 03h
Default: 10h
Description: LSD1 LUT_GATE baseline register

Bit(s)	Name	Description	Default	Type
7:6	*RSVD*		00b	R/W
5	LSD1_BYPASS	1:use Baseline always for DAC output, 0,normal working	0b	R/W
4	LSD1_POL	LSD output 1=pos/increase byt LUT/TEMP,0=neg/decrease by LUT/TEMP	1b	R/W
3:0	LSD1_BASE<3:0>	LSD1 basline LSB	0000b	R/W

Page: 00h
Address: 04h
Default: 99h
Description: LSD1 LUT_GATE baseline register

Bit(s)	Name	Description	Default	Type
7:0	LSD1_BASE<11:4>	LSD1 basline LSB	10011001b	R/W

Page: 00h
Address: 05h
Default: 1Ah
Description: store the address of the LUT_VOLT which baseline of temperature is store, a value between 0-63

Bit(s)	Name	Description	Default	Type
7:0	LSD1_LUTV_BS_ADD<7:0>	Address of the baseline in the LSD1_DEL	00011010b	R/W

Page: 00h
Address: 06h
Default: 10h
Description: LSD2 LUT_GATE baseline register

Bit(s)	Name	Description	Default	Type
7:6	*RSVD*		00b	R/W
5	LSD2_BYPASS	1:use Baseline always for DAC output, 0,normal working	0b	R/W
4	LSD2_POL	LSD output 1=pos/increase byt LUT/TEMP,0=neg/decrease by LUT/TEMP	1b	R/W
3:0	LSD2_BASE<3:0>	LSD2 basline LSB	0000b	R/W

Page: 00h
Address: 07h
Default: 99h
Description: LSD2 LUT_GATE baseline register

Bit(s)	Name	Description	Default	Type
7:0	LSD2_BASE<11:4>	LSD2 basline LSB	10011001b	R/W

Page: 00h
Address: 08h
Default: 1Ah
Description: store the address of the LUT_VOLT which baseline of temperature is store, a value between 0-63

Bit(s)	Name	Description	Default	Type
7:0	LSD2_LUTV_BS_ADD<7:0>	Address of the baseline in the LSD2_DEL	00011010b	R/W

Page: 00h
Address: 09h
Default: 10h
Description: LSD3 LUT_GATE baseline register

Bit(s)	Name	Description	Default	Type
7:6	*RSVD*		00b	R/W
5	LSD3_BYPASS	1:use Baseline always for DAC output, 0,normal working	0b	R/W
4	LSD3_POL	LSD output 1=pos/increase byt LUT/TEMP,0=neg/decrease by LUT/TEMP	1b	R/W
3:0	LSD3_BASE<3:0>	LSD3 basline LSB	0000b	R/W

Page: 00h
Address: 0Ah
Default: 99h
Description: LSD3 LUT_GATE baseline register

Bit(s)	Name	Description	Default	Type
7:0	LSD3_BASE<11:4>	LSD3 basline LSB	10011001b	R/W

Page: 00h
Address: 0Bh
Default: 1Ah
Description: store the address of the LUT_VOLT which baseline of temperature is store, a value between 0-63.Default is 25C

Bit(s)	Name	Description	Default	Type
7:0	LSD3_LUTV_BS_ADD<7:0>	Address of the baseline in the LSD3_DEL	00011010b	R/W

Page: 00h
Address: 0Ch
Default: 10h
Description: LSD4 LUT_GATE baseline register

Bit(s)	Name	Description	Default	Type
7:6	*RSVD*		00b	R/W
5	LSD4_BYPASS	1:use Baseline always for DAC output, 0,normal working	0b	R/W
4	LSD4_POL	LSD output 1=pos/increase byt LUT/TEMP,0=neg/decrease by LUT/TEMP	1b	R/W
3:0	LSD4_BASE<3:0>	LSD4 basline LSB	0000b	R/W

Page: 00h
Address: 0Dh
Default: 99h
Description: LSD4 LUT_GATE baseline register

Bit(s)	Name	Description	Default	Type
7:0	LSD4_BASE<11:4>	LSD4 basline LSB	10011001b	R/W

Page: 00h
Address: 0Eh
Default: 1Ah
Description: store the address of the LUT_VOLT which baseline of temperature is store, a value between 0-63

Bit(s)	Name	Description	Default	Type
7:0	LSD4_LUTV_BS_ADD<7:0>	Address of the baseline in the LSD4_DEL	00011010b	R/W

Page: 00h
Address: 0Fh
Default: 68h
Description: Store the temperature when the baseline for LUT_TEMP and LUT_VOLTare extracted;12 bit

Bit(s)	Name	Description	Default	Type
7:0	LUT_TEMP_BS_TEMP<11:4>		01101000b	R/W

Page: 00h
Address: 10h
Default: 00h
Description: Store the temperature when the baseline for LUT_TEMP and LUT_VOLTare extracted;12 bit

Bit(s)	Name	Description	Default	Type
7:4	LUT_TEMP_BS_TEMP<3:0>		00000000b	R/W
3:0	*RSVD*			R/W

Page: 00h
Address: 11h
Default: 97h
Description: Store the address of the LUT_TEMP which BASE value is stored, a value between 0-255.Default is 104 which gives -40+104*0.625=25C

Bit(s)	Name	Description	Default	Type
7:0	LUT_TEMP_BS_ADD<7:0>		10010111b	R/W

Page: 00h
Address: 12h
Default: 89h
Description: Store the LUT_TEMP MSB of the baseline ADC reading for LSD1 TEMP pin

Bit(s)	Name	Description	Default	Type
7:0	LSD1_TS_BS<11:4>		10001001b	R/W

Page: 00h
Address: 13h
Default: 89h
Description: Store the LUT_TEMP MSB of the baseline ADC reading for LSD2 TEMP pin

Bit(s)	Name	Description	Default	Type
7:0	LSD2_TS_BS<11:4>		10001001b	R/W

Page: 00h
Address: 14h
Default: 22h
Description: Store the LUT_TEMP LSB of the baseline ADC reading for LSD1/2 TEMP pin

Bit(s)	Name	Description	Default	Type
7:4	LSD2_TS_BS<3:0>		0010b	R/W
3:0	LSD1_TS_BS<3:0>		0010b	R/W

Page: 00h
Address: 15h
Default: 89h
Description: Store the LUT_TEMP MSB of the baseline ADC reading for LSD3 TEMP pin

Bit(s)	Name	Description	Default	Type
7:0	LSD3_TS_BS<11:4>		10001001b	R/W

Page: 00h
Address: 16h
Default: 89h
Description: Store LUT_TEMP MSB of the baseline ADC readingfor LSD4 TEMP pin

Bit(s)	Name	Description	Default	Type
7:0	LSD4_TS_BS<11:4>		10001001b	R/W

Page: 00h
Address: 17h
Default: 22h
Description: Store the LUT_TEMP LSB of baseline ADC reading for T=25C for LSD3and LSD4 TEMP pin

Bit(s)	Name	Description	Default	Type
7:4	LSD4_TS_BS<3:0>		0010b	R/W
3:0	LSD3_TS_BS<3:0>		0010b	R/W

Page: 00h
Address: 1Fh
Default: 64h
Description: write 6xH to show it is a macom part

Bit(s)	Name	Description	Default	Type
7:4	*RSVD*	*Reserved*	0110b	R/W
3:0	VERSION<3:0>	Version number	0100b	R/W

Page: 00h
Address: 33h
Default: FFh
Description: input select of ADC,power down LSDx_TEMP also mean the disable the coresponds TS. Disable one channel means the next channel will take place of it. For example, if only one channel is left, then ADC will keep sample it.Digital need to send a enable signal at the previous channel of a current sense channel to garantee the settling time

Bit(s)	Name	Description	Default	Type
7	EN_LSD3_OUTN	0=disable, 1=enable	1b	R/W
6	EN_LSD2_OUTN	0=disable, 1=enable	1b	R/W
5	EN_LSD1_OUTN	0=disable, 1=enable	1b	R/W
4	EN_LSD4_OUTP	0=disable, 1=enable	1b	R/W
3	EN_LSD3_OUTP	0=disable, 1=enable	1b	R/W
2	EN_LSD2_OUTP	0=disable, 1=enable	1b	R/W
1	EN_LSD1_OUTP	0=disable, 1=enable	1b	R/W
0	*RSVD*	*Reserved*	1b	R/W

Page: 00h
Address: 5Bh
Default: 00h
Description: control the adc in manual mode

Bit(s)	Name	Description	Default	Type
7	mux_sel_I	Control the mux for current channel	0b	R/W
6	mux_sel_v	Control the mux for voltage channel	0b	R/W
5	adc_iext_sel	Select the iext from externa l to internal	0b	R/W
4	adc_override	1:copy adc_dac<11:0> to all adc chnl beside chnl 0,11, 0: don't copy	0b	R/W
3:2	adc_tiagain<1:0>	Control the tia gain in adc	00b	R/W
1:0	adc_vdiv<1:0>	Control the voltage diverider in adc	00b	R/W

Page: 00h
Address: 65h
Default: 8Bh
Description: LSD1 driver control bytes;- DISABLED mode, where the LSDs are disabled and the gates are not connected to the buffers
- SAFE mode, where the LSDs are enabled but the gates are connected to the negative supply (or whatever the lower limit is specified)
- LIVE mode, where the LSDs are enabled and their output is connected to the gates

Bit(s)	Name	Description	Default	Type
7	LSD1_CL<2>	set the current limit threshold from 20mA to 140mA with 30mA per step,LSDx_CL<2:0>=<111> To disbale current limitor	1b	R/W
6	LSD1_CL<1>	Set the current limit threshold from 20mA to 140mA with 30mA per step	0b	R/W
5	LSD1_CL<0>	Set the current limit threshold from 20mA to 140mA with 30mA per step	0b	R/W
4	*RSVD*	*Reserved*	0b	R/W
3	*RSVD*	*Reserved*	1b	R/W
2	LSD1_5G_OPAMP_EN	LSD_5G_OPAMP_EN" is only used in the 5G mode, and doesn't affect the switch states in the RFE mode. When "LSD_5G_OPAMP_EN" is "1", the OP AMP will be enabled and the OP AMP feedback path will be internally connected in the standby mode, even though "EN" is low. When "LSD_5G_OPAMP_EN" is "0" (and "EN" is "0"), the OP AMP will be disabled, and the OP AMP output will be pulled down to VNEG.	0b	R/W
1	LSD1_5G_ENB	Mode bit, 0 for 5G,1 for RFE	1b	R/W
0	LSD1_REG_EN	Digital LSD enable	1b	R/W

Page: 00h
Address: 66h
Default: 00h
Description: LSD1 driver control bytes; - Current sense of PMOS/NMOS and resistor setting on the DAC output path.

Bit(s)	Name	Description	Default	Type
7	*RSVD*	*Reserved*	0b	R/W
6	LSD1_CSP_EN	Write 1 to enable the current sense of PMOS in the LSD driver	0b	R/W
5	LSD1_CSN_EN	Write 1 to enable the current sense of NMOS in the LSD driver	0b	R/W
4	*RSVD*	*Reserved*	0b	R/W
3:2	LSD1_Rset<1:0>	set the resistor on the DAC output path:00:15K, 01:12.5K,10:13.75K,11:11.25K	00b	R/W
1	*RSVD*	*Reserved*	0b	R/W
0	*RSVD*	*Reserved*	0b	R/W

Page: 00h
Address: 67h
Default: 8Bh
Description: LSD2 driver control bytes;- DISABLED mode, where the LSDs are disabled and the gates are not connected to the buffers
- SAFE mode, where the LSDs are enabled but the gates are connected to the negative supply (or whatever the lower limit is specified)
- LIVE mode, where the LSDs are enabled and their output is connected to the gates

Bit(s)	Name	Description	Default	Type
7	LSD2_CL<2>	set the current limit threshold from 20mA to 140mA with 30mA per step,LSDx_CL<2:0>=<111> To disbale current limitor	1b	R/W
6	LSD2_CL<1>	Set the current limit threshold from 20mA to 140mA with 30mA per step	0b	R/W
5	LSD2_CL<0>	Set the current limit threshold from 20mA to 140mA with 30mA per step	0b	R/W
4	*RSVD*	*Reserved*	0b	R/W
3	*RSVD*	*Reserved*	1b	R/W
2	LSD2_5G_OPAMP_EN	LSD_5G_OPAMP_EN" is only used in the 5G mode, and doesn't affect the switch states in the RFE mode. When "LSD_5G_OPAMP_EN" is "1", the OP AMP will be enabled and the OP AMP feedback path will be internally connected in the standby mode, even though "EN" is low. When "LSD_5G_OPAMP_EN" is "0" (and "EN" is "0"), the OP AMP will be disabled, and the OP AMP output will be pulled down to VNEG.	0b	R/W
1	LSD2_5G_ENB	Mode bit, 0 for 5G,1 for RFE	1b	R/W
0	LSD2_REG_EN	Digital LSD enable	1b	R/W

Page: 00h
Address: 68h
Default: 00h
Description: LSD2 driver control bytes; - Current sense of PMOS/NMOS and resistor setting on the DAC output path.

Bit(s)	Name	Description	Default	Type
7	*RSVD*	*Reserved*	0b	R/W
6	LSD2_CSP_EN	Write 1 to enable the current sense of PMOS in the LSD driver	0b	R/W
5	LSD2_CSN_EN	Write 1 to enable the current sense of NMOS in the LSD driver	0b	R/W
4	*RSVD*	*Reserved*	0b	R/W
3:2	LSD2_Rset<1:0>	set the resistor on the DAC output path:00:15K, 01:12.5K,10:13.75K,11:11.25K	00b	R/W
1	*RSVD*	*Reserved*	0b	R/W
0	*RSVD*	*Reserved*	0b	R/W

Page: 00h
Address: 69h
Default: 8Bh
Description: LSD3 driver control bytes;- DISABLED mode, where the LSDs are disabled and the gates are not connected to the buffers
- SAFE mode, where the LSDs are enabled but the gates are connected to the negative supply (or whatever the lower limit is specified)
- LIVE mode, where the LSDs are enabled and their output is connected to the gates

Bit(s)	Name	Description	Default	Type
7	LSD3_CL<2>	set the current limit threshold from 20mA to 140mA with 30mA per step,LSDx_CL<2:0>=<111> To disbale current limitor	1b	R/W
6	LSD3_CL<1>	Set the current limit threshold from 20mA to 140mA with 30mA per step	0b	R/W
5	LSD3_CL<0>	Set the current limit threshold from 20mA to 140mA with 30mA per step	0b	R/W
4	*RSVD*	*Reserved*	0b	R/W
3	*RSVD*	*Reserved*	1b	R/W
2	LSD3_5G_OPAMP_EN	LSD_5G_OPAMP_EN" is only used in the 5G mode, and doesn't affect the switch states in the RFE mode. When "LSD_5G_OPAMP_EN" is "1", the OP AMP will be enabled and the OP AMP feedback path will be internally connected in the standby mode, even though "EN" is low. When "LSD_5G_OPAMP_EN" is "0" (and "EN" is "0"), the OP AMP will be disabled, and the OP AMP output will be pulled down to VNEG.	0b	R/W
1	LSD3_5G_ENB	Mode bit, 0 for 5G,1 for RFE	1b	R/W
0	LSD3_REG_EN	Digital LSD enable	1b	R/W

Page: 00h
Address: 6Ah
Default: 00h
Description: LSD3 driver control bytes; - Current sense of PMOS/NMOS and resistor setting on the DAC output path.

Bit(s)	Name	Description	Default	Type
7	*RSVD*	*Reserved*	0b	R/W
6	LSD3_CSP_EN	Write 1 to enable the current sense of PMOS in the LSD driver	0b	R/W
5	LSD3_CSN_EN	Write 1 to enable the current sense of NMOS in the LSD driver	0b	R/W
4	*RSVD*	*Reserved*	0b	R/W
3:2	LSD3_Rset<1:0>	set the resistor on the DAC output path:00:15K, 01:12.5K,10:13.75K,11:11.25K	00b	R/W
1	*RSVD*	*Reserved*	0b	R/W
0	*RSVD*	*Reserved*	0b	R/W

Page: 00h
Address: 6Bh
Default: 8Bh
Description: LSD4 driver control bytes;- DISABLED mode, where the LSDs are disabled and the gates are not connected to the buffers
- SAFE mode, where the LSDs are enabled but the gates are connected to the negative supply (or whatever the lower limit is specified)
- LIVE mode, where the LSDs are enabled and their output is connected to the gates

Bit(s)	Name	Description	Default	Type
7	LSD4_CL<2>	set the current limit threshold from 20mA to 140mA with 30mA per step,LSDx_CL<2:0>=<111> To disbale current limitor	1b	R/W
6	LSD4_CL<1>	Set the current limit threshold from 20mA to 140mA with 30mA per step	0b	R/W
5	LSD4_CL<0>	Set the current limit threshold from 20mA to 140mA with 30mA per step	0b	R/W
4	*RSVD*	*Reserved*	0b	R/W
3	*RSVD*	*Reserved*	1b	R/W
2	LSD4_5G_OPAMP_EN	LSD_5G_OPAMP_EN" is only used in the 5G mode, and doesn't affect the switch states in the RFE mode. When "LSD_5G_OPAMP_EN" is "1", the OP AMP will be enabled and the OP AMP feedback path will be internally connected in the standby mode, even though "EN" is low. When "LSD_5G_OPAMP_EN" is "0" (and "EN" is "0"), the OP AMP will be disabled, and the OP AMP output will be pulled down to VNEG.	0b	R/W
1	LSD4_5G_ENB	Mode bit, 0 for 5G,1 for RFE	1b	R/W
0	LSD4_REG_EN	Digital LSD enable	1b	R/W

Page: 00h
Address: 6Ch
Default: 00h
Description: LSD4 driver control bytes; - Current sense of PMOS/NMOS and resistor setting on the DAC output path.

Bit(s)	Name	Description	Default	Type
7	*RSVD*	*Reserved*	0b	R/W
6	LSD4_CSP_EN	Write 1 to enable the current sense of PMOS in the LSD driver	0b	R/W
5	LSD4_CSN_EN	Write 1 to enable the current sense of NMOS in the LSD driver	0b	R/W
4	*RSVD*	*Reserved*	0b	R/W
3:2	LSD4_Rset<1:0>	set the resistor on the DAC output path:00:15K, 01:12.5K,10:13.75K,11:11.25K	00b	R/W
1	*RSVD*	*Reserved*	0b	R/W
0	*RSVD*	*Reserved*	0b	R/W

Page: 00h
Address: 6Dh
Default: 00h
Description: Normal working , the codes to DAC are digital generated. Write to following bytes will override the generated control bytes. Override control register form 4x DAC

Bit(s)	Name	Description	Default	Type
7:4	DAC_ORD <3:0>	LSD4,LSD3,LSD2,LSD1;1=Override,0=not overide	0000b	R/W
3:0	TEMP_ORD <3:0>	Use the data in OFFCHIP_TEMP<11:0> To override the cal_tsx<11:0> , LSD4,LSD3,LSD2,LSD1;1=Override,0=not overide	0000b	R/W

Page: 00h
Address: 6Eh
Default: 00h
Description: MSB of the DAC for LSD1 from digital

Bit(s)	Name	Description	Default	Type
7:0	DAC_LSD1<11:4>		00000000b	R

Page: 00h
Address: 6Fh
Default: 00h
Description: LSB of the DAC for LSD1 from digital

Bit(s)	Name	Description	Default	Type
7:4	DAC_LSD1<3:0>	LSB of the DAC for the out LSD1	0000b	R
3:0	*RSVD*		0000b	R

Page: 00h
Address: 70h
Default: FFh
Description: Override MSB of LSD1 from GUI

Bit(s)	Name	Description	Default	Type
7:0	DAC_LSD1_ORD<11:4>		11111111b	R/W

Page: 00h
Address: 71h
Default: F0h
Description: Override LSB of LSD1 from GUI

Bit(s)	Name	Description	Default	Type
7:4	DAC_LSD1_ORD<3:0>		1111b	R/W
3:0	*RSVD*		0000b	R/W

Page: 00h
Address: 72h
Default: 00h
Description: MSB of the DAC for output LSD2 from digital

Bit(s)	Name	Description	Default	Type
7:0	DAC_LSD2<11:4>		00000000b	R

Page: 00h
Address: 73h
Default: 00h
Description: LSB of the DAC for output LSD2 from digital

Bit(s)	Name	Description	Default	Type
7:4	DAC_LSD2 <3:0>	LSB of the DAC for output LSD2 from digital	0000b	R
3:0	*RSVD*		0000b	R

Page: 00h
Address: 74h
Default: FFh
Description: Override MSB of LSD2 from GUI

Bit(s)	Name	Description	Default	Type
7:0	DAC_LSD2_ORD<11:4>		11111111b	R/W

Page: 00h
Address: 75h
Default: F0h
Description: Override LSB of LSD2 from GUI

Bit(s)	Name	Description	Default	Type
7:4	DAC_LSD2_ORD<3:0>		1111b	R/W
3:0	*RSVD*		0000b	R/W

Page: 00h
Address: 76h
Default: 00h
Description: MSB of the DAC for output LSD3 from digital

Bit(s)	Name	Description	Default	Type
7:0	DAC_LSD3<11:4>		00000000b	R

Page: 00h
Address: 77h
Default: 00h
Description: LSB of the DAC for output LSD2 from digital

Bit(s)	Name	Description	Default	Type
7:4	DAC_LSD3<3:0>		0000b	R
3:0	*RSVD*		0000b	R

Page: 00h
Address: 78h
Default: FFh
Description: override MSB of LSD3 from GUI

Bit(s)	Name	Description	Default	Type
7:0	DAC_LSD3_ORD<11:4>		11111111b	R/W

Page: 00h
Address: 79h
Default: F0h
Description: override LSB of LSD3 from GUI

Bit(s)	Name	Description	Default	Type
7:4	DAC_LSD3_ORD<3:0>		1111b	R/W
3:0	*RSVD*		0000b	R/W

Page: 00h
Address: 7Ah
Default: 00h
Description: MSB of the DAC for output LSD4 from digital

Bit(s)	Name	Description	Default	Type
7:0	DAC_LSD4<11:4>		00000000b	R

Page: 00h
Address: 7Bh
Default: 00h
Description: LSB of the DAC for output LSD4 from digital

Bit(s)	Name	Description	Default	Type
7:4	DAC_LSD4<3:0>		0000b	R
3:0	*RSVD*		0000b	R

Page: 00h
Address: 7Ch
Default: FFh
Description: override MSB of LSD4 from GUI

Bit(s)	Name	Description	Default	Type
7:0	DAC_LSD4_ORD<11:4>		11111111b	R/W

Page: 00h
Address: 7Dh
Default: F0h
Description: override LSB of LSD4 from GUI

Bit(s)	Name	Description	Default	Type
7:4	DAC_LSD4_ORD<3:0>		1111b	R/W
3:0	*RSVD*		0000b	R/W

Page: 00h
Address: 7Eh
Default: 57h
Description: reserved

Bit(s)	Name	Description	Default	Type
7:4	Pre_driver_current<3:0>	from 4.0mA to 11.5mA, 0.5mA/ step:6.5mA Is the default setting,the current is source type from supply	0101b	R/W
3	Tswoff_infinity	Extend the Tswoff timer to infinity, shutdown opam in 4x LSD won't shutdown HSD sequencly	0b	R/W
2:0	HSD_driver_current<2:0>	HSD output current setting, from 3mA to 10mA 1mA per step	111b	R/W

Page: 00h
Address: 7Fh
Default: 00h
Description: I2C can wrtie to Define the GPIO status

Bit(s)	Name	Description	Default	Type
7:4	*RSVD*	*Reserved*	0000b	R/W
3:0	gpio_status<3:0>	<3>=GPIO3, <2>=GPIO2<1>=GPIO1,<0>=GPIO0	0000b	R/W

Page: 00h
Address: 80h
Default: D3h
Description: delay in startup and timing diagram

Bit(s)	Name	Description	Default	Type
7:6	ton<1:0>	00=Tswon x1, 01=Tswon x 256; 10= Tswon x 512, 11= Tswon x 1024 (extend the clock cycle number)	11b	R/W
5:4	tswon<1:0>	00=32 Clock cycle,01=64,10=128,11=256, clock cyle=1/12Mhz	01b	R/W
3:2	tswoff<1:0>	00=32 Clock cycle,01=64,10=128,11=256, clock cyle=1/12Mhz	00b	R/W
1:0	toff<1:0>	00=Tswoff x1, 01=Tswoff x 256; 10= Tswoff x 512, 11= Tswoff x 1024 (extend the clock cycle number)	11b	R/W

Page: 00h
Address: 93h
Default: A0h
Description: Alarm ctrl bits 0

Bit(s)	Name	Description	Default	Type
7:6	UV_alarm_Vth	00b: 00:3.8V (Set undervoltage voltage monitor threshold on main input power) 01b: 01:4.0V 10b: 10:4.2V 11b: 11:4.4V	10b	R/W
5:4	OT_Shutdown_threshold	00b: Define the over temperature shutdown threshold 00 130C 01b: 01 140C 10b: 10 150C 11b: 11 Turn off thermal shutdown for HTOL	10b	R/W
3:2	vneg_rdy_vth	00b: vth=-3.9V 01b: vth=-4.4V 10b: vth=-4.9V 11b: vth=-5.4V	00b	R/W
1:0	*RSVD*		00b	R/W

Page: 00h
Address: 94h
Default: F8h
Description: Write the limit theshold of IIN1 reading from ADC, if the MSB of ADC reading is high than this value, issue a alarm bit

Bit(s)	Name	Description	Default	Type
7:0	IIN1_THRESHOLD<7:0>		11111000b	R/W

Page: 00h
Address: 95h
Default: F8h
Description: Write the limit theshold of IIN2 reading from ADC, if the MSB of ADC reading is high than this value, issue a alarm bit

Bit(s)	Name	Description	Default	Type
7:0	IIN2_THRESHOLD<7:0>		11111000b	R/W

Page: 00h
Address: 96h
Default: F8h
Description: TEMP1 pin overtemperature alarm threshold, report over temperature alarm if the internal temperature reading above this value.

Bit(s)	Name	Description	Default	Type
7:0	TEMP1_OT_THD<7:0>		11111000b	R/W

Page: 00h
Address: 97h
Default: F0h
Description: TEMP1 overtemperature alarm reset threshold, if the internal temperature reading go less than this value.

Bit(s)	Name	Description	Default	Type
7:0	TEMP1_OT_R_THD<7:0>		11110000b	R/W

Page: 00h
Address: 98h
Default: F8h
Description: TEMP2 overtemperature alarm threshold, report over temperature alarm if the internal temperature reading above this value.

Bit(s)	Name	Description	Default	Type
7:0	TEMP2_OT_THD<7:0>		11111000b	R/W

Page: 00h
Address: 99h
Default: F0h
Description: TEMP2 overtemperature alarm reset threshold, if the internal temperature reading go less than this value.

Bit(s)	Name	Description	Default	Type
7:0	TEMP2_OT_R_THD<7:0>		11110000b	R/W

Page: 00h
Address: 9Ah
Default: F8h
Description: TEMP3 overtemperature alarm threshold, report over temperature alarm if the internal temperature reading above this value.

Bit(s)	Name	Description	Default	Type
7:0	TEMP3_OT_THD<7:0>		11111000b	R/W

Page: 00h
Address: 9Bh
Default: F0h
Description: TEMP3 overtemperature alarm reset threshold, if the internal temperature reading go less than this value.

Bit(s)	Name	Description	Default	Type
7:0	TEMP3_OT_R_THD<7:0>		11110000b	R/W

Page: 00h
Address: 9Ch
Default: F8h
Description: TEMP4 overtemperature alarm threshold, report over temperature alarm if the internal temperature reading above this value.

Bit(s)	Name	Description	Default	Type
7:0	TEMP4_OT_THD<7:0>		11111000b	R/W

Page: 00h
Address: 9Dh
Default: F0h
Description: TEMP4 overtemperature alarm reset threshold, if the internal temperature reading go less than this value.

Bit(s)	Name	Description	Default	Type
7:0	TEMP4_OT_R_THD<7:0>		11110000b	R/W

Page: 00h
Address: 9Eh
Default: F8h
Description: Tempersture sensor by BG overtemperature alarm threshold, report over temperature alarm if the internal temperature reading above this value.

Bit(s)	Name	Description	Default	Type
7:0	TS_VBG_OT_S_THD<7:0>		11111000b	R/W

Page: 00h
Address: 9Fh
Default: F0h
Description: Tempersture sensor by BG overtemperature alarm reset threshold, if the internal temperature reading go less than this value.

Bit(s)	Name	Description	Default	Type
7:0	TS_VBG_OT_R_THD<7:0>		11110000b	R/W

Page: 00h
Address: A0h
Default: F8h
Description: Tempersture sensor by TS_PTAT overtemperature alarm threshold, report over temperature alarm if the internal temperature reading above this value.

Bit(s)	Name	Description	Default	Type
7:0	TS_PTAT_OT_S_THD<7:0>		11111000b	R/W

Page: 00h
Address: A1h
Default: F0h
Description: Tempersture sensor by TS_PTAT overtemperature alarm reset threshold, if the internal temperature reading go less than this value.

Bit(s)	Name	Description	Default	Type
7:0	TS_PTAT_OT_R_THD<7:0>		11110000b	R/W

Page: 00h
Address: A2h
Default: 81h
Description: Fail pin Ctrl, in scan and bist mode, always cmos output only

Bit(s)	Name	Description	Default	Type
7	alarm_clear	Write it to clear all alamr register from temp_alarm.alarm0,alarm1	1b	R/W
6	ts_autocalib	Write it to run a temperature sensor auto calib function	0b	R/W
5	Fail_out_cmos	Change the Fail output pin to CMOS output	0b	R/W
4	Fail_flip_polar	Filp the Fail polarity from low active to high active	0b	R/W
3:1	Fail_interrupt_duration	Duration of Fail pull low at interrupt mode: 000=12,001=24…….111=96 Clock cycles	000b	R/W
0	FAIL_PIN_MODE	Controls the behavior of the FAIL pin between 1:Trigger_lock Mode and 0: Interrupt_mode	1b	R/W

Page: 00h
Address: A3h
Default: 00h
Description: Alarm mask 0 for register Alarm0

Bit(s)	Name	Description	Default	Type
7:0	Alarmmask0<7:0>	Write it to maks the alarm status in register Alarm0	00000000b	R/W

Page: 00h
Address: A4h
Default: 00h
Description: Alarm mask 1 for register Alarm_LUT_VOLT

Bit(s)	Name	Description	Default	Type
7:0	Alarmmask1<7:0>	Write it to maks the alarm status in register Alarm_LUT_VOLT	00000000b	R/W

Page: 00h
Address: A5h
Default: 23h
Description: Alarm mask 2 for TEMP_ALARM

Bit(s)	Name	Description	Default	Type
7:0	Alarmmask2<7:0>	Write it to maks the alarm status in register TEMP_ALARM; mask<1:0> Due to RFP application ,there may be no thermistor on the pins	00100011b	R/W

Page: 00h
Address: A6h
Default: 03h
Description: Alarm mask 3 for Alarm_LUT_TEMP

Bit(s)	Name	Description	Default	Type
7:0	Alarmmask3<7:0>	Write it to maks the alarm status in register Alarm_LUT_TEMP	00000011b	R/W

Page: 00h
Address: A7h
Default: 00h
Description: rsvd

Bit(s)	Name	Description	Default	Type
7:0	RSVD0<7:0>	*rsvd*	00000000b	R/W

Page: 00h
Address: AAh
Default: FFh
Description: Set the up limit of the DAC code of LSD1, MSB

Bit(s)	Name	Description	Default	Type
7:0	UPLIMIT_LSD1<11:4>		11111111b	R/W

Page: 00h
Address: ABh
Default: FFh
Description: Set the up limit of the DAC code of LSD2, MSB

Bit(s)	Name	Description	Default	Type
7:0	UPLIMIT_LSD2<11:4>		11111111b	R/W

Page: 00h
Address: ACh
Default: FFh
Description: Set the up limit of the DAC code of LSD1 and LSD2, LSB

Bit(s)	Name	Description	Default	Type
7:4	UPLIMIT_LSD1<3:0>		1111b	R/W
3:0	UPLIMIT_LSD2<3:0>		1111b	R/W

Page: 00h
Address: ADh
Default: FFh
Description: Set the up limit of the DAC code of LSD3, MSB

Bit(s)	Name	Description	Default	Type
7:0	UPLIMIT_LSD3<11:4>		11111111b	R/W

Page: 00h
Address: AEh
Default: FFh
Description: Set the up limit of the DAC code of LSD4, MSB

Bit(s)	Name	Description	Default	Type
7:0	UPLIMIT_LSD4<11:4>		11111111b	R/W

Page: 00h
Address: AFh
Default: FFh
Description: Set the up limit of the DAC code of LSD3 and LSD4, LSB

Bit(s)	Name	Description	Default	Type
7:4	UPLIMIT_LSD3<3:0>		1111b	R/W
3:0	UPLIMIT_LSD4<3:0>		1111b	R/W

Page: 00h
Address: B0h
Default: 00h
Description: Set the bottom limit of the DAC code of LSD1, MSB

Bit(s)	Name	Description	Default	Type
7:0	BTLIMIT_LSD1<11:4>		00000000b	R/W

Page: 00h
Address: B1h
Default: 00h
Description: Set the bottom limit of the DAC code of LSD2, MSB

Bit(s)	Name	Description	Default	Type
7:0	BTLIMIT_LSD2<11:4>		00000000b	R/W

Page: 00h
Address: B2h
Default: 00h
Description: Set the bottom limit of the DAC code of LSD1 and LSD2, LSB

Bit(s)	Name	Description	Default	Type
7:4	BTLIMIT_LSD1<3:0>		0000b	R/W
3:0	BTLIMIT_LSD2<3:0>		0000b	R/W

Page: 00h
Address: B3h
Default: 00h
Description: Set the bottom limit of the DAC code of LSD3, MSB

Bit(s)	Name	Description	Default	Type
7:0	BTLIMIT_LSD3<11:4>		00000000b	R/W

Page: 00h
Address: B4h
Default: 00h
Description: Set the bottom limit of the DAC code of LSD4, MSB

Bit(s)	Name	Description	Default	Type
7:0	BTLIMIT_LSD4<11:4>		00000000b	R/W

Page: 00h
Address: B5h
Default: 00h
Description: Set the bottom limit of the DAC code of LSD3 and LSD4, LSB

Bit(s)	Name	Description	Default	Type
7:4	BTLIMIT_LSD3<3:0>		0000b	R/W
3:0	BTLIMIT_LSD4<3:0>		0000b	R/W

Page: 00h
Address: B6h
Default: 08h
Description: control bit of the LUT voltage

Bit(s)	Name	Description	Default	Type
7:5	*RSVD*		000b	R/W
4	*RSVD*		0b	R/W
3:0	LUTVOLT_TEMP_SEL<3:0>	LUT_VOLT_CTRL<3:0>: 0000: TS_VPTAT -> LSD1/2/3/4 0001: ts_vbg -> LSD1/2/¾ 0010: TS1 -> LSD1/2/3/4 0011:TS2 -> LSD1/2/3/4 0100:TS3 -> LSD1/2/3/4; 0101:TS3>LSD2 And LSD4; TS1->LSD1 and LSD3 0110:TS4 -> LSD1/2/3/4 0111:TS1 -> LSD1 and LSD3, TS2-> LSD2 and LSD4 1000: TS3 -> LSD1 and LSD3, TS4 -> LSD2 and LSD4 (default) 1001: TS1->LSD1 and LSD3, TS2=LSD2, TS4=LSD4 1010:TS3->LSD1 And LSD3, TS2=LSD2, TS4=LSD4 1011:TS2->LSD2 And LSD4, TS1=LSD1, TS3=LSD3 1100:TS4->LSD2 And LSD4, TS1=LSD1, TS3=LSD3 1101: TS1->LSD1;TS2->LSD2;TS3->LSD3;TS3->LSD4 1110:internal TSPTAT>LSD2 and LSD4; TS1->LSD1 and LSD3 1111:TS_OFFCHIP -> LSD1/2/3/4	1000b	R/W

Page: 00h
Address: B7h
Default: 80h
Description: I2C control, skipped in scan mode(need to confirmed by digital designer)

Bit(s)	Name	Description	Default	Type
7	*RSVD*	*Reserved*	1b	R/W
6:0	i2c_add_reg	Store the I2C address	0000000b	R/W

Page: 00h
Address: B8h
Default: 55h
Description: I2C control, skipped in scan mode(need to confirmed by digital designer)

Bit(s)	Name	Description	Default	Type
7	*RSVD*	*rsvd*	0b	R/W
6:0	i2c_allcall_adr<6:0>	Store the I2C broadcasting address	1010101b	R/W

Page: 00h
Address: E0h
Default: 00h
Description: Write the NVM burn counter result,automatic increase 1 when NVM burned

Bit(s)	Name	Description	Default	Type
7:0	NVM_BURN_COUNT<7:0>	Store the NVM burns counter result	00000000b	R

Page: 00h
Address: E1h
Default: 00h
Description: Write the NVM burn counter result,automatic increase 1 when NVM burned,reseve following E2-FF register for NVM burn function. Keep them idle.

Bit(s)	Name	Description	Default	Type
7:0	NVM_BURN_COUNT<15:8>	Store the NVM burns counter result	00000000b	R

Page: 00h
Address: FAh
Register Name: PASSWORD0
Default Value: 00'h
Description: password for level 0 control; write only to the end of this page

Bit(s)	Name	Description	Default	Type
[7:0]	PASSWORD0<7:0>	0000 0000b: Password does not match 0000 0001b: Password matches	0000 0000b	R

Page: 00h
Address: FBh
Register Name: PASSWORD1
Default Value: 00'h
Description: password for level 1 control

Bit(s)	Name	Description	Default	Type
[7:0]	PASSWORD1<7:0>	0000 0000b: Password does not match 0000 0001b: Password matches	0000 0000b	R

Page: 00h
Address: FCh
Register Name: PASSWORD2
Default Value: 00'h
Description: password for level 2 control

Bit(s)	Name	Description	Default	Type
[7:0]	PASSWORD2<7:0>	0000 0000b: Password does not match 0000 0001b: Password matches	0000 0000b	R

Page: 00h
Address: FDh
Register Name: PASSWORD3
Default Value: 00'h
Description: password for level 3 control

Bit(s)	Name	Description	Default	Type
[7:0]	PASSWORD3<7:0>	0000 0000b: Password does not match 0000 0001b: Password matches	0000 0000b	R

Page: GLOBAL
Address: FEh
Register Name: PAGE
Default Value: 00'h
Description: Register page

Bit(s)	Name	Description	Default	Type
[7:0]	Page<7:0>	Register page.	0000 0000b	R/W

Page: 02h
Address: 00h
Register Name: CHIPID
Default Value: 50'h
Description: Chip ID register.

Bit(s)	Name	Description	Default	Type
[7:0]	CHIPID	MABC11050 Chip ID	0101 0000b	R

Page: 02h
Address: 01h
Register Name: REVID
Default Value: 01'h
Description: Revision ID register.

Bit(s)	Name	Description	Default	Type
[7:0]	REVID	MABC11050 revision	0000 0001b	R

Page: 02h
Address: 02h
Register Name: SOFT_RESET
Default Value: 00'h
Description: Software reset register. Not download from NVM, need to program from Host.

Bit(s)	Name	Description	Default	Type
[7:0]	SOFT_RESET	0000 0000b: Normal operation. 1010 1010b: Self Clearing Reset (16 clock cycles at 12MHz) 0101 01010b: Reset everything without an OTP download	0000 0000b	R/W
NOTES: 1. Writing AAh causes a 16 12MHz clock cycles reset (self clearing) 2. Writing 55h reset everything without download OTP (double check with RF design).				

Page: 02h
Address: 09h
Register Name: I2C_ANA
Default Value: 41'h
Description: RSVD

Bit(s)	Name	Description	Default	Type
[7]	I2C_allcall_dis	0: Part will respond to the broadcast address [Note 1] 1: Part will not respond to the broadcasting address.	0b	R/W
[6:0]	I2c_ana<6:0>	The address from the i2c_add_sel	100 0001b	R
NOTES: 1. Broadcast address is found in Page: 00h, Address: B8h				

Page: 02h
Address: 0Fh
Register Name: CHNL0_MSB
Default Value: 00'h
Description: MSB readback of input channel 0

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_I_LSD_ADJUST<11:4>	Reserved		R

Page: 02h
Address: 10h
Register Name: CHNL0_LSB
Default Value: 0x'h
Description: LSB readback of input channel 0

Bit(s)	Name	Description	Default	Type
[7:4]	*RSVD*	*Reserved (set to default)*	0000b	R
[3:0]	Access_ctrl<3:0>	Bit<0/1/2/3>.=1 means password0/1/2/3 is right	0000b	R

Page: 02h
Address: 11h
Register Name: CHNL1_MSB
Default Value: 00'h
Description: MSB readback of input channel 1

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_LSD1_OUTP<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 12h
Register Name: CHNL1_LSB
Default Value: 00'h
Description: LSB readback of input channel 1

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_LSD1_OUTP<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 13h
Register Name: CHNL2_MSB
Default Value: 00'h
Description: MSB readback of input channel 2

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_LSD2_OUTP<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 14h
Register Name: CHNL2_LSB
Default Value: 00'h
Description: LSB readback of input channel 2

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_LSD2_OUTP<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 15h
Register Name: CHNL3_MSB
Default Value: 00'h
Description: MSB readback of input channel 3

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_LSD3_OUTP<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 16h
Register Name: CHNL3_LSB
Default Value: 00'h
Description: LSB readback of input channel 3

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_LSD3_OUTP<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 17h
Register Name: CHNL4_MSB
Default Value: 00'h
Description: MSB readback of input channel 4

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_LSD4_OUTP<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 18h
Register Name: CHNL4_LSB
Default Value: 00'h
Description: LSB readback of input channel 4

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_LSD4_OUTP<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 19h
Register Name: CHNL5_MSB
Default Value: 00'h
Description: MSB readback of input channel 5

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_LSD1_OUTN<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 1Ah
Register Name: CHNL5_LSB
Default Value: 00'h
Description: LSB readback of input channel 5

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_LSD1_OUTN<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 1Bh
Register Name: CHNL6_MSB
Default Value: 00'h
Description: MSB readback of input channel 6

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_LSD2_OUTN<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 1Ch
Register Name: CHNL6_LSB
Default Value: 00'h
Description: LSB readback of input channel 6

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_LSD2_OUTN<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 1Dh
Register Name: CHNL7_MSB
Default Value: 00'h
Description: MSB readback of input channel 7

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_LSD3_OUTN<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 1Eh
Register Name: CHNL7_LSB
Default Value: 00'h
Description: LSB readback of input channel 7

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_LSD3_OUTN<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 1Fh
Register Name: CHNL8_MSB
Default Value: 00'h
Description: MSB readback of input channel 8

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_LSD4_OUTN<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 20h
Register Name: CHNL8_LSB
Default Value: 00'h
Description: LSB readback of input channel 8

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_LSD4_OUTN<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 27h
Register Name: CHNL12_MSB
Default Value: 00'h
Description: MSB readback of input channel 12

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_IIN1<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 28h
Register Name: CHNL12_LSB
Default Value: 00'h
Description: LSB readback of input channel 12

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_IIN1<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 29h
Register Name: CHNL13_MSB
Default Value: 00'h
Description: MSB readback of input channel 13

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_IIN2<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 2Ah
Register Name: CHNL13_LSB
Default Value: 00'h
Description: LSB readback of input channel 13

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_IIN2<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 2Fh
Register Name: CHNL16_MSB
Default Value: 00'h
Description: MSB readback of input channel 16

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_LSD4_TEMP<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 30h
Register Name: CHNL16_LSB
Default Value: 00'h
Description: LSB readback of input channel 16

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_LSD4_TEMP<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 31h
Register Name: CHNL17_MSB
Default Value: 00'h
Description: MSB readback of input channel 17

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_LSD3_TEMP<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 32h
Register Name: CHNL17_LSB
Default Value: 00'h
Description: LSB readback of input channel 17

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_LSD3_TEMP<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 33h
Register Name: CHNL18_MSB
Default Value: 00'h
Description: MSB readback of input channel 18

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_LSD2_TEMP<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 34h
Register Name: CHNL18_LSB
Default Value: 00'h
Description: LSB readback of input channel 18

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_LSD2_TEMP<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 35h
Register Name: CHNL19_MSB
Default Value: 00'h
Description: MSB readback of input channel 19

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_LSD1_TEMP<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 36h
Register Name: CHNL19_LSB
Default Value: 00'h
Description: LSB readback of input channel 19

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_LSD1_TEMP<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 39h
Register Name: CHNL21_MSB
Default Value: 00'h
Description: MSB readback of input channel 21

Bit(s)	Name	Description	Default	Type
[7:0]	ADC_EXT_VNEG<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 3Ah
Register Name: CHNL21_LSB
Default Value: 00'h
Description: LSB readback of input channel 21

Bit(s)	Name	Description	Default	Type
[7:4]	ADC_EXT_VNEG<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 3Fh
Register Name: TEMP_ALARM
Default Value: 00'h
Description: Latched alarm: Temperature sensor status,

Bit(s)	Name	Description	Default	Type
[7]	iin1_cl_lt	Current input 1: Current limit indicator 1b: Current limit reached or exceeded 0b: Normal operation	0b	R
[6]	iin2_cl_lt	Current input 2: Current limit indicator 1b: Current limit reached or exceeded 0b: Normal operation	0b	R
[5]	RSVD	Reserved	0b	R
[4]	TS_PTAT_Alarm	Latched temperature alarm for TS_PTAT 1b: PTAT temperature sensor threshold reached or exceeded 0b: Normal operation	0b	R
[3]	LSD4_TS_Alarm	Latched temperature alarm for LSD4 1b: LSD4 temperature sensor threshold reached or exceeded 0b: Normal operation	0b	R
[2]	LSD3_TS_Alarm	Latched temperature alarm for LSD3 1b: LSD3 temperature sensor threshold reached or exceeded 0b: Normal operation	0b	R
[1]	LSD2_TS_Alarm	Latched temperature alarm for LSD2 1b: LSD2 temperature sensor threshold reached or exceeded 0b: Normal operation	0b	R
[0]	LSD1_TS_Alarm	Latched temperature alarm for LSD1 1b: LSD1 temperature sensor threshold reached or exceeded 0b: Normal operation	0b	R

Page: 02h
Address: 40h
Register Name: ALARM0
Default Value: 00'h
Description: Real-time alarm: Device voltage and current status

Bit(s)	Name	Description	Default	Type
[7]	neg_uv_rt	Negative voltage supply under-voltage alarm 1b: Negative voltage supply is not ready 0b: Normal operation	0b	R
[6]	lsd1_cl_rt	LSD1 output current limit alarm 1b: LSD1 output current limit reached or exceeded 0b: Normal operation	0b	R
[5]	lsd2_cl_rt	LSD2 output current limit alarm 1b: LSD2 output current limit reached or exceeded 0b: Normal operation	0b	R
[4]	lsd3_cl_rt	LSD3 output current limit alarm 1b: LSD3 output current limit reached or exceeded 0b: Normal operation	0b	R
[3]	lsd4_cl_rt	LSD4 output current limit alarm 1b: LSD4 output current limit reached or exceeded 0b: Normal operation	0b	R
[2]	v1p8d_uv_rt	Digital 1.8V under-voltage alarm 1b: 1.8V digital supply is too low 0b: Normal operation	0b	R
[1]	v1p8a_uv_rt	Analog 1.8V under-voltage alarm 1b: 1.8V analog supply is too low 0b: Normal operation	0b	R
[0]	undervoltage_alarm_rt	Analog 5V under-voltage alarm 1b: 5V analog supply is too low 0b: Normal operation	0b	R

Page: 02h
Address: 41h
Register Name: ALARM1
Default Value: 00'h
Description: Latched alarm: Device voltage and current status

Bit(s)	Name	Description	Default	Type
[7]	neg_uv_lt	Negative voltage supply under-voltage alarm 1b: Negative voltage supply is not ready 0b: Normal operation	0b	R
[6]	lsd1_cl_lt	LSD1 output current limit alarm 1b: LSD1 output current limit reached or exceeded 0b: Normal operation	0b	R
[5]	lsd2_cl_lt	LSD2 output current limit alarm 1b: LSD2 output current limit reached or exceeded 0b: Normal operation	0b	R
[4]	lsd3_cl_lt	LSD3 output current limit alarm 1b: LSD3 output current limit reached or exceeded 0b: Normal operation	0b	R
[3]	lsd4_cl_lt	LSD4 output current limit alarm 1b: LSD4 output current limit reached or exceeded 0b: Normal operation	0b	R
[2]	v1p8d_uv_lt	Digital 1.8V under-voltage alarm 1b: 1.8V digital supply is too low 0b: Normal operation	0b	R
[1]	v1p8a_uv_lt	Analog 1.8V under-voltage alarm 1b: 1.8V analog supply is too low 0b: Normal operation	0b	R
[0]	undervoltage_alarm_lt	Analog 5V under-voltage alarm 1b: 5V analog supply is too low 0b: Normal operation	0b	R

Page: 02h
Address: 42h
Register Name: ALARM_LUT_TEMP
Default Value: 00'h
Description: realtime(unlatched) version of ALAMR0

Bit(s)	Name	Description	Default	Type
[7]	lsd4_lut_temp_p	0b: Normal operation 1b: ALU did not finish at the address 255 for LSD_TEMP4	0b	R
[6]	lsd4_lut_temp_n	0b: Normal operation 1b: ALU did not finish at the address 0 for LSD_TEMP4	0b	R
[5]	lsd3_lut_temp_p	0b: Normal operation 1b: ALU did not finish at the address 255 for LSD_TEMP3	0b	R
[4]	lsd3_lut_temp_n	0b: Normal operation 1b: ALU did not finish at the address 0 for LSD_TEMP3	0b	R
[3]	lsd2_lut_temp_p	0b: Normal operation 1b: ALU did not finish at the address 255 for LSD_TEMP2	0b	R
[2]	lsd2_lut_temp_n	0b: Normal operation 1b: ALU did not finish at the address 0 for LSD_TEMP2	0b	R
[1]	lsd1_lut_temp_p	0b: Normal operation 1b: ALU did not finish at the address 255 for LSD_TEMP1	0b	R
[0]	lsd1_lut_temp_n	0b: Normal operation 1b: ALU did not finish at the address 0 for LSD_TEMP1	0b	R

Page: 02h
Address: 43h
Register Name: ALARM_LUT_VOLT
Default Value: 00'h
Description: latched version of ALARM0

Bit(s)	Name	Description	Default	Type
[7]	lsd4_lut_volt_p	0b: Normal operation 1b: ALU didn't finish at the address 63 for LSD4_DEL	0b	R
[6]	lsd4_lut_volt_n	0b: Normal operation 1b: ALU didn't finish at the address 0 for LSD4_DEL	0b	R
[5]	lsd3_lut_volt_p	0b: Normal operation 1b: ALU didn't finish at the address 63 for LSD3_DEL	0b	R
[4]	lsd3_lut_volt_n	0b: Normal operation 1b: ALU didn't finish at the address 0 for LSD3_DEL	0b	R
[3]	lsd2_lut_volt_p	0b: Normal operation 1b: ALU didn't finish at the address 63 for LSD2_DEL	0b	R
[2]	lsd2_lut_volt_n	0b: Normal operation 1b: ALU didn't finish at the address 0 for LSD2_DEL	0b	R
[1]	lsd1_lut_volt_p	0b: Normal operation 1b: ALU didn't finish at the address 63 for LSD1_DEL	0b	R
[0]	lsd1_lut_volt_n	0b: Normal operation 1b: ALU didn't finish at the address 0 for LSD1_DEL	0b	R

Page: 02h
Address: 46h
Register Name: OFFCHIP_TEMP_MSB
Default Value: 00'h
Description: Store the calculated off-chip temperature MSB. The expected temperature range of the temperature sensor is -45° to -125°C (RSVD)

Bit(s)	Name	Description	Default	Type
[7:0]	offchip_temp<11:4>	User defined	0000 0000b	R/W

Page: 02h
Address: 47h
Register Name: OFFCHIP_TEMP_LSB
Default Value: 00'h
Description: Store the calculated off-chip temperature LSB. The expected temperature range of the temperature sensor is -45° to -125°C (RSVD)

Bit(s)	Name	Description	Default	Type
[7:4]	offchip_temp<3:0>	User defined	0000b	R/W
[3:0]	*RSVD*	*Reserved (set to default)*	0000b	R

Page: 02h
Address: 48h
Register Name: CAL_TS1_MSB
Default Value: 00'h
Description: Store the calculated temperature MSB for the temperature sensor on LSD1

Bit(s)	Name	Description	Default	Type
[7:0]	CAL_TS1<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 49h
Register Name: CAL_TS1_LSB
Default Value: 00'h
Description: Store the calculated temperature LSB for the temperature sensor on LSD1

Bit(s)	Name	Description	Default	Type
[7:4]	CAL_TS1<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved*	0000b	R

Page: 02h
Address: 4Ah
Register Name: CAL_TS2_MSB
Default Value: 00'h
Description: Store the calculated temperature MSB for the temperature sensor on LSD2

Bit(s)	Name	Description	Default	Type
[7:0]	CAL_TS2<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 4Bh
Register Name: CAL_TS2_LSB
Default Value: 00'h
Description: Store the calculated temperature LSB for the temperature sensor on LSD2

Bit(s)	Name	Description	Default	Type
[7:4]	CAL_TS2<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved*	0000b	R

Page: 02h
Address: 4Ch
Register Name: CAL_TS3_MSB
Default Value: 00'h
Description: Store the calculated temperature MSB for the temperature sensor on LSD3

Bit(s)	Name	Description	Default	Type
[7:0]	CAL_TS3<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 4Dh
Register Name: CAL_TS3_LSB
Default Value: 00'h
Description: Store the calculated temperature LSB for the temperature sensor on LSD3

Bit(s)	Name	Description	Default	Type
[7:4]	CAL_TS3<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved*	0000b	R

Page: 02h
Address: 4Eh
Register Name: CAL_TS4_MSB
Default Value: 00'h
Description: Store the calculated temperature MSB for the temperature sensor on LSD4

Bit(s)	Name	Description	Default	Type
[7:0]	CAL_TS4<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 4Fh
Register Name: CAL_TS4_LSB
Default Value: 00'h
Description: Store the calculated temperature LSB for the temperature sensor on LSD4

Bit(s)	Name	Description	Default	Type
[7:4]	CAL_TS4<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved*	0000b	R

Page: 02h
Address: 50h
Register Name: RSVD
Default Value: 00'h
Description: Reserved

Bit(s)	Name	Description	Default	Type
[7:0]	RSVD	Reserved	0000 0000b	R

Page: 02h
Address: 51h
Register Name: RSVD
Default Value: 00'h
Description: StReserved

Bit(s)	Name	Description	Default	Type
[7:4]	RSVD	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved*	0000b	R

Page: 02h
Address: 52h
Register Name: CAL_INT_PTAT_MSB
Default Value: 00'h
Description: Store the calculated temperature MSB for the internal PTAT temperature sensor.

Bit(s)	Name	Description	Default	Type
[7:0]	CAL_INT_TS_PTAT<11:4>	Reserved	0000 0000b	R

Page: 02h
Address: 53h
Register Name: CAL_INT_PTAT_LSB
Default Value: 00'h
Description: Store the calculated temperature LSB for the internal PTAT temperature sensor.

Bit(s)	Name	Description	Default	Type
[7:4]	CAL_INT_TS_PTAT<3:0>	Reserved	0000b	R
[3:0]	*RSVD*	*Reserved*	0000b	R

Page: 01h
Address: 62h
Register Name: POWER_MSB
Default Value: 00'h
Description: Pre-programmed non-volatile memory location for power level MSB.

Bit(s)	Name	Description	Default	Type
[7:0]	POWER_MSB	Power level MSB	0000 0000b	R/W

Page: 01h
Address: 6Ch
Register Name: VENDOR_CODE
Default Value: 00'h
Description: Pre-programmed non-volatile memory location for interface identification coding

Bit(s)	Name	Description	Default	Type
[7:0]	VENDOR_CODE	Identical to interface identification coding	0000 0000b	R/W

Page: 01h
Address: 6Dh
Register Name: UNI_MOD_TYP_NO1
Default Value: 00'h
Description: Pre-programmed non-volatile memory location for unique software identification

Bit(s)	Name	Description	Default	Type
[7:0]	UNI_MOD_TYP_NO1	Unique software identification	0000 0000b	R/W

Page: 01h
Address: 6Eh
Register Name: UNI_MOD_TYP_NO2
Default Value: 00'h
Description: Pre-programmed non-volatile memory location for unique software identification

Bit(s)	Name	Description	Default	Type
[7:0]	UNI_MOD_TYP_NO2	Unique software identification	0000 0000b	R/W

Page: 01h
Address: 6Fh
Register Name: POWER_LSB
Default Value: 00'h
Description: Pre-programmed non-volatile memory location for power level LSB (Binary value * 0.1W)

Bit(s)	Name	Description	Default	Type
[7:0]	POWER_LSB	Power level LSB (Binary value * 0.1W)	0000 0000b	R/W

Page: 01h
Address: 70h
Register Name: DL_FREQ_LOW1
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	DL_FREQ_LOW1	Binary in MHz, lower address LSB	0000 0000b	R/W

Page: 01h
Address: 71h
Register Name: DL_FREQ_LOW2
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	DL_FREQ_LOW2	Binary in MHz, upper address MSB	0000 0000b	R/W

Page: 01h
Address: 72h
Register Name: DL_FREQ_HIGH1
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	DL_FREQ_HIGH1	Binary in MHz, lower address LSB	0000 0000b	R/W

Page: 01h
Address: 73h
Register Name: DL_FREQ_HIGH2
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	DL_FREQ_HIGH2	Binary in MHz, upper address MSB	0000 0000b	R/W

Page: 01h
Address: 74h
Register Name: CODE_YEAR
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	CODE_YEAR	Binary year -2000	0000 0000b	R/W

Page: 01h
Address: 75h
Register Name: CODE_WEEK
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	CODE_WEEK	Binary week	0000 0000b	R/W

Page: 01h
Address: 76h
Register Name: MODULE_NAME1
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	MODULE_NAME1	ASCII module name and / or serial number	0000 0000b	R/W

Page: 01h
Address: 77h
Register Name: MODULE_NAME2
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	MODULE_NAME2	ASCII module name and / or serial number	0000 0000b	R/W

Page: 01h
Address: 78h
Register Name: MODULE_NAME3
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	MODULE_NAME3	ASCII module name and / or serial number	0000 0000b	R/W

Page: 01h
Address: 79h
Register Name: MODULE_NAME4
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	MODULE_NAME4	ASCII module name and / or serial number	0000 0000b	R/W

Page: 01h
Address: 7Ah
Register Name: MODULE_NAME5
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	MODULE_NAME5	ASCII module name and / or serial number	0000 0000b	R/W

Page: 01h
Address: 7Bh
Register Name: MODULE_NAME6
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	MODULE_NAME6	ASCII module name and / or serial number	0000 0000b	R/W

Page: 01h
Address: 7Ch
Register Name: MODULE_NAME7
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	MODULE_NAME7	ASCII module name and / or serial number	0000 0000b	R/W

Page: 01h
Address: 7Dh
Register Name: MODULE_NAME8
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	MODULE_NAME8	ASCII module name and / or serial number	0000 0000b	R/W

Page: 01h
Address: 7Eh
Register Name: MODULE_NAME9
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	MODULE_NAME9	ASCII module name and / or serial number	0000 0000b	R/W

Page: 01h
Address: 7Fh
Register Name: MODULE_NAME10
Default Value: 00'h
Description: Pre-programmed non-volatile memory

Bit(s)	Name	Description	Default	Type
[7:0]	MODULE_NAME10	ASCII module name and / or serial number	0000 0000b	R/W

Page: 80h
Address: 00h to 7Fh
Register Name: LUT_TEMP[0:127]
Default Value: 00'h
Description: LUT from -40C ,per 2.5C

Bit(s)	Address	Name	Description	Default	Type
[7:0]	00h-7Fh	LUT_TEMP[0:127] Bit[7:0]	User Defined Look-Up Table Record	0000 0000b	R/W

Page: 81h
Address: 00h to 7Fh
Register Name: LUT_TEMP[128:255]
Default Value: 00'h
Description: LUT from -40C ,per 2.5C

Bit(s)	Address	Name	Description	Default	Type
[7:0]	00h-7Fh	LUT_TEMP[128:255] Bit[7:0]	User Defined Look-Up Table Record	0000 0000b	R/W

Page: 90h
Address: 00h to 3Fh
Register Name: LSD1_VOLT[0:63]
Default Value: 00'h
Description: LSD Channel 1, Record 0 of look-up-table (LUT) for gate voltage. Intended temperature range from -40°C to +125°C

Bit(s)	Address	Name	Description	Default	Type
[7:0]	00h-3F	LSD1_VOLT[0:63] Bit[7:0]	User Defined Look-Up Table Record	0000 0000b	R/W

Page: 91h
Address: 00h to 3Fh
Register Name: LSD2_VOLT[0:63]
Default Value: 00'h
Description: LUT from -40C ,per 2.5C

Bit(s)	Address	Name	Description	Default	Type
[7:0]	00h-3Fh	LSD2_VOLT[0:63] Bit[7:0]	User Defined Look-Up Table Record	0000 0000b	R/W

Page: 92h
Address: 00h to 3Fh
Register Name: LSD3_VOLT[0:63]
Default Value: 00'h
Description: LUT from -40C ,per 2.5C

Bit(s)	Address	Name	Description	Default	Type
[7:0]	00h-3Fh	LSD3_VOLT[0:63] Bit[7:0]	User Defined Look-Up Table Record	0000 0000b	R/W

Page: 93h
Address: 00h to 3Fh
Register Name: LSD4_VOLT[0:63]
Default Value: 00'h
Description: LUT from -40C ,per 2.5C

Bit(s)	Address	Name	Description	Default	Type
[7:0]	00h-3Fh	LSD4_VOLT[0:63] Bit[7:0]	User Defined Look-Up Table Record	0000 0000b	R/W