High Linearity Distributed Power Amplifier
0.05 - 6 GHz

MAAP-011307
Rev. V2

Features

- P1dB Output Power: 29 dBm
- Gain: 12 dB
- Noise Figure: 5 dB
- Output IP3: 40 dBm
- Reverse Isolation: 30 dB
- 50 Ω Matched Input and Output
- Lead-Free 5 mm 32-Lead PQFN Package
- Halogen-Free "Green" Mold Compound
- RoHS* Compliant

Applications

- Instrumentation
- EW, ECM, MILCOM

Description

The MAAP-011307 is a wideband amplifier that operates from DC to 6 GHz. The device features 12 dB gain, 29 dBm P1dB and excellent noise figure. This power amplifier also features gate bias adjust pins to change current setting to compensate for power or temperature.

This device is ideally suited for applications requiring a broad bandwidth such as laboratory instrumentation.

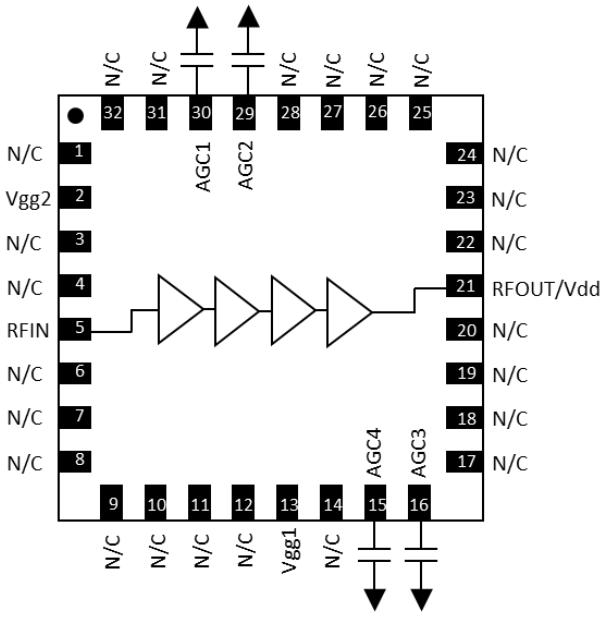
The high reverse isolation also makes this an excellent choice for driver or buffer amplifier applications.

Ordering Information[1]

Part Number	Package
MAAP-011307-TR0500	500 Piece Reel
MAAP-011307-SMB	Sample Board

1. Reference Application Note M513 for reel size information.

Functional Schematic[2]



Pin Configuration[3]

Pin #	Function
1, 3, 4, 6 - 12, 13, 14, 17 - 20, 22 - 28, 31, 32	N/C
2	$V_{GG}2$
5	RF_{IN}
13	$V_{GG}1$
15	AGC4
16	AGC3
21	RF_{OUT} / V_{DD}
29	AGC2
30	AGC1
Paddle[4]	GND

2. See Application Schematic for external capacitor values.
3. MACOM recommends connecting all N/C package pins to ground.
4. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications:
Freq. = 0.05 - 6.0 GHz, T_A = 25°C, V_{DD} = +12 V, $V_{GG}1$ = -0.8 V, $V_{GG}2$ = +5.2 V, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	1 GHz 2 GHz 6 GHz	dB	10.0 10.0 8.0	12.0 12.0 10.5	—
OIP3	P_{IN} = 0 dBm / tone, 10 MHz tone spacing 1 - 6 GHz	dBm	—	40.0	—
P1dB	—	dBm	—	29	—
Noise Figure	0.05 - 0.7 GHz 0.7 - 6 GHz	dB	—	12 5	—
Drain Current[5]	—	mA	—	330	—
Current	$V_{GG}1$ $V_{GG}2$	µA	—	30 100	—

5. Set quiescent drain current by adjusting the gate potentials. See bias sequencing instructions below.

Recommended Operating Limits

Parameter	Maximum
RF Input Power CW	20 dBm
V_{DD}	14 V
$V_{GG}1$	-3 V to -0.5 V
$V_{GG}2$	3 V to 5.5 V
Operating Temperature	-40ºC to +85ºC
Junction Temperature[6,7]	+150ºC

6. Operating at nominal conditions with $T_J \leq 150°C$ will ensure MTTF > 1 x 10^6 hours.
7. Junction Temperature (T_J) = T_C + Θ_{JC} * ((V * I) - (P_{OUT} - P_{IN}))
   Typical thermal resistance (Θ_{JC}) = 14°C/W
   a) For T_C = +25°C,
   T_J = 80.2°C @ 12 V, 300 mA, P_{IN} = 0 dBm, P_{OUT} = 13 dBm
   b) For T_C = +85°C,
   T_J = 133.2°C @ 12 V, 365 mA, P_{IN} = 18 dBm, P_{OUT} = 30 dBm

Absolute Maximum Ratings[9,10]

Parameter	Absolute Maximum
RF Input Power CW	24 dBm
V_{DD}	15 V
$V_{GG}1$	-5 V to -0.4 V
$V_{GG}2$	1 V to 5.6 V
Storage Temperature	-55°C to +150°C

9. Exceeding any one or combination of these limits may cause permanent damage to this device.
10. MACOM does not recommend sustained operation near these survivability limits.

Bias Sequencing

Turn ON:

1. Apply -2.5 V to $V_{GG}1$
2. Apply +5.2 V to $V_{GG}2$
3. Apply +12 V to V_{DD}
4. Adjust $V_{GG}1$ more positive until I_{DQ} = 300 mA[8]
5. Apply RF.

Turn OFF:

1. Turn off is the reverse order.

8. $V_{GG}1$ - $V_{GG}2$ should be approximately equal to 6 V when I_{DQ} = 300 mA.

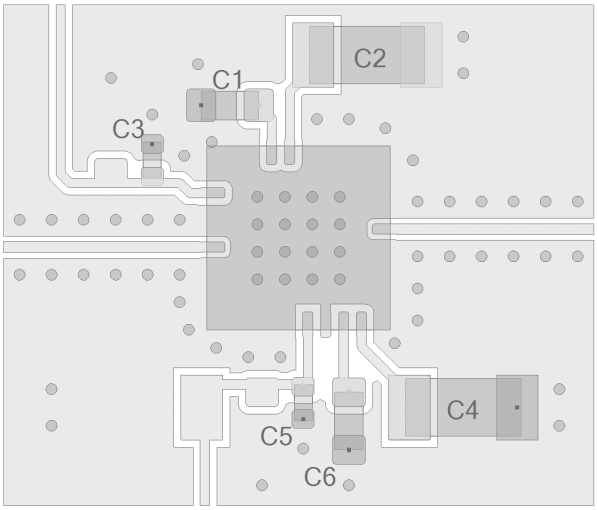
Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Sample Board Layout



Recommended PCB Information

RF input and output are 50 Ω transmission lines on single layer 6.6 mil Rogers RO4350B with 1/2 oz. Copper. Use plated through hole (PTH) filled vias in the ground plane and under device. These filled vias should be capped over and planarized. PCB files for MACOM Sample Board are available on the MAAP-011307 Product Page.

Grounding and Thermal Vias

The total ground (common mode) inductance should not exceed 0.03 nH (30 pH). This is equivalent to placing at least four 12 mil (305 µm) diameter vias under the device, assuming a 6.6 mil (168 µm) thick RF layer to ground. For best thermal management and datasheet performance, use as many PTH vias as physically possible. Vias shown here are 305 µm diameter in a recommended 4 x 4 array.

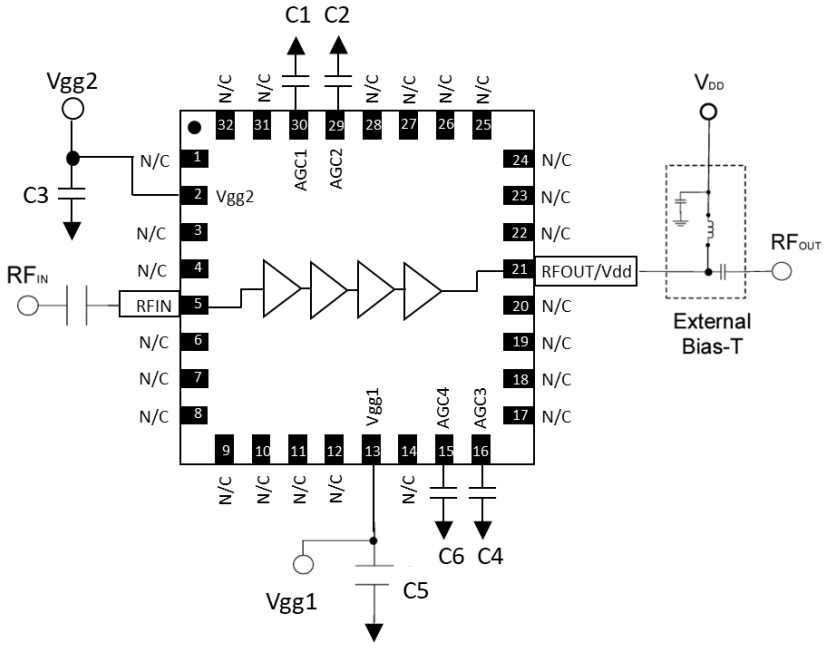
Parts List

Part	Value	Case Style
C1, C6	1000 pF	0603
C2, C4	1 µF	1206
C3, C5	100 pF	0402

Sample Board Material Specifications

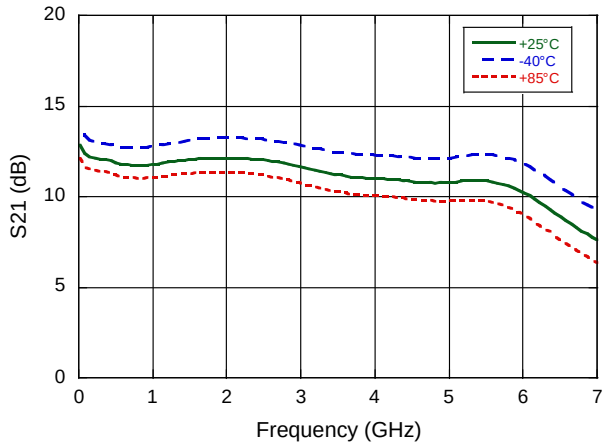
Top Layer: 1/2 oz Copper Cladding, 0.017 mm thickness
Dielectric Layer: Rogers RO4350B 0.2676 mm thickness
Bottom Layer: 1/2 oz Copper Cladding, 0.017 mm thickness
Copper on Top/Bottom Layer to be plated up additional 1 oz.
Finished overall thickness: 0.274 mm

Application Schematic

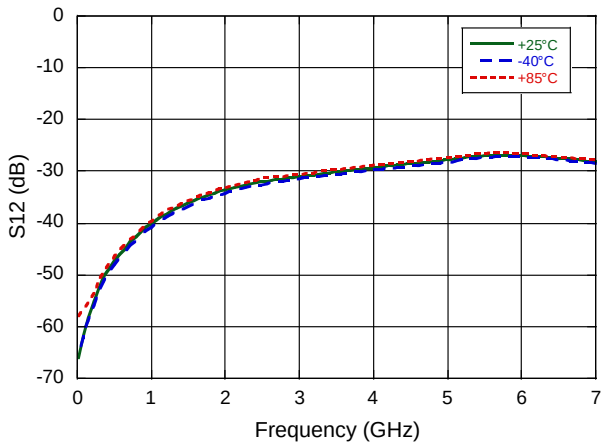


Typical Performance Curves

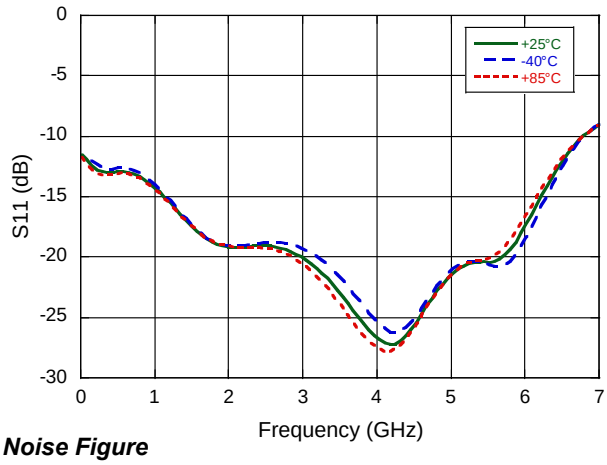
Gain



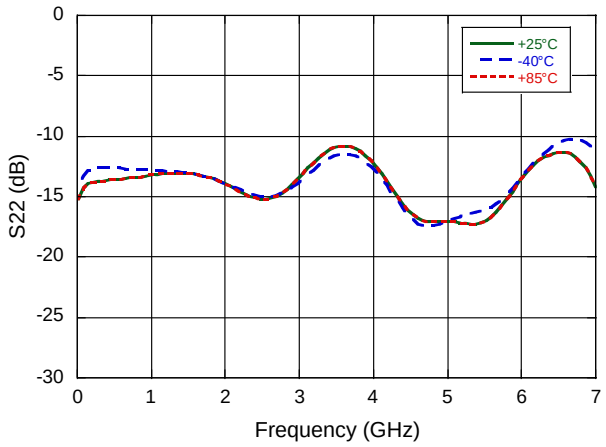
Reverse Isolation



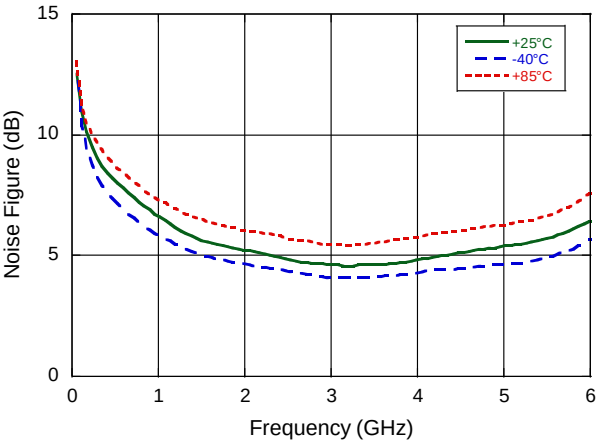
Input Return Loss



Output Return Loss

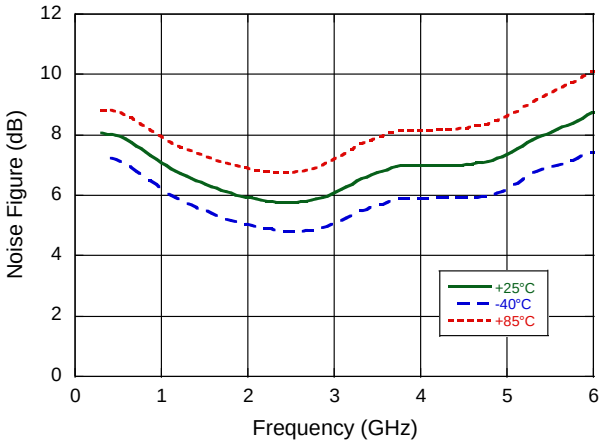


Noise Figure

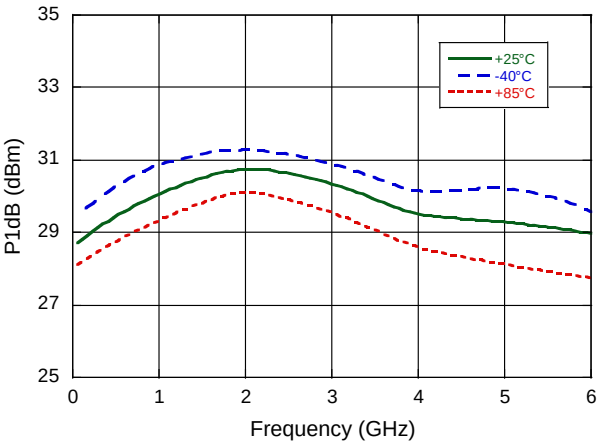


Typical Performance Curves

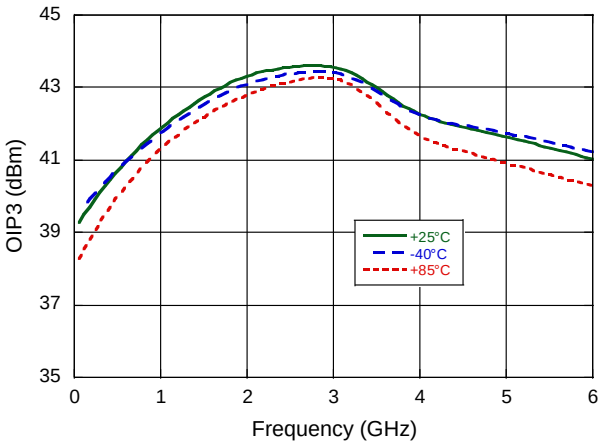
Noise Figure



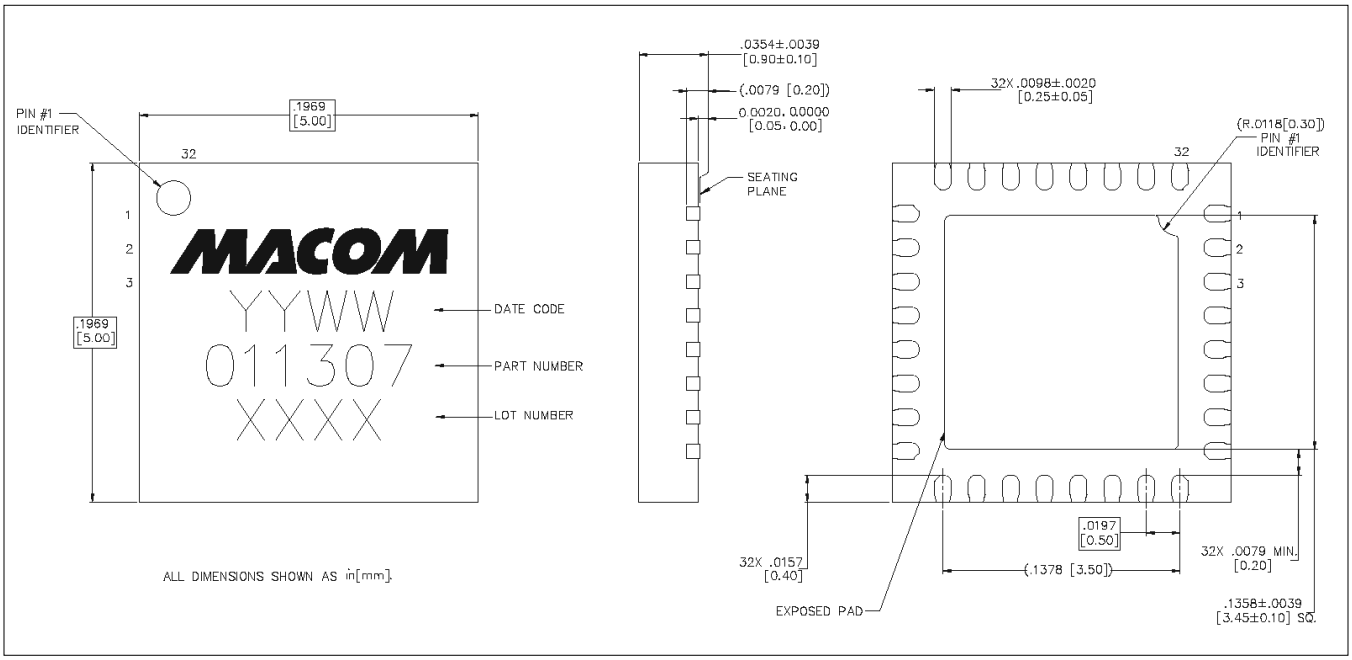
P1dB



OIP3



Lead-Free 5 mm 32-Lead PQFN†



† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.
Plating is NiPdAuAg

Revision History

Rev	Date	Change Description
V1	3/29/24	Original Release
V2	July 2024	Update Bias Sequencing