5 W, Power Amplifier
37 - 43 GHz

MAAP-FR1423-DIE
Rev. V1

Features

- Gain: 21 dB @ 40 GHz
- Output Power: 37.5 dBm @ 40 GHz
- PAE: 22% @ 40 GHz
- Power Supply: 10 V
- 50Ω Input & Output Matched
- Chip Size: 3.6 mm x 2.8 mm x 0.1 mm
- RoHS* Compliant

Applications

- Satcom
- Radar

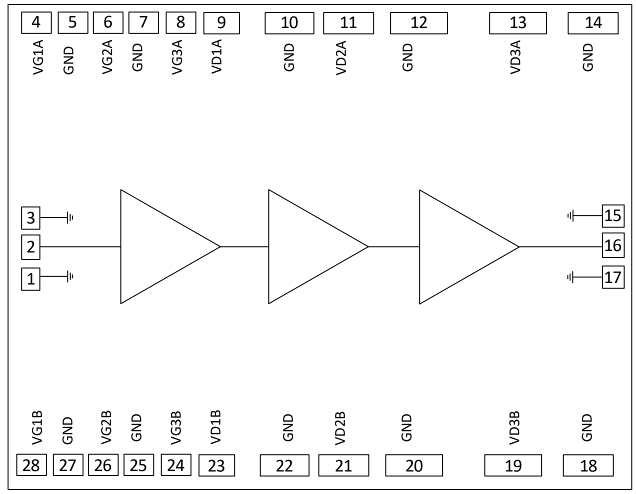
Description

The MAAP-FR1423-DIE is a high-performance GaN Power Amplifier MMIC designed to operate from 37 GHz to 43 GHz.

The amplifier has 37.5 dBm of output power and 22% PAE at 40 GHz while maintaining a safe operation of less than 200°C of junction temperature. This device is ideally suited for pulsed satellite communication and radar applications.

This product is manufactured using a high performance 100 nm gate length GaN on Si HEMT technology (D01GH). The MMIC uses gold bonding pads and backside metallization.

Functional Schematic



Pin Function[1]

Pin #	Function	Pin #	Function
1,3,5,7,10,12, 14,15,17,18, 20,22,25,27	GND	16	RF_{OUT}
2	RF_{IN}	19	VD3B
4	VG1A	21	VD2B
6	VG2A	23	VD1B
8	VG3A	24	VG3B
9	VD1A	26	VG2B
11	VD2A	28	VG1B
13	VD3A		

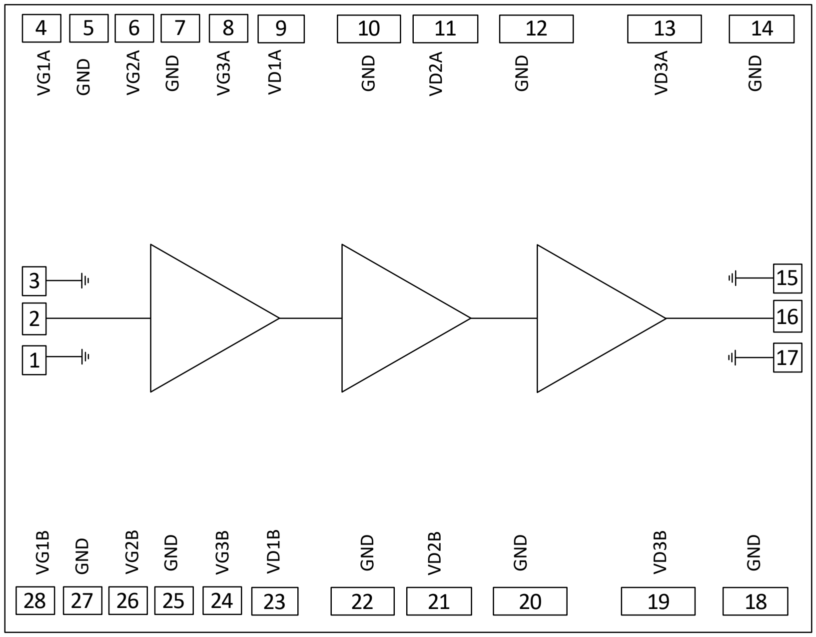
1. MACOM recommends connecting unused package pins to ground.

Ordering Information

Part Number	Description
MAAP-FR1423-DIE	bulk
MAAP-FR1423-DIESMB	Sample Board

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Pin Configuration and Functional Descriptions



Pin #	Pin Name	Description
2	RF_{IN}	RF Signal Input. This pad is matched to 50 Ω and is AC coupled.
4, 6, 8 24, 26,28	VG1,2,3A VG3,2,1B	Gate control voltage. Adjust from –2.0 V to 0 V to achieve the desired quiescent current. For bypassing 47 pF and 0.1 µF SMT capacitors are recommended. The 47 pF capacitor should be placed as closely to the die as physically possible. The positioning of the 0.1 µF capacitor is not as critical. VG1,2,3A and VG1,2,3B are internally connected. Biasing from one side is sufficient.
9, 11, 13 19, 21, 23	VD1,2,3A VD3,2,1B	Drain bias. For bypassing 47 pF and 0.1 µF SMT capacitors are recommended. The 47 pF capacitor should be placed as closely to the die as physically possible. The positioning of the 0.1 µF capacitor is not as critical. VD1,2,3A and VD1,2,3B are internally connected but must be biased from both sides.
16	RF_{OUT}	RF Signal Output. This pad is matched to 50 Ω and is AC coupled.
1,3,5,7,10,12, 14,15,17,18, 20,22,25,27	GND	These pads are grounded with thru-substrate vias.

Recommended Operating Conditions

Parameter	Symbol	Unit	Min.	Typ.	Max.
Input power	Pin	dBm	—	—	22
Voltage Bias	$VD_{1,2,3}$	V	—	10	—
Quiescent Current	$ID_1+ID_2+ID_3$	A	—	0.73	—
Junction Temperature	T_J	°C	—	—	+200
Operating Temperature	T_C	°C	-40	—	+85
Storage Temperature		°C	-40	—	+150

Absolute Maximum Ratings[5,6]

Parameter	Symbol	Unit	Min.	Max.
Drain Voltage	V_{Dxx}	V	—	+15
Gate Voltage	V_{Gxx}	V	-3	0
Junction Temperature[7,8]	T_J	°C	—	220
Storage Temperature	T_C	°C	-40	150
Maximum Temperature during assembly (do not exceed 60s)	-	°C	—	300

5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. MACOM does not recommend sustained operation near these survivability limits.
7. Operating at nominal conditions with $T_J \leq +200°C$ will ensure MTTF > 1 x 10^7 hours.
8. Junction Temperature $T_J = T_C + \Theta jc * (VDD * IDD)$, calculated at Pin = 22dBm using the IDD at 39.5 GHz where it is highest.
   a) For $T_C = +25°C$,
   $T_J = 121°C$ @ VDD=10V, IDD=2.72 A, Typical thermal resistance $\Theta jc = 3.5$ °C/W.
   b) For $T_C = +85°C$,
   $T_J = 185°C$ @ VDD=10V, IDD=2.33 A, Typical thermal resistance $\Theta jc = 4.3$ °C/W.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Handling the Die

This MMIC has fragile exposed airbridges on its surface and must be handled on the edges only using a vacuum collet or suitable tweezers. Do not touch the surface of the chip with a vacuum collet, tweezers, or fingers.

Electrical Specifications: Freq. = 37 - 43 GHz, $VD_{1,2,3}$ = 10 V, T_A = + 25°C (CW mode), Quiescent Bias Currents (ID_1 = 110 mA ID_2 = 220 mA, ID_3 = 400 mA)

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Small Signal Gain	37 GHz 40 GHz 43 GHz	dB	18 19 16	20 21 18	—
Input Reflection Coefficient	—	dB	—	-10	—
Output Reflection Coefficient	—	dB	—	-10	—
Drain Current Total $ID_{1,2,3}$	Saturated Power @ 37 GHz Saturated Power @ 40 GHz Saturated Power @ 43 GHz	A	—	2.30 2.60 2.25	—
Saturated Output Power	37 GHz @ Pin = 22 dBm 40 GHz @ Pin = 22 dBm 43 GHz @ Pin = 22 dBm	dBm	35 35 34	36.8 37.5 36.5	—
Power Added Efficiency	Saturated Power @ 37 GHz Saturated Power @ 40 GHz Saturated Power @ 43 GHz	%	14 18 14	19 22 18	—

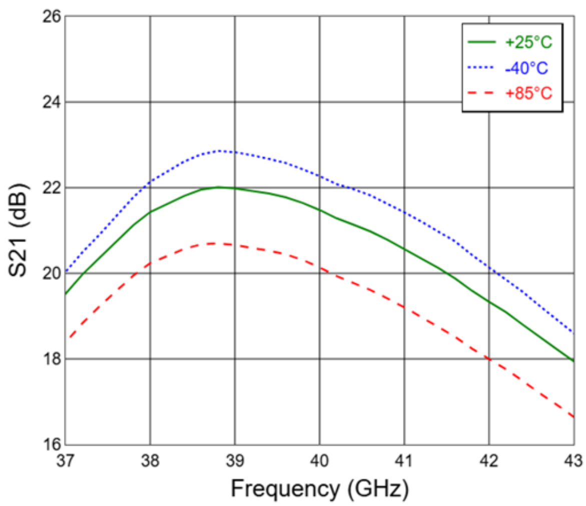
Operating the MAAP-FR1423-DIE

Turn-on
- Apply VG –2 V
- Increase VDD_1, VDD_2, and VDD_3 to 10 V
- Set ID_1, ID_2, and ID_3 by adjusting VG_1, VG_2, and VG_3 more positive
- Apply RFIN signal

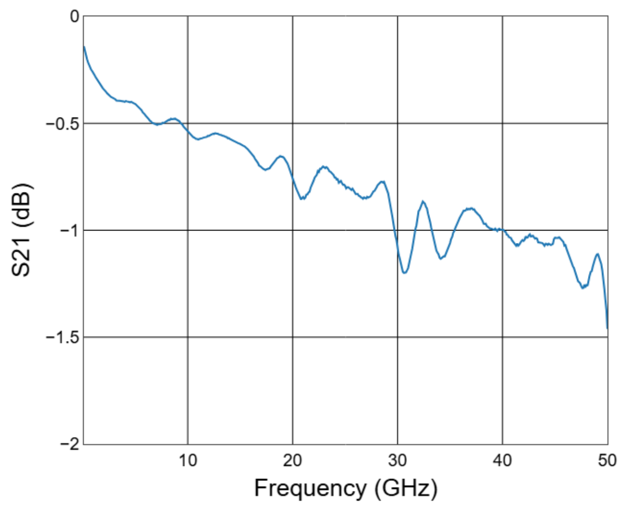
Turn-off
- Remove RFIN signal
- Decrease VG to –2 V
- Decrease VDD to 0 V

Typical Performance Curves - CW operation on evaluation board (Losses de-embedded) $V_{D1,2,3}$ = 10 V with I_{D1} = 110 mA I_{D2} = 220 mA, I_{D3} = 400 mA

Small Signal Gain vs Frequency and Temperature

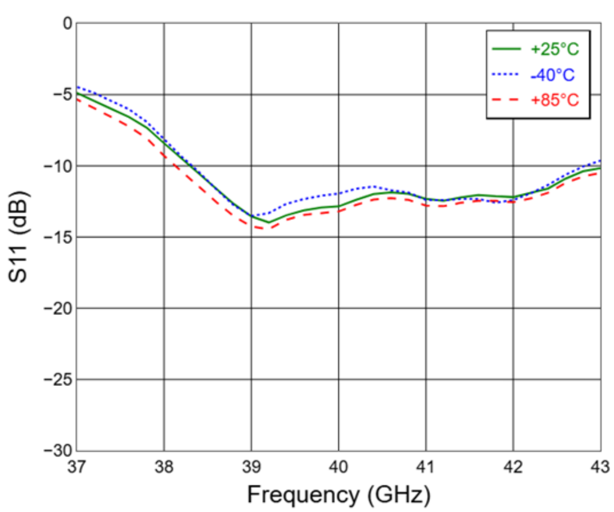


Loss from Connector to Wire-bond Plane[9]

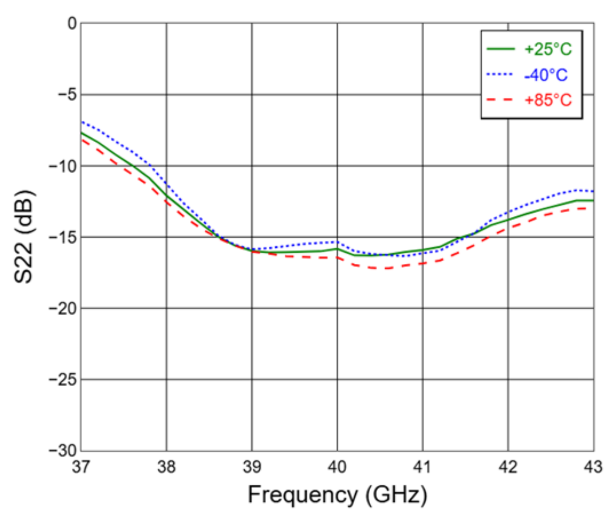


9. Losses shown for 2x thru, i.e. for input and output trace combined. An insertion loss of 0.6 dB at 40 GHz was assumed for de-embedding to account for assembly losses and fringing capacitances.

Input Return Loss vs Frequency and Temperature

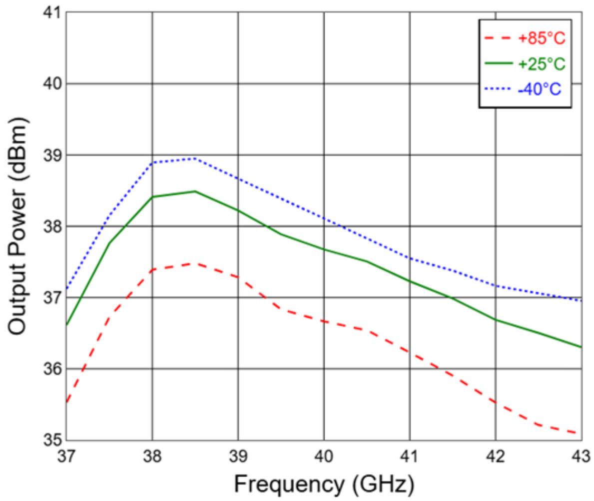


Output Return Loss vs Frequency and Temperature

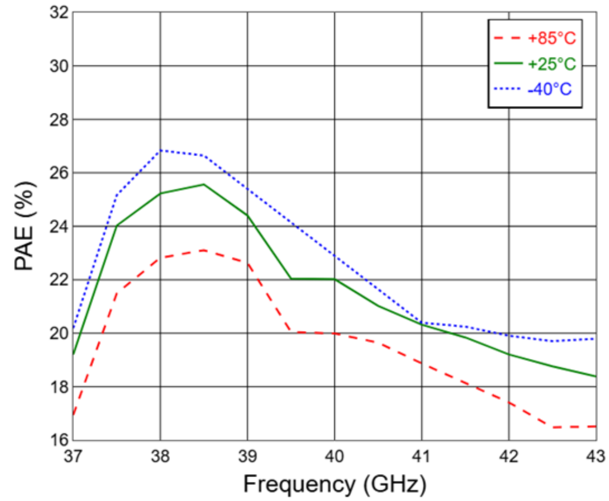


Typical Performance Curves - CW operation on evaluation board (Losses de-embedded) $V_{D1,2,3}$ = 10 V with I_{D1} = 110 mA I_{D2} = 220 mA, I_{D3} = 400 mA, Pin = 22dBm

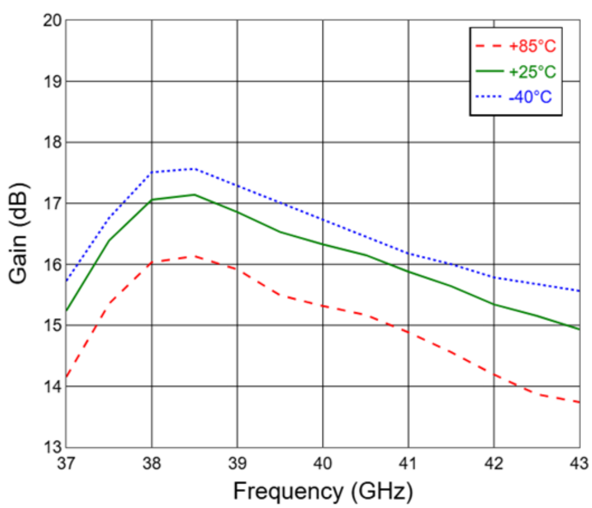
Output Power vs Frequency and Temperature



PAE vs Frequency and Temperature

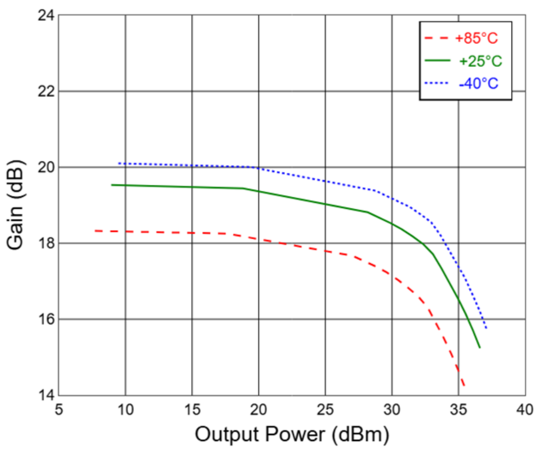


Large Signal Gain vs Frequency and Temperature

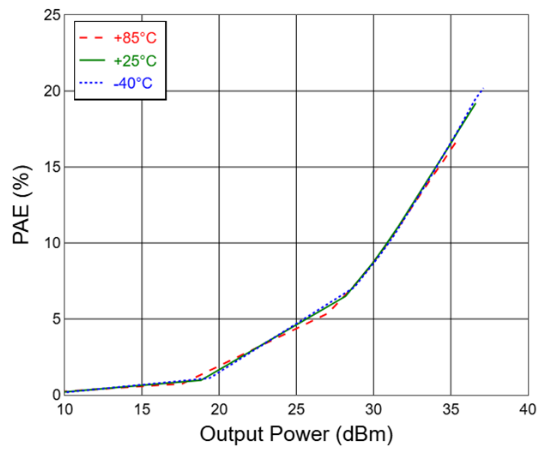


Typical Performance Curves - CW operation on evaluation board (Losses de-embedded) $V_{D1,2,3}$ = 10V with I_{D1} = 110 mA I_{D2} = 220 mA, I_{D3} = 400 mA

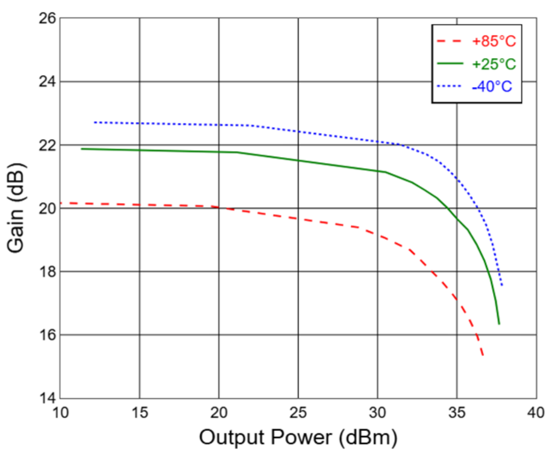
Gain @37GHz vs Pout and Temperature



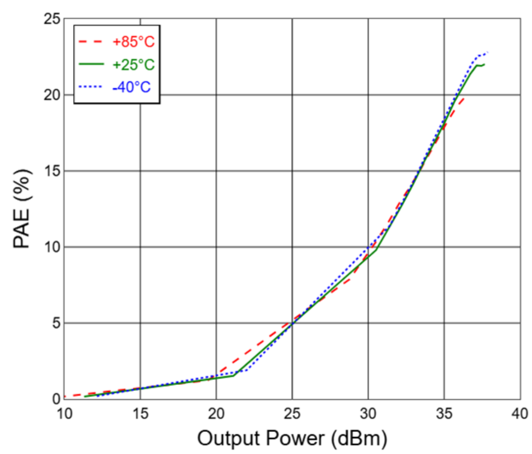
PAE @37GHz vs Pout and Temperature



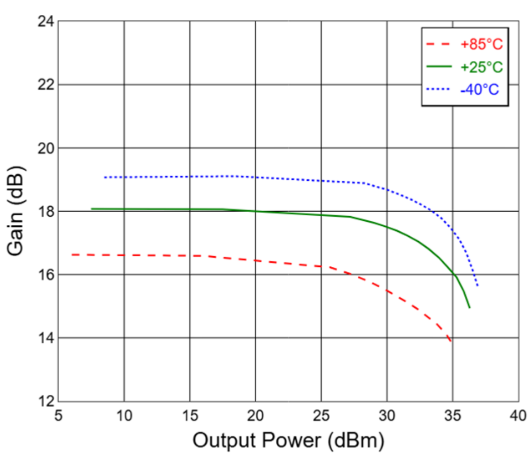
Gain @40GHz vs Pout and Temperature



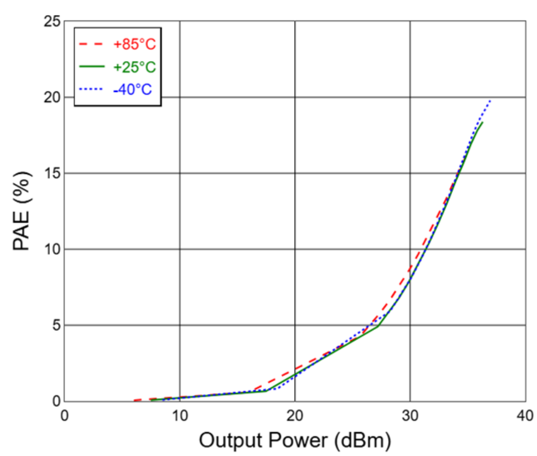
PAE @40GHz vs Pout and Temperature



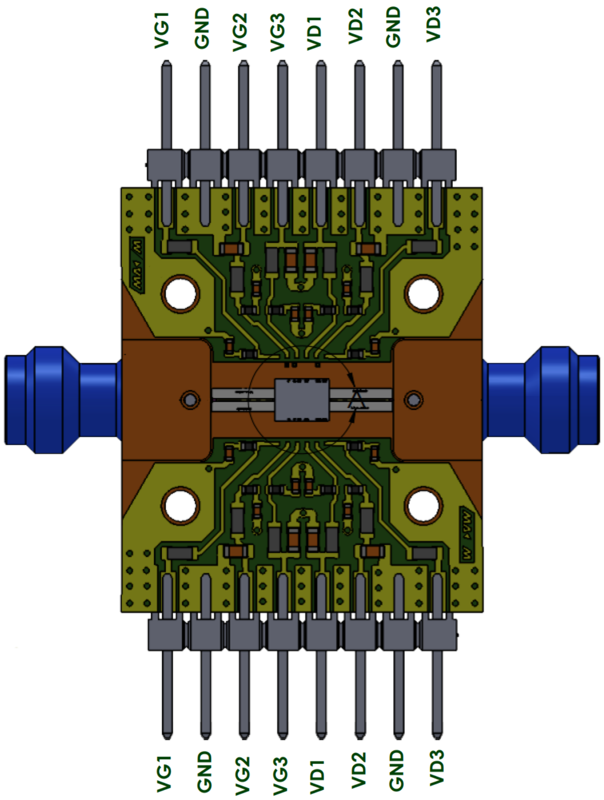
Gain @43GHz vs Pout and Temperature



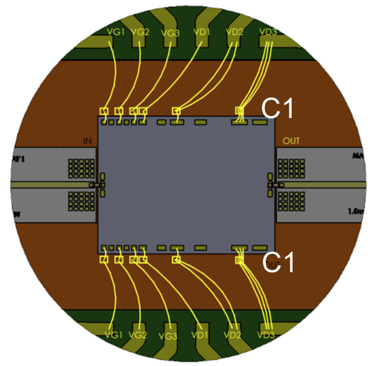
PAE @43GHz vs Pout and Temperature



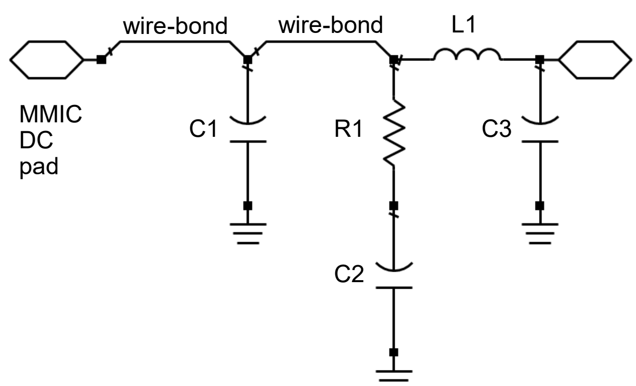
Evaluation Board



Evaluation Board (Detail A)



Evaluation Board (DC bias)



Parts List

Part	Value	Case Style	Manufacturer	Type	Manufacturer's Part number
C1	47 pF	380 × 380 µm	ATC	Single Layer Capacitor	116RG470M100TT
C2	0.1 uF	0402	Capax	Capacitor	0402X104K500SNT
R1	10 Ohm	0402	ROHM	Resistor	ESR01MZPJ100
L1	10 nH #	0603	Coilcraft	Inductor	0603HC-10NXJEW
C3	0.1 uF #	0603	KEMET	Capacitor	C0603C105K3RACTU

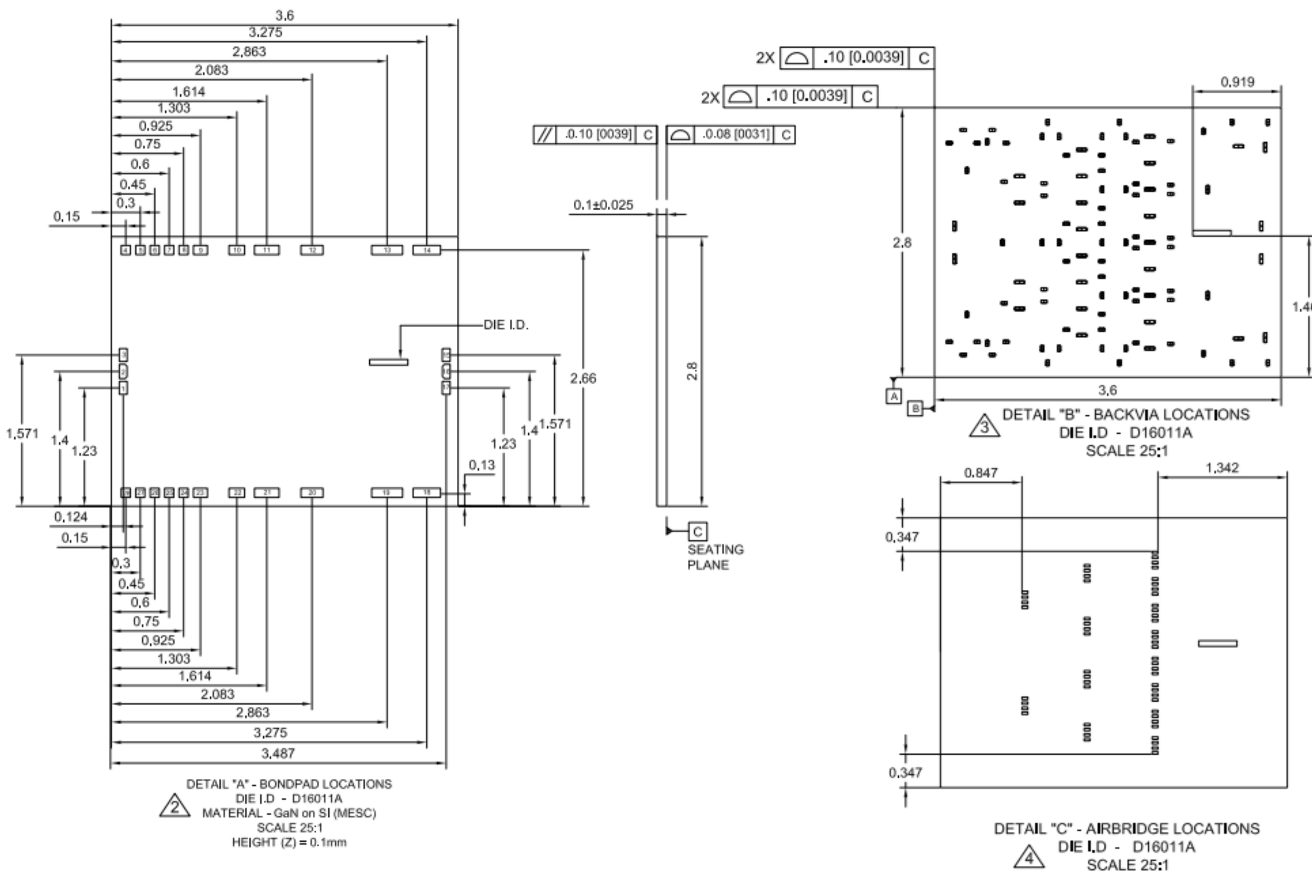
VG1 and VD3 do not have L1 and C3 due to space constraints on board.

Recommended Bonding Diagram and Application Details

For optimum performance, RF input and output transmission lines require either 75 um gold ribbon (wedge bond) or 2 x 25 um diameter gold wire bonds. The gap between the MMIC and the RF input and output lines should be a nominal 50 um.

In the shown configuration 47 pF chip capacitors are used as part of the supply bypassing network. These chip capacitors are to be placed as close to the die as practically possible. The larger 0.1 µF capacitor could be implemented using an SMT component on a PCB instead of a chip cap: in this case, proximity to the MMIC die is less

Outline



Rev	Date	Change Description
V1P	4/29/24	Document creation
V2P	5/28/25	Biasing condition update
V1	12/03/25	Final release

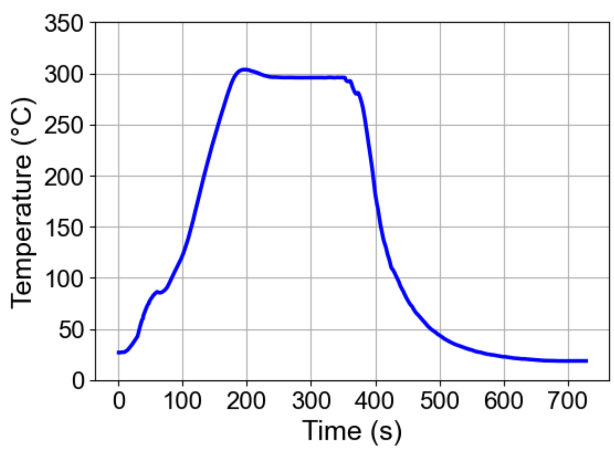
Thermal Considerations

Due to the high power dissipation of this PA, careful consideration needs to be given to the thermal path in the application. The thermal path to the heatsink must be designed to have sufficiently low thermal resistance to support a maximum of 85ºC temperature at the backside of the die. Directly mounting to a metal heatsink using one of the die attach methods outlined is highly recommended. If the MMIC is to be mounted onto a PCB, an embedded copper coin is recommended in the die attach area.

Die attach - Soldering

- To avoid permanent damages or impact on reliability during the soldering process, die temperature should never exceed 310°C.
- Temperature in excess of 300°C should not be applied to the die longer than 1 min. Toxic fumes will be generated from the part at temperatures higher than 400°C.

Recommended soldering profile using AuSn preform (17µm) and Cu Carrier with 1mm of thickness



Die attach - Epoxy

To avoid permanent damage or impact on reliability due to thermal management, epoxy with high thermal conductivity is recommended such as EPOTEK EK2000, NAMICS H9890-6A, or NAMICS H9890-11A