Power Amplifier
10.0 - 15.35 GHz

Features
- Fully Integrated Power Amplifier
- Wide Bandwidth 10.0 - 15.35 GHz
- 30 dB Small Signal Gain
- 40 dBm Third Order Intercept Point (OIP3)
- 31 dBm Output P1dB
- Integrated Power Detector
- Bias Voltage 5 V, 1.3 A
- Lead-Free 5 mm 24-lead QFN Package
- RoHS* Compliant

Description
The MAAP-110150 is a packaged linear power amplifier that operates over the range 10.0 - 15.35 GHz. The device typically provides 30 dB of gain and 40 dBm OIP3 with more than 31 dBm of output P1dB.

This power amplifier is assembled in a lead free, fully molded 5 mm QFN package and consists of a 3 stage power amplifier with integrated, on-chip peak power detector and envelope detector. The device includes on-chip ESD protection structures and DC by-pass capacitors to ease the implementation and volume assembly.

The device is well suited for use in the 10, 11, 13, 15 GHz cellular backhaul applications.

Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAAP-110150</td>
<td>Bulk</td>
</tr>
<tr>
<td>MAAP-110150-TR0500</td>
<td>Tape and Reel</td>
</tr>
<tr>
<td>MAAP-110150-001SMB</td>
<td>Sample Board</td>
</tr>
</tbody>
</table>

1. Reference Application Note M513 for reel size information.
2. All sample boards include 5 loose parts.


For further information and support please visit:
https://www.macom.com/support
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Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Units</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain Voltage (V&lt;sub&gt;D&lt;/sub&gt;)</td>
<td>10.00 - 10.30 GHz</td>
<td>V</td>
<td>7 V</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Gate Voltage (V&lt;sub&gt;G&lt;/sub&gt;)</td>
<td>-3 V</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Drain to Gate Voltage (V&lt;sub&gt;D&lt;/sub&gt;-V&lt;sub&gt;G&lt;/sub&gt;)</td>
<td>10 V</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C to +150°C</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>+175°C</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Maximum Operating Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>P&lt;sub&gt;Diss&lt;/sub&gt;</td>
<td>10 W</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>+150°C</td>
</tr>
</tbody>
</table>

5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. MACOM does not recommend sustained operation near these survivability limits.
7. Operating at nominal conditions with T<sub>J</sub> ≤ 150°C will ensure MTTF > 1 x 10<sup>6</sup> hours.
8. Channel temperature directly affects device MTTF. Channel temperature should be kept as low as possible to maximize lifetime. Thermal resistance, Θ<sub>JC</sub>, is 9.2°C/W.
9. For saturated performance, it is recommended that the sum of (2V<sub>DD</sub> + abs (V<sub>GG</sub>)) < 15 V.
### PCB Layout

![PCB Layout Image]

### Parts List

<table>
<thead>
<tr>
<th>Part</th>
<th>Value</th>
<th>Case Style</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1,C3,C5,C7,C8, C9,C10,C12,C16</td>
<td>100 nF</td>
<td>0402</td>
</tr>
<tr>
<td>C2,C4,C6,C11,C15</td>
<td>4.7 µF</td>
<td>0603</td>
</tr>
<tr>
<td>R1,R3</td>
<td>100 Ω</td>
<td>0402</td>
</tr>
<tr>
<td>R2</td>
<td>10 KΩ</td>
<td>0402</td>
</tr>
<tr>
<td>R4,R5</td>
<td>560 Ω</td>
<td>0402</td>
</tr>
</tbody>
</table>

### Application Schematic

![Application Schematic Image]
Biasing
All gates should be pinched-off, \( V_G < -2 \text{ V} \), before applying the drain voltage, \( V_D = 5 \text{ V} \) (do not exceed maximum specified \( V_{DG} \) value of 10 V). Then the gate voltages can be increased until the desired quiescent drain current is reached in each stage. The recommended quiescent bias is \( V_D = 5 \text{ V} \), \( I_{D1} + I_{D2} = 1300 \text{ mA} \) (total). The performance in this datasheet has been measured with a fixed gate voltage and no drain current regulation under large signal operation. It is also possible to regulate the drain current dynamically, to limit the DC power dissipation under RF drive. To turn off the device, the turn on bias sequence should be followed in reverse.

Detector Operation
MAAP-110150 includes a power and envelope detector. As per the application schematic, the power detector requires an external 5 V supply and the envelope detector requires -5 V. The output from the resistive voltage divider can be fed into an ADC or multimeter for the result.

Bias Arrangement
Each DC pin (\( V_{D1,2}, V_{D3} \) and \( V_{G1,2}, V_{G3} \)) needs to have bypass capacitance of 100 nF mounted as close to the packaged device as possible.

Handling Procedures
Please observe the following precautions to avoid damage:

Static Sensitivity
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these CDM class C1, HBM Class 0A devices.
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Typical Performance Curves: $V_D = 5\,V$, $I_{DQ} = 1.3\,A$, $V_G = -1.05 \sim -0.85\,V$, $T_A = +25^\circ C$

- Broadband S-Parameters vs. Freq (GHz), $V_d = 5\,V$, $I_d = 1.3\,A$
- Gain (S21) vs. Freq (GHz), $V_d = 5\,V$, $I_d = 1.3\,A$
- Return Loss (S11/S22) vs. Freq (GHz), $V_d = 5\,V$, $I_d = 1.3\,A$
- P1dB/P3dB/Psat (dBm) vs. Freq (GHz), $V_d = 5\,V$, $I_d = 1.3\,A$
- Output IP3 (dBm) vs. Freq (GHz), $V_d = 5\,V$, $I_d = 1.3\,A$
- Output IP3 (dBm) vs. SCL Output Pwr (dBm), $V_d = 5\,V$, $I_d = 1.3\,A$
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Typical Performance Curves: $V_D = 5\, \text{V}$, $I_{DQ} = \text{Various}$, $V_G = -1.05 \sim -0.85\, \text{V}$, $T_A = +25\,\text{°C}$
Lead-Free 5 mm 24-Lead PQFN

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 3 requirements.
Plating is NiPdAu