Features
- 15 W Power Amplifier
- 42 dBm Saturated Pulsed Output Power
- 17 dB Large Signal Gain
- $P_{\text{SAT}}>40\%$ Power Added Efficiency
- Dual Sided Bias Architecture
- On Chip Bias Circuit
- 100% On-Wafer DC, RF and Output Power Testing
- 100% Visual Inspection to MIL-STD-883 Method 2010

Description
The MAAP-015036 is a two stage GaAs MMIC power amplifier operating from 8.5 - 10.5 GHz, with a saturated pulsed output power of 42 dBm and a large signal gain of 18 dB.

This power amplifier uses GaAs pHEMT device technology and is based upon optical gate lithography to ensure high repeatability and uniformity. The chip has surface passivation for protection and backside via holes and gold metallisation to allow a conductive epoxy die attach process.

This device is well suited for communications, Point to Point radio and radar applications.

Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAAP-015036-DIE</td>
<td>Die in Gel Pack(^1)</td>
</tr>
<tr>
<td>MAAP-015036-DIEEV1</td>
<td>Sample Board Direct Gate Bias</td>
</tr>
<tr>
<td>MAAP-015036-DIEEV2</td>
<td>Sample Board On-Chip Gate Bias</td>
</tr>
</tbody>
</table>

1. Die quantity varies.

Functional Schematic

Pin Configuration\(^2\)

<table>
<thead>
<tr>
<th>Pad No.</th>
<th>Function</th>
<th>Pad No.</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$V_{G1}$</td>
<td>15</td>
<td>$V_{G2}$</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>16</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>$V_{SS1}$</td>
<td>17</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>$V_{1.5}$</td>
<td>18</td>
<td>$V_{D1}$</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>19</td>
<td>$V_{G2}$</td>
</tr>
<tr>
<td>6</td>
<td>$V_{SS2}$</td>
<td>20</td>
<td>GND</td>
</tr>
<tr>
<td>7</td>
<td>$V_{2.5}$</td>
<td>21</td>
<td>$V_{2.5}$</td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>22</td>
<td>$V_{SS2}$</td>
</tr>
<tr>
<td>9</td>
<td>$V_{G2}$</td>
<td>23</td>
<td>GND</td>
</tr>
<tr>
<td>10</td>
<td>$V_{D2}$</td>
<td>24</td>
<td>$V_{1.5}$</td>
</tr>
<tr>
<td>11</td>
<td>GND</td>
<td>25</td>
<td>$V_{SS1}$</td>
</tr>
<tr>
<td>12</td>
<td>GND</td>
<td>26</td>
<td>GND</td>
</tr>
<tr>
<td>13</td>
<td>$V_{D2}$</td>
<td>27</td>
<td>$V_{G1}$</td>
</tr>
<tr>
<td>14</td>
<td>$RF_{OUT}$</td>
<td>28</td>
<td>$RF_{IN}$</td>
</tr>
</tbody>
</table>

2. Backside metal is RF, DC and thermal ground.

\(^{1}\) Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

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## Electrical Specifications - Pulsed Operation: Duty Cycle = 5%, Pulse = 5 µs,
Freq. = 8.5 - 10.5 GHz, \( T_A = +25°C \), \( Z_0 = 50 \, \Omega \), \( P_{IN} = 26 \, \text{dBm} \), \( V_G = -0.9 \, \text{V} \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Units</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (Large Signal)</td>
<td>dB</td>
<td>—</td>
<td>17</td>
<td>—</td>
</tr>
<tr>
<td>Gain</td>
<td>dB</td>
<td>—</td>
<td>17</td>
<td>—</td>
</tr>
<tr>
<td>Gain Flatness</td>
<td>dB</td>
<td>—</td>
<td>1</td>
<td>—</td>
</tr>
<tr>
<td>Input Return Loss</td>
<td>dB</td>
<td>—</td>
<td>-15</td>
<td>—</td>
</tr>
<tr>
<td>Output Return Loss</td>
<td>dB</td>
<td>—</td>
<td>-25</td>
<td>—</td>
</tr>
<tr>
<td>Saturated Output Power (8.5 - 10.5 GHz)</td>
<td>dBm</td>
<td>40.5</td>
<td>42</td>
<td>—</td>
</tr>
<tr>
<td>Saturated Output Power (9.0 - 10.0 GHz)</td>
<td>dBm</td>
<td>41.0</td>
<td>42</td>
<td>—</td>
</tr>
<tr>
<td>Power Added Efficiency</td>
<td>%</td>
<td>—</td>
<td>45</td>
<td>—</td>
</tr>
<tr>
<td>8.5 - 9.0 GHz</td>
<td>—</td>
<td>45</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>9.0 - 10.0 GHz</td>
<td>—</td>
<td>45</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>10.0 - 10.5 GHz</td>
<td>—</td>
<td>43</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>Drain Bias Voltage</td>
<td>V</td>
<td>—</td>
<td>8.0</td>
<td>—</td>
</tr>
<tr>
<td>Drain Current</td>
<td>A</td>
<td>3.5</td>
<td>4.8</td>
<td>5.5</td>
</tr>
</tbody>
</table>

### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Absolute Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Power</td>
<td>30 dBm</td>
</tr>
<tr>
<td>Drain Voltage</td>
<td>+8.5 V</td>
</tr>
<tr>
<td>Gate Voltage</td>
<td>-3.0 V &lt; ( V_G &lt; -0.0 , \text{V} )</td>
</tr>
<tr>
<td>Bias Voltage</td>
<td>-6.0 V &lt; ( V_{SS} &lt; -4.0 , \text{V} )</td>
</tr>
<tr>
<td>Drain Current</td>
<td>6 A</td>
</tr>
<tr>
<td>Gate Current (Direct Bias)</td>
<td>160 mA</td>
</tr>
<tr>
<td>Gate Current (On Chip Bias)</td>
<td>165 mA</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Junction Temperature(^5,6)</td>
<td>+170°C</td>
</tr>
</tbody>
</table>

3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. MACOM does not recommend sustained operation near these survivability limits.
5. Operating at nominal conditions with \( T_J \leq +160°C \) will ensure MTTF > 1.0 \times 10^6 \, \text{hours}.
6. Typical thermal resistance (\( \Theta JC \)) = 5.7°C/W.

### Handling Procedures

Please observe the following precautions to avoid damage:

#### Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices.
Power Amplifier, 15 W
8.5 - 10.5 GHz

Bonding Diagram - On Chip Bias

Bonding Diagram - Direct Gate Bias

7. Components C1 - C8 are all 120 pF chips.

MMIC Bare Die

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Pulsed Performance Curves over Gate Voltage: $V_D = 8\, \text{V}$, Duty Cycle = 5%, Pulse = 5 $\mu\text{s}$

**Gain vs. Frequency**

**Reverse Isolation vs. Frequency**

**Input Return Loss vs. Frequency**

**Output Return Loss vs. Frequency**
Pulsed Performance Curves over Gate Voltage: $P_{IN} = 25$ dBm, Duty Cycle = 5%, Pulse = 5 µs

**Gain vs. Frequency**

- Gain versus Frequency graph showing the gain in dB as a function of frequency for different gate voltages.

**Output Power vs. Frequency**

- Output power versus frequency graph showing the output power in dBm as a function of frequency for different gate voltages.

**Drain Current vs. Frequency**

- Drain current versus frequency graph showing the drain current in A as a function of frequency for different gate voltages.

**PAE vs. Frequency**

- PAE versus frequency graph showing the power added efficiency as a function of frequency for different gate voltages.
Pulsed Performance Curves over Freq.: $V_G = -0.9$ V, Duty Cycle = 5%, Pulse = 5 µs

**Gain vs. Input Power**

**Output Power vs. Input Power**

**Drain Current vs. Input Power**

**PAE vs. Input Power**

**Gate Current vs. Input Power @ 9 GHz**
Pulsed Performance Curves over Temperature:
$V_G = -0.9\, \text{V}$, $P_{IN} = 25\, \text{dBm}$, Duty Cycle = 5%, Pulse = 5 µs

**Gain vs. Frequency**

**Output Power vs. Frequency**

**Drain Current vs. Frequency**

**PAE vs. Frequency**

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Pulsed Performance Curves over Bias Circuit Voltage, Duty Cycle = 5%, Pulse = 5 µs

**Gain vs. Frequency**

**Reverse Isolation vs. Frequency**

**Input Return Loss vs. Frequency**

**Output Return Loss vs. Frequency**
Pulsed Performance Curves over Bias Circuit Voltage:
$P_{IN} = 25$ dBm, Duty Cycle = 5%, Pulse = 5 µs

**Gain vs. Frequency**

- $V_{GS} = 4.5$ V
- $V_{GS} = 6.0$ V
- $V_{GS} = 5.5$ V
- $V_{GS} = 6.0$ V

**Output Power vs. Frequency**

- $V_{GS} = 4.5$ V
- $V_{GS} = 6.0$ V
- $V_{GS} = 5.5$ V
- $V_{GS} = 6.0$ V

**Drain Current vs. Frequency**

- $V_{GS} = 4.5$ V
- $V_{GS} = 6.0$ V
- $V_{GS} = 5.5$ V
- $V_{GS} = 6.0$ V

**PAE vs. Frequency**

- $V_{GS} = 4.5$ V
- $V_{GS} = 6.0$ V
- $V_{GS} = 5.5$ V
- $V_{GS} = 6.0$ V

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Pulsed Performance Curves over Frequency:
Bias Circuit Voltage = -5 V, Duty Cycle = 5%, Pulse = 5 µs

**Gain vs. Input Power**

```
Gain (dB)
22  20  18  16  14  12  10
5  10  15  20  25  Input Power (dBm)
```

```
8.0 GHz  10.0 GHz
8.5 GHz  10.5 GHz
9.0 GHz  11.0 GHz
9.5 GHz  11.5 GHz
```

**Output Power vs. Input Power**

```
Pout (dBm)
45  40  35  30  25  20  15  10  5  0
5  10  15  20  25  Input Power (dBm)
```

```
8.0 GHz  10.0 GHz
8.5 GHz  10.5 GHz
9.0 GHz  11.0 GHz
9.5 GHz  11.5 GHz
```

**Drain Current vs. Input Power**

```
Id (A)
6  5  4  3  2  1
5  10  15  20  25  Input Power (dBm)
```

```
8.0 GHz  10.0 GHz
8.5 GHz  10.5 GHz
9.0 GHz  11.0 GHz
9.5 GHz  11.5 GHz
```

**PAE vs. Input Power**

```
PAE (%)
60  50  40  30  20  10  0
5  10  15  20  25  Input Power (dBm)
```

```
8.0 GHz  10.0 GHz
8.5 GHz  10.5 GHz
9.0 GHz  11.0 GHz
9.5 GHz  11.5 GHz
```

**Bias Circuit Current vs. Input Power**

```
ISS Total (mA)
125  120  115  110  105
5  10  15  20  25  Input Power (dBm)
```

```
8.0 GHz  10.0 GHz
8.5 GHz  10.5 GHz
9.0 GHz  11.0 GHz
9.5 GHz  11.5 GHz
```
Applications Section

Application Notes

Note 1 - Biasing
The gate bias is applied in one of the following:
1. Direct Gate Bias:- $V_{G1}$ & $V_{G2}$ provide the direct gate bias input to the 2 MMIC stages. This method of biasing allows the user to control the total drain current without the scaling factor provided by the bias circuit. It is recommended that the gate voltage is supplied by both sides of the die. Biasing from one side is optional. Optimum performance can be achieved with a -0.9 V operation.
2. Bias Circuit Biasing:- Applying -5 V to $V_{SS1}$ & $V_{SS2}$, will typically draw 4.5 A with no further adjustment necessary. Wafer lot variation may result in some devices experiencing higher or lower drain currents than the typical 4.5 A. It is recommended that the bias circuits on both sides of the PA are used. Biasing from one side is optional.

Note 2 - Bias Sequence
When switching on the PA, in each case, the gate bias must be applied before the drain voltage is applied. The drain voltage $V_{D1}$ & $V_{D2}$ should be biased from the top and bottom sides of the die.

Note 3 - Decoupling Circuits
Each bias pad, $V_G$, $V_{SS}$ & $V_D$ must have a decoupling capacitor of 120 pF as close to the device as possible, as is shown in the bonding diagrams. Symmetrical decoupling circuits must be maintained on both sides of the die for bias circuit or direct gate bias operation. Under pulsed operation a large capacitance on the drain will cause a “ringing” effect on the supply voltage. This potentially produces a high voltage at the PA terminals. A recommended decoupling circuit is provided where shunt decoupling capacitors are connected in series with a resistor to minimize this effect.

Note 4 - Pulse Operation
The performance of the MAAP-015036 is characterized under pulsed conditions with a duty cycle of 5% consisting of a pulse width of 5 µS applied to the drain. Under pulsed conditions the gate is constantly biased using either the on chip bias circuit or using a gate voltage directly applied to the PA. It is recommended that the die is mounted with an adequate thermal solution.

Note 5 - Input / Output Transitions
The PA performance must be achieved in a 50 Ω impedance environment on the RF input and output. To maintain performance three bond wires are recommended on the output of the PA each with a maximum length of less than 600 µm. Longer bond wire lengths can be used providing bond pad compensation, in the form of a stub, is used on the application board.
Application Circuit

[Diagram of the Application Circuit with labels for V_{G1}, V_{G2}, V_{S1}, V_{S2}, V_{D1}, and V_{D2}.]

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Applications Section

Handling and Assembly

Die Attachment
This product is manufactured from 0.100 mm (0.004") thick substrate and has vias through to the backside to enable grounding to the circuit. Microstrip substrates should be brought as close to the die as possible and bond wire lengths on the input and output kept as short as possible. The mounting surface should be clean and flat.

If using conductive epoxy, recommended epoxies are Tanaka TS3332LD, Die Mat DM6030HK, Abletherm 2600AT or DM6030HK-Pt cured per the manufacturer's cure schedule. Epoxy should be applied in accordance with the manufacturers specifications and should avoid contact with the top surface of the die. An epoxy fillet should be visible around the total die periphery. For additional information please see the MACOM "Epoxy Specifications for Bare Die" application note.

If eutectic mounting is preferred, then a flux-less gold-tin (AuSn) preform, approximately 0.0012 thick, placed between the die and the attachment surface should be used. A die attach bonder that utilizes a heated collet and provides scrubbing action to ensure total wetting to prevent void formation in a nitrogen atmosphere is recommended. The gold-tin eutectic (80% Au 20% Sn) has a melting point of approximately 280°C (Note: Gold Germanium should be avoided). The work station temperature should be 310°C +/-10°C. Exposure time to these extreme temperatures should be kept to minimum. The die and collet should be pre-heated, to avoid excessive thermal shock during assembly. Avoidance of air bridges and force impact are critical during placement.

Wire Bonding
Windows are provided in the surface passivation above the bond pads to allow wire bonding to the die’s gold bond pads. The recommended wire bonding procedure uses 0.076 mm x 0.013 mm (0.003" x 0.0005") 99.99% pure gold ribbon with 0.5-2% elongation to minimize RF port bond inductance. Gold 0.025 mm (0.001") diameter wedge or ball bonds are acceptable for DC Bias connections. Aluminium wire should be avoided. Thermo-compression bonding is recommended though thermo-sonic bonding may be used providing the ultrasonic content of the bond is minimized. Bond force, time and ultrasonic's are all critical parameters. Bonds should be made from the bond pads on the die to the package or substrate. All bonds should be as short as possible.