MAAP-015035-DIE

Power Amplifier, 12 W
8.5 - 11.5 GHz

Features
- 12 W X-Band Power Amplifier
- 36 dB Small Signal Gain
- 41 dBm Saturated Pulsed Output Power
- 40% Power Added Efficiency
- On Chip Gate Bias Circuit
- 100% On-wafer DC & RF Power Tested
- 100% Visual Inspection to MIL-STD-833
- Bare Die

Description
The MAAP-015035-DIE is a three stage 8.5 - 11.5 GHz GaAs pHEMT MMIC power amplifier capable of achieving a saturated pulsed output power of 41 dBm and a small signal gain of 36 dB. The gate terminals of the power amplifier can be biased directly using a direct gate voltage or using an on chip gate bias circuit. The chip includes surface passivation for added protection and reliability.

This device is well suited for communication and radar applications.

Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAAP-015035-DIE</td>
<td>Die in Vacuum release gel pack</td>
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</table>

Functional Schematic

Pad Configuration

<table>
<thead>
<tr>
<th>Pad #</th>
<th>Function</th>
<th>Pad #</th>
<th>Function</th>
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<tbody>
<tr>
<td>1</td>
<td>$V_G1$</td>
<td>17</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>Bias Circuit GND</td>
<td>18</td>
<td>$V_D3$</td>
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<tr>
<td>3</td>
<td>GND</td>
<td>19</td>
<td>$V_D2$</td>
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<tr>
<td>4</td>
<td>$V_B1$</td>
<td>20</td>
<td>$V_G3$</td>
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<tr>
<td>5</td>
<td>$V_D1$</td>
<td>21</td>
<td>Bias Circuit GND</td>
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<tr>
<td>6</td>
<td>$V_G2$</td>
<td>22</td>
<td>$V_B3$</td>
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<tr>
<td>7</td>
<td>Bias Circuit GND</td>
<td>23</td>
<td>$V_B2$</td>
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<tr>
<td>8</td>
<td>GND</td>
<td>24</td>
<td>GND</td>
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<tr>
<td>9</td>
<td>$V_B2$</td>
<td>25</td>
<td>Bias Circuit GND</td>
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<tr>
<td>10</td>
<td>$V_B3$</td>
<td>26</td>
<td>$V_G2$</td>
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<td>11</td>
<td>Bias Circuit GND</td>
<td>27</td>
<td>$V_D1$</td>
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<td>12</td>
<td>$V_G3$</td>
<td>28</td>
<td>$V_B1$</td>
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<tr>
<td>13</td>
<td>$V_D2$</td>
<td>29</td>
<td>GND</td>
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<tr>
<td>14</td>
<td>$V_D3$</td>
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<td>Bias Circuit GND</td>
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<tr>
<td>15</td>
<td>GND</td>
<td>31</td>
<td>$V_G1$</td>
</tr>
<tr>
<td>16</td>
<td>RF_OUT</td>
<td>32</td>
<td>RF_IN</td>
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* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

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DC-0004809
Power Amplifier, 12 W
8.5 - 11.5 GHz

Electrical Specifications:
Freq. = 8.5 - 11.5 GHz, T_A = +25°C, Duty Cycle = 5%, Pulse = 5 µs, P_IN = 8 dBm, V_G = -0.9 V

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Units</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
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<tbody>
<tr>
<td>Gain (Large Signal)</td>
<td>dB</td>
<td>32</td>
<td>33</td>
<td>—</td>
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<tr>
<td>Gain</td>
<td>dB</td>
<td>—</td>
<td>36</td>
<td>—</td>
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<tr>
<td>Gain Flatness</td>
<td>dB</td>
<td>—</td>
<td>1</td>
<td>—</td>
</tr>
<tr>
<td>Input Return Loss</td>
<td>dB</td>
<td>—</td>
<td>12</td>
<td>—</td>
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<tr>
<td>Output Return Loss</td>
<td>dB</td>
<td>—</td>
<td>10</td>
<td>—</td>
</tr>
<tr>
<td>Saturated Output Power</td>
<td>dBm</td>
<td>40</td>
<td>41</td>
<td>—</td>
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<tr>
<td>Power Added Efficiency</td>
<td>%</td>
<td>—</td>
<td>35</td>
<td>40</td>
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<tr>
<td>8.5 - 9.0 GHz</td>
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<tr>
<td>9.0 - 10.0 GHz</td>
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<tr>
<td>10.0 - 11.5 GHz</td>
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<tr>
<td>Drain Bias Voltage</td>
<td>V</td>
<td>—</td>
<td>8.0</td>
<td>—</td>
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<tr>
<td>Drain Current</td>
<td>A</td>
<td>2.5</td>
<td>3.0</td>
<td>5.5</td>
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Absolute Maximum Ratings1,2
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<tr>
<th>Parameter</th>
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<tbody>
<tr>
<td>Input Power</td>
<td>12 dBm</td>
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<tr>
<td>Drain Voltage</td>
<td>8.5 V</td>
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<tr>
<td>Gate Voltage</td>
<td>-2.0 V &lt; V_G &lt; -0.7 V</td>
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<tr>
<td>Bias Voltage</td>
<td>-6.5 V &lt; V_B &lt; -4.5 V</td>
</tr>
<tr>
<td>Drain Current</td>
<td>6 A</td>
</tr>
<tr>
<td>Gate Current (Direct Bias)</td>
<td>30 mA</td>
</tr>
<tr>
<td>Gate Current (On Chip Bias)</td>
<td>180 mA</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Junction Temperature3,4</td>
<td>+175°C</td>
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Handling Procedures
Please observe the following precautions to avoid damage:

Static Sensitivity
Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.
Bonding Diagram - On Chip Bias

Bonding Diagram - Direct Gate Bias

5. Components C1 - C12 are all 100 pF chips.

MMIC Bare Die
Power Amplifier, 12 W
8.5 - 11.5 GHz

Typical Pulsed Performance Curves over Gate Voltage

**Gain vs. Frequency**

![Graph showing Gain vs. Frequency for different gate voltages](image)

**Reverse Isolation vs. Frequency**

![Graph showing Reverse Isolation vs. Frequency for different gate voltages](image)

**Input Return Loss vs. Frequency**

![Graph showing Input Return Loss vs. Frequency for different gate voltages](image)

**Output Return Loss vs. Frequency**

![Graph showing Output Return Loss vs. Frequency for different gate voltages](image)
Typical Pulsed Performance Curves over Gate Voltage: $P_{IN} = 10$ dBm

**Gain vs. Frequency**

- **Frequency (GHz):** 8, 9, 10, 11, 12
- **Gain (dB):** 24, 26, 28, 30, 32, 34
- **Gate Voltage Levels:** VG = -0.7 V, -0.8 V, -0.9 V, -1.0 V, -1.1 V

**Output Power vs. Frequency**

- **Frequency (GHz):** 8, 9, 10, 11, 12
- **Output Power (dBm):** 34, 36, 38, 40, 42, 44
- **Gate Voltage Levels:** VG = -0.7 V, -0.8 V, -0.9 V, -1.0 V, -1.1 V

**Drain Current vs. Frequency**

- **Frequency (GHz):** 2.0, 2.5, 3.0, 3.5, 4.0, 4.5, 5.0, 5.5, 6.0
- **Drain Current (A):** 2.0, 2.5, 3.0, 3.5, 4.0, 4.5, 5.0
- **Gate Voltage Levels:** VG = -0.7 V, -0.8 V, -0.9 V, -1.0 V, -1.1 V

**PAE vs. Frequency**

- **Frequency (GHz):** 8, 9, 10, 11, 12
- **PAE (%):** 10, 15, 20, 25, 30, 35, 40, 45, 50
- **Gate Voltage Levels:** VG = -0.7 V, -0.8 V, -0.9 V, -1.0 V, -1.1 V
Typical Pulsed Performance Curves over Frequency: $V_G = -0.9$ V

Gain vs. Input Power

Output Power vs. Input Power

Drain Current vs. Input Power

PAE vs. Input Power

Gate Current vs. Input Power
Typical Pulsed Performance Curves over Temperature: $V_G = -0.9\ V$, $P_{IN} = 7\ dBm$

**Gain vs. Frequency**

**Output Power vs. Frequency**

**Drain Current vs. Frequency**

**PAE vs. Frequency**
Power Amplifier, 12 W
8.5 - 11.5 GHz

Typical Pulsed Performance Curves over Temperature at 9 GHz, $V_G = -0.9$ V

**Gain vs. Input Power**

![Gain Graph](image1)

**Output Power vs. Input Power**

![Output Graph](image2)

**Drain Current vs. Input Power**

![Drain Current Graph](image3)

**PAE vs. Input Power**

![PAE Graph](image4)

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DC-0004809
Typical Pulsed Performance Curves over Bias Circuit Voltage

**Gain vs. Frequency**

![Gain vs. Frequency Graph](image)

**Reverse Isolation vs. Frequency**

![Reverse Isolation vs. Frequency Graph](image)

**Input Return Loss vs. Frequency**

![Input Return Loss vs. Frequency Graph](image)

**Output Return Loss vs. Frequency**

![Output Return Loss vs. Frequency Graph](image)
Typical Pulsed Performance Curves over Bias Circuit Voltage: $P_{\text{IN}} = 7$ dBm

**Gain vs. Frequency**

- $V_B = -4.5$ V
- $V_B = -5.0$ V
- $V_B = -5.5$ V
- $V_B = -6.0$ V

**Output Power vs. Frequency**

- $V_B = -4.5$ V
- $V_B = -5.0$ V
- $V_B = -5.5$ V
- $V_B = -6.0$ V

**Drain Current vs. Frequency**

- $V_B = -4.5$ V
- $V_B = -5.0$ V
- $V_B = -5.5$ V
- $V_B = -6.0$ V

**PAE vs. Frequency**

- $V_B = -4.5$ V
- $V_B = -5.0$ V
- $V_B = -5.5$ V
- $V_B = -6.0$ V
Typical Pulsed Performance Curves over Frequency (Bias Circuit Voltage = -5 V)

**Gain vs. Input Power**

![Gain vs. Input Power graph]

**Output Power vs. Input Power**

![Output Power vs. Input Power graph]

**Drain Current vs. Input Power**

![Drain Current vs. Input Power graph]

**PAE vs. Input Power**

![PAE vs. Input Power graph]

**Bias Circuit Current vs. Frequency**

![Bias Circuit Current vs. Frequency graph]
Power Amplifier, 12 W
8.5 - 11.5 GHz

Typical CW Performance Curves over Bias Circuit Voltage: Freq = 9 GHz

**Gain vs. Input Power**

- Gain vs. Input Power graph showing the gain in dB plotted against input power in dBm. The graph includes multiple curves for different bias voltages (VB = -4.5 V, -5.0 V, -5.5 V, -6.0 V).

**Output Power vs. Input Power**

- Output power vs. input power graph showing output power in dBm plotted against input power in dBm. The graph includes multiple curves for different bias voltages (VB = -4.5 V, -5.0 V, -5.5 V, -6.0 V).

**Drain Current vs. Input Power**

- Drain current vs. input power graph showing drain current in mA plotted against input power in dBm. The graph includes multiple curves for different bias voltages (VB = -4.5 V, -5.0 V, -5.5 V, -6.0 V).

**PAE vs. Input Power**

- PAE vs. input power graph showing power added efficiency (%) plotted against input power in dBm. The graph includes multiple curves for different bias voltages (VB = -4.5 V, -5.0 V, -5.5 V, -6.0 V).
Typical CW Performance Curves over Gate Voltage: $V_D = 6$ V

**Gain vs. Frequency**

![Gain vs. Frequency Graph]

**Isolation vs. Frequency**

![Isolation vs. Frequency Graph]

**Input Return Loss vs. Frequency**

![Input Return Loss vs. Frequency Graph]

**Output Return Loss vs. Frequency**

![Output Return Loss vs. Frequency Graph]
Typical CW Performance Curves over Gate Voltage: \( V_D = 6 \) V; Constant \( P_{IN} = 6 \) dBm

- **Gain vs. Frequency**
- **Output Power vs. Frequency**
- **Drain Current vs. Frequency**
- **PAE vs. Frequency**
Typical CW Performance Curves over Frequency: $V_G = -0.9 \text{ V}, V_D = 6 \text{ V}$

- **Gain vs. Input Power**
  - Graph showing gain (dB) vs. input power (dBm) for different frequencies.

- **Output Power vs. Input Power**
  - Graph showing output power (dBm) vs. input power (dBm) for different frequencies.

- **Drain Current vs. Input Power**
  - Graph showing drain current (mA) vs. input power (dBm) for different frequencies.

- **PAE vs. Input Power**
  - Graph showing power added efficiency (PAE) vs. input power (dBm) for different frequencies.

- **Gate Current vs. Input Power**
  - Graph showing gate current (mA) vs. input power (dBm) for different frequencies.
Applications Section

Application Notes

Note 1 - Biasing
The gate bias is applied in one of the following:

1. Direct Gate Bias: \( V_{G1}, V_{G2}, \) & \( V_{G3} \) provide the direct gate bias input to the 3 MMIC stages. This method of biasing allows the user to control the total drain current without the scaling factor provided by the bias circuit. It is recommended that the gate voltage is supplied by both sides of the Die. Optimum performance can be achieved with a -0.9 V operation.

2. Bias Circuit Biasing: Applying -5 V to \( V_{B1}, V_{B2}, \) & \( V_{B3} \) will typically draw 3 A with no further adjustment necessary. Wafer lot variation may result in some devices experiencing higher or lower drain currents than the typical 3 A. It is necessary to connect the Bias Circuit Ground (Pad 2,7,11,21, 25, & 30) to ground in order for this bias circuit to function correctly. It is recommended that the bias circuits on both sides of the PA are used.

Note 2 - Bias Sequence
When switching on the PA, In each case, the gate bias must be applied before the drain voltage is applied. The Drain Voltage \( V_{D1}, V_{D2}, \) & \( V_{D3} \) should be biased from the top and bottom sides of the die.

Note 3 - Decoupling Circuits
Each bias pad, \( V_{G} \) or \( V_{B} \), and \( V_{D} \) must have a decoupling capacitor of 100 pF as close to the device as possible, as is shown in the bonding diagrams. In the case where the bias circuit is used the additional bond wire to ground must be made as short as possible.

Under pulsed operation a large capacitance on the Drain will cause a “ringing” effect on the supply voltage. This potentially produces a high voltage at the PA terminals. A recommended decoupling circuit is provided where shunt decoupling capacitors are connected in series with a resistor to minimize this effect.

Note 4 - Pulse Operation
The performance of the MAAP-015035-DIE is characterized under pulsed conditions with a duty cycle of 5% consisting of a pulse width of 5 µs applied to the drain. Under pulsed conditions the gate is constantly biased using either the on chip bias circuit or using a gate voltage directly applied to the PA. It is recommended that the die is mounted with an adequate thermal solution.

Note 5 - CW Operation
The PA is only recommended for CW operation at reduced drain voltages. With a recommended drain voltage of 6 V, and a direct gate voltage of -0.9 V or using the on chip bias circuit at -5 V.

Note 6 - Input / Output Transitions
The PA performance must be achieved in a 50 Ω impedance environment on the RF input and output. To maintain performance three bond wires are recommended on the output of the PA each with a maximum length of <600 µm. Longer bond wire lengths can be used providing bond pad compensation, in the form of a stub, is used on the application board.
Applications Section

Handling and Assembly

Die Attachment
This product is manufactured from 0.100 mm (0.004") thick substrate and has vias through to the backside to enable grounding to the circuit. Microstrip substrates should be brought as close to the die as possible and bond wire lengths on the input and output kept as short as possible. The mounting surface should be clean and flat. If using conductive epoxy, recommended epoxies are Tanaka TS3332LD, Die Mat DM6030HK or DM6030HK-Pt cured per the manufacturer’s cure schedule. Epoxy should be applied in accordance with the manufacturers specifications and should avoid contact with the top surface of the die. An epoxy fillet should be visible around the total die periphery. For additional information please see the MACOM “Epoxy Specifications for Bare Die” application note. If eutectic mounting is preferred, then a flux-less gold-tin (AuSn) preform, approximately 0.0012 thick, placed between the die and the attachment surface should be used. A die attach bonder that utilizes a heated collet and provides scrubbing action to ensure total wetting to prevent void formation in a nitrogen atmosphere is recommended. The gold-tin eutectic (80% Au 20% Sn) has a melting point of approximately 280ºC (Note: Gold Germanium should be avoided). The work station temperature should be 310ºC +/-10ºC. Exposure time to these extreme temperatures should be kept to minimum. The die and collet should be pre-heated, to avoid excessive thermal shock during assembly. Avoidance of air bridges and force impact are critical during placement.

Wire Bonding
Windows are provided in the surface passivation above the bond pads to allow wire bonding to the die’s gold bond pads. The recommended wire bonding procedure uses 0.076 mm x 0.013 mm (0.003" x 0.0005") 99.99% pure gold ribbon with 0.5 - 2% elongation to minimize RF port bond inductance. Gold 0.025 mm (0.001") diameter wedge or ball bonds are acceptable for DC Bias connections. Aluminium wire should be avoided. Thermo-compression bonding is recommended though thermo-sonic bonding may be used providing the ultrasonic content of the bond is minimized. Bond force, time and ultrasonic's are all critical parameters. Bonds should be made from the bond pads on the die to the package or substrate. All bonds should be as short as possible.

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Application Circuit
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