

## Features

- High Gain: 15 dB
- P1dB: +32 dBm
- P<sub>SAT</sub>: +33 dBm
- OIP3: +37dBm @ +28 dBm/tone output power
- Bias Voltage: V<sub>DD</sub> = +6 V
- Bias Current: I<sub>DQ</sub> = 2000 mA
- Die size: 3.43 x 4.28 x 0.1 mm
- RoHS\* Compliant

## Applications

- Satellite Communications
- 5G FR2
- Short Range, High Throughput Communications

## Description

The MAAP-011443-DIE is a 41 GHz - 46 GHz amplifier with a nominal 15 dB of gain and saturated output power of +33 dBm.

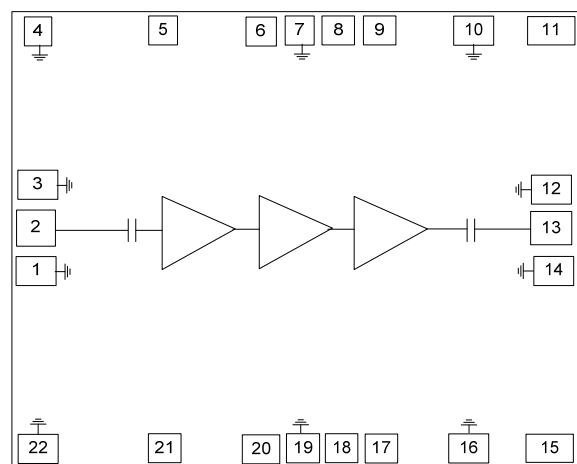
The MAAP-011443-DIE can be used as a final stage amplifier ideally suited for Q-band satellite communication systems as well as 5G systems and short range, high throughput communication links.

This product is fabricated using a GaAs pHEMT process which features full passivation for enhanced reliability.

## Ordering Information

Part Number	Package
MAAP-011443-DIE	Bare die

## Functional Schematic



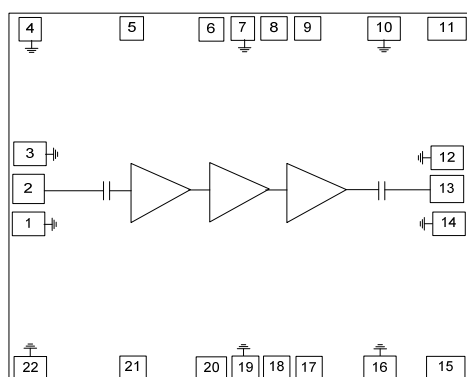
## Pin Configuration<sup>1</sup>

Pad #	Pad Name	Description
1,3,4,7,10,12,14, 16, 19, 22	GND	Ground
2	RF <sub>IN</sub>	RF Input
5, 21	V <sub>G1,2</sub>	Gate Voltage 1, 2
6, 20	V <sub>D1</sub>	Drain Voltage 1
8, 18	V <sub>D2</sub>	Drain Voltage 2
9, 17	V <sub>G3</sub>	Gate Voltage 3
11, 15	V <sub>D3</sub>	Drain Voltage 3
13	RF <sub>OUT</sub>	RF Output

1. The backside of the die must be connected to RF, DC and thermal ground.

\* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

## Functional Schematic



## Pin Description

Pin #	Name	Description
1, 3, 4, 7, 10, 12, 14, 16, 19, 22	GND	These pads are grounded on the MMIC.
2	RF <sub>IN</sub>	RF Signal Input. This pad is matched to 50 $\Omega$ and is AC coupled.
5, 21	VG1, 2	Gate bias for stages 1 and 2 of the amplifier. There is no internal connection between pads 5 and 21 and so both pins need to be externally connected to the same voltage. Adjust $V_G$ from -2 V to 0 V to achieve the desired quiescent current. External bypass capacitors are required as described in the applications schematic
6, 20	VD1	Drain bias for stage 1 of the amplifier. There is no internal connection between pads 6 and 20 and so both pins need to be externally connected to the same voltage. External bypass capacitors are required as described in the applications schematic
8, 18	VD2	Drain bias for stage 2 of the amplifier. There is no internal connection between pads 8 and 18 and so both pins need to be externally connected to the same voltage. External bypass capacitors are required as described in the applications schematic
9, 17	VG3	Gate bias for stage 3 of the amplifier. There is no internal connection between pads 9 and 17 and so both pins need to be externally connected to the same voltage. Adjust $V_G$ from -2 V to 0 V to achieve the desired quiescent current. External bypass capacitors are required as described in the applications schematic
11, 15	VD3	Drain bias for stage 3 of the amplifier. There is no internal connection between pads 11 and 15 and so both pins need to be externally connected to the same voltage. External bypass capacitors are required as described in the applications schematic
13	RF <sub>OUT</sub>	RF Signal Output. This pad is matched to 50 $\Omega$ and is AC coupled

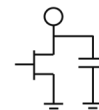
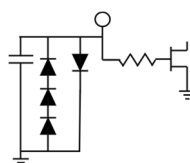
## Interface Schematics

RF<sub>IN</sub>

RF<sub>OUT</sub>

$V_{D1}, V_{D2}, V_{D3}$

$V_{G1, 2}, V_{G3}$



**RF Electrical Specifications: Freq. = 41 - 46 GHz,  $V_D = 6$  V,  $I_{DQ} = 2000$  mA,  $T_A = +25^\circ\text{C}$**

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	$P_{IN} = 0$ dBm 41.0 GHz 43.5 GHz 45.5 GHz 46.0 GHz	dB	8.5 11.0 13.5 —	11.5 14.5 16.5 15.5	—
Input Return Loss	$P_{IN} = -10$ dBm	dB	—	15	—
Output Return Loss	$P_{IN} = -10$ dBm	dB	—	15	—
P1dB	—	dBm	—	32	—
$P_{SAT}$	41.0 GHz, $P_{IN} = 19$ dBm 43.5 GHz, $P_{IN} = 18$ dBm 45.5 GHz, $P_{IN} = 17$ dBm 46.0 GHz, $P_{IN} = 17$ dBm	dBm	31 31 31 —	33 33 33 33	—
OIP3	Tone Spacing = 10 MHz, $P_{OUT} = 28$ dBm/tone	dBm	—	37	—

**DC Electrical Specifications:**

Parameter	Units	Min.	Typ.	Max.
Drain Voltage	V	—	6	—
Gate Voltage	V	—	-0.7	—
Quiescent Drain Current	A	—	2	—
Saturated Drain Current	A	—	2.3	—
Saturated Gate Current	mA	—	4	—

**Maximum Operating Ratings**

Parameter	Rating
Input Power	+25 dBm
Junction Temperature <sup>2,3</sup>	+160°C
Operating Temperature	-40°C to +85°C

2. Operating at nominal conditions with junction temperature  $\leq +160^\circ\text{C}$  will ensure MTTF  $> 1 \times 10^6$  hours.
3. Junction Temperature ( $T_J$ ) =  $T_C + \Theta_{JC} * [(V * I) - (P_{OUT} - P_{IN})]$ .  
Typical thermal resistance ( $\Theta_{JC}$ ) = 5.4 °C/W.
  - a) For  $T_C = +25^\circ\text{C}$  at the backside of the die  
 $T_J = 90^\circ\text{C}$  @ 6 V, 2.34 A  
 $P_{OUT} = 33$  dBm,  $P_{IN} = 22$  dBm, 42 GHz
  - b) For  $T_C = +85^\circ\text{C}$  at the backside of the die  
 $T_J = 154^\circ\text{C}$  @ 6 V, 2.34 A  
 $P_{OUT} = 31$  dBm,  $P_{IN} = 22$  dBm, 42 GHz

**Absolute Maximum Ratings<sup>4,5</sup>**

Parameter	Absolute Maximum
Input Power	+30 dBm
Drain Voltage	6.5 V
Gate Voltage	-3 to 0 V
Junction Temperature <sup>6</sup>	+175°C
Storage Temperature	-65°C to +125°C

4. Exceeding any one or combination of these limits may cause permanent damage to this device.
5. MACOM does not recommend sustained operation near these survivability limits.
6. Junction temperature directly effects device MTTF. Junction temperature should be kept as low as possible to maximize lifetime.

## **Biasing Conditions**

Recommended biasing conditions are  $V_D = 6\text{ V}$ ,  $I_{DQ} = 2000\text{ mA}$  (controlled with  $V_G$ ). The drain bias voltage range is 5 to 6 V, and the quiescent drain current biasing range is 1800 to 2400 mA.

## **Operating the MAAP-011443-DIE**

### **Turn-on**

1. Apply  $V_G$  (-2 V).
2. Apply  $V_D$  (6 V typical).
3. Set  $I_{DQ}$  by adjusting  $V_G$  more positive (typically -0.9 to -0.5V for  $I_{DQ} = 2000\text{ mA}$ ).
4. Apply  $RF_{IN}$  signal.

### **Turn-off**

1. Remove  $RF_{IN}$  signal.
2. Decrease  $V_G$  to -2 V.
3. Decrease  $V_D$  to 0 V.

## **Handling Procedures**

Please observe the following precautions to avoid damage:

### **Static Sensitivity**

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices.

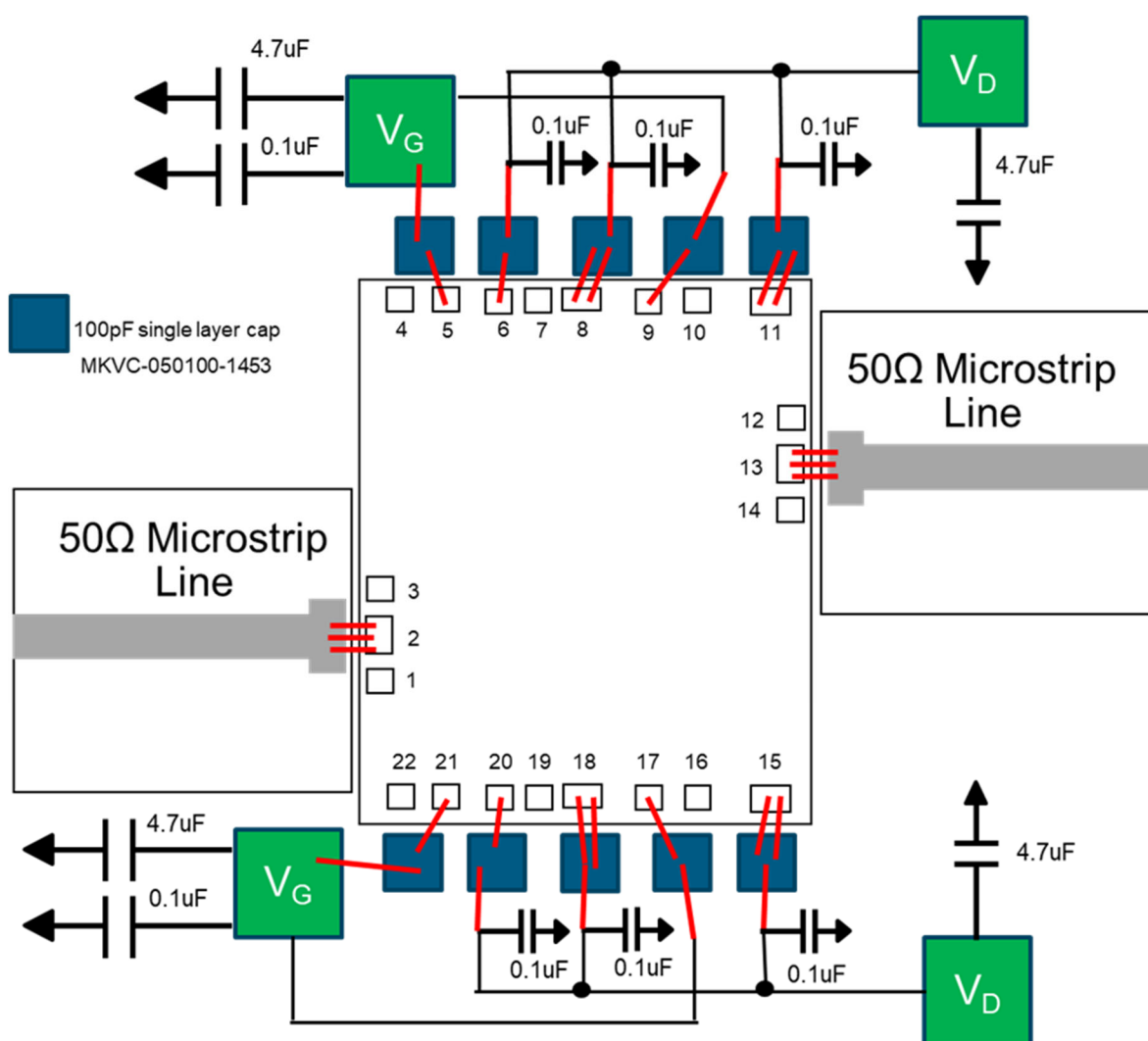
### **Handling the Die**

This MMIC has fragile exposed airbridges on its surface and must be handled on the edges only using a vacuum collet or suitable tweezers. Do not touch the surface of the chip with a vacuum collet, tweezers, or fingers.

### Recommended Bonding Diagram and Application Details:

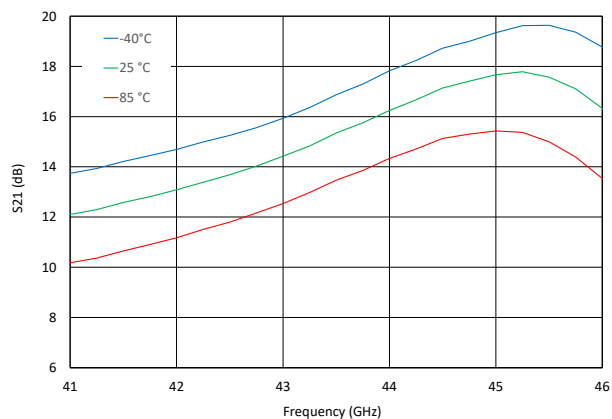
For optimum performance, RF input and output transmission lines require either 3 mil gold ribbon (wedge bond) or 3 x 1 mil diameter gold wire bonds. The gap between the MMIC and the RF input and output lines should be a nominal 3 mil. The RF input and output microstrip lines can be flared in the region of the wirebonds to compensate for them.

In the configuration shown below MACOM MKVC-050100-1453 100 pF chip capacitors are used as part of the drain supply bypassing network. These chip capacitors are to be placed as close to the die as practically possible. The larger 0.1  $\mu$ F capacitor could be implemented using an SMT component on a PCB instead of a chip cap: in this case, proximity to the MMIC die is less important. The circuit is not sensitive to the positioning of the 4.7  $\mu$ F capacitors however these should be on the same PCB as the rest of the biasing components.

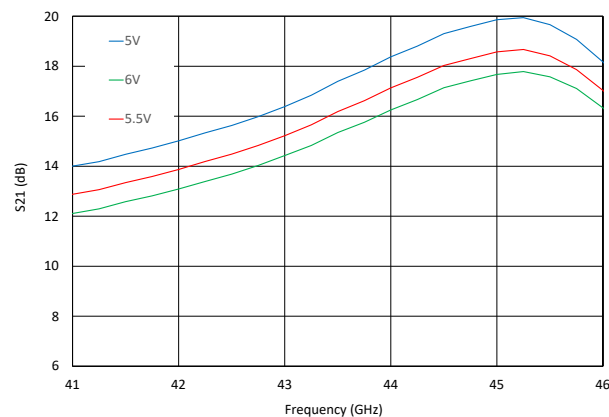


### Typical Performance Curves: $V_D = 6\text{ V}$ , $I_{DQ} = 2000\text{ mA}$

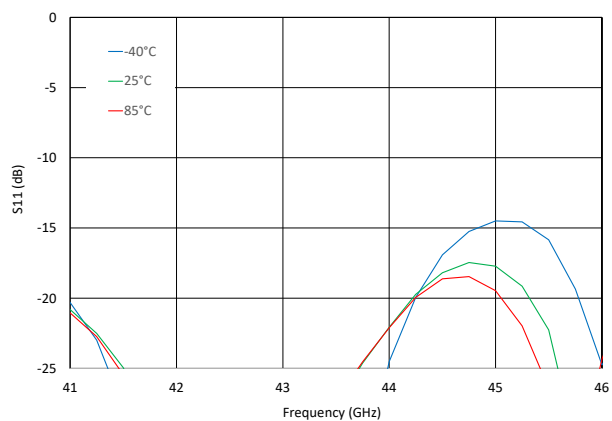
**Small Signal Gain vs. Frequency over Temperature**



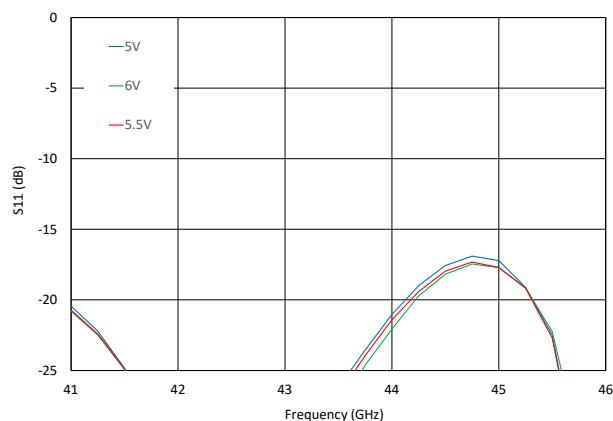
**Small Signal Gain vs. Frequency over Bias Voltage**



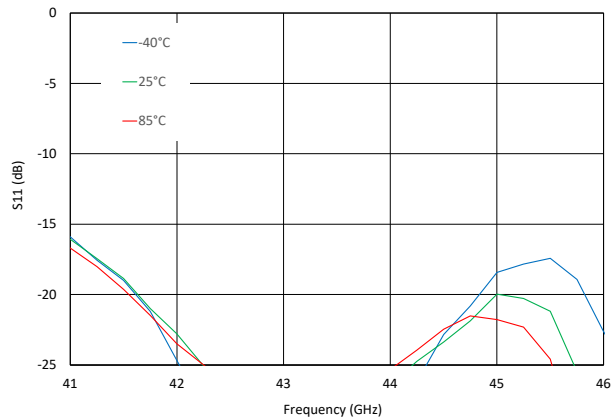
**Input Return Loss vs. Frequency over Temperature**



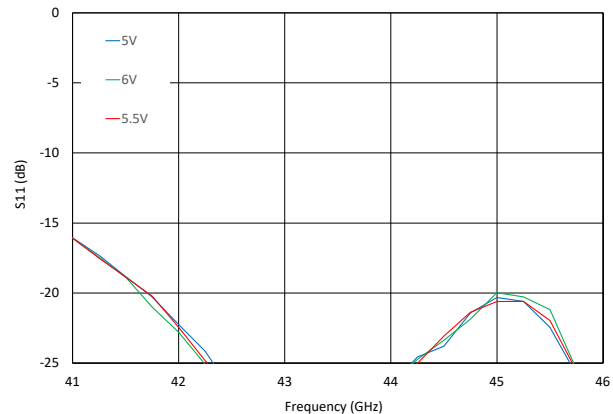
**Input Return Loss vs. Frequency over Bias Voltage**



**Output Return Loss vs. Frequency over Temperature**

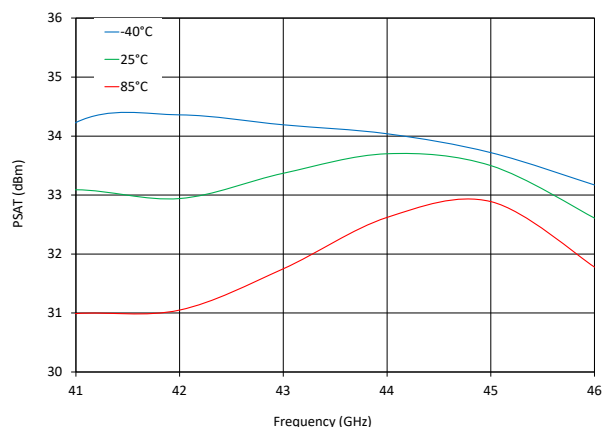


**Output Return Loss vs. Frequency over Bias Voltage**

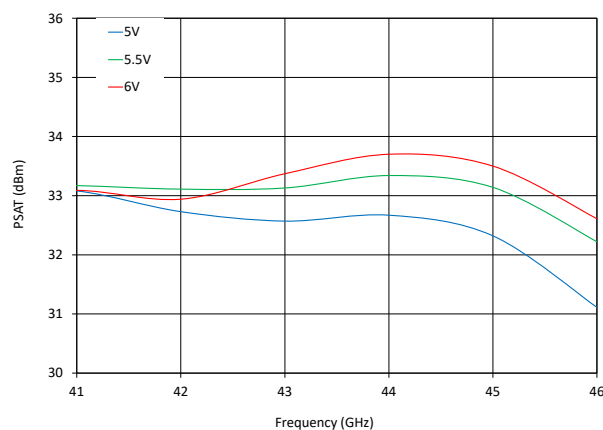


**Typical Performance Curves:  $V_D = 6\text{ V}$ ,  $I_{DQ} = 2000\text{ mA}$**

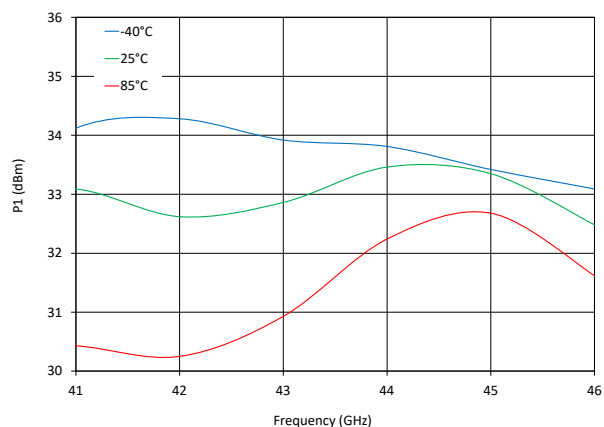
**$P_{SAT}$  vs. Frequency over Temperature**



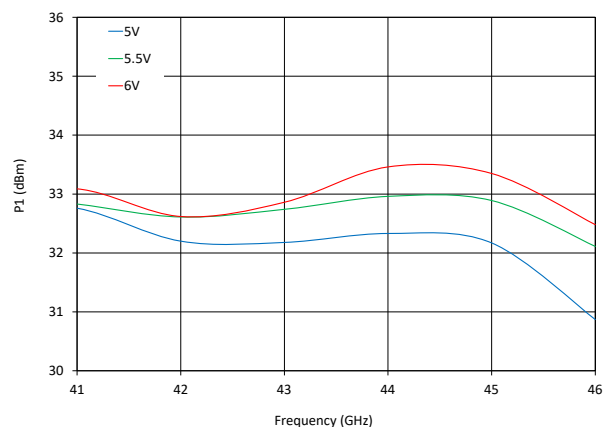
**$P_{SAT}$  vs. Frequency over Bias Voltage**



**$P_{1dB}$  vs. Frequency over Temperature**



**$P_{1dB}$  vs. Frequency over Bias Voltage**



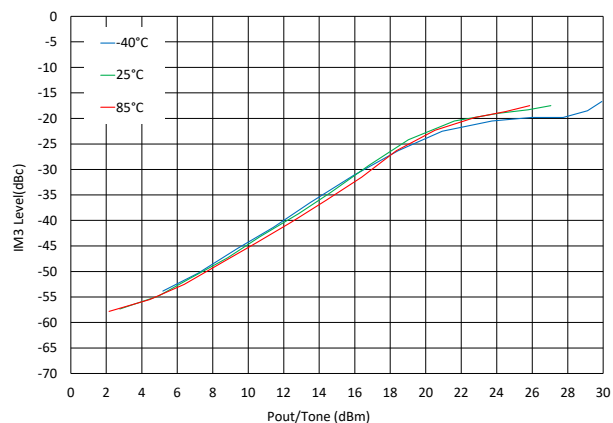
# Power Amplifier, 2 W 41 - 46 GHz



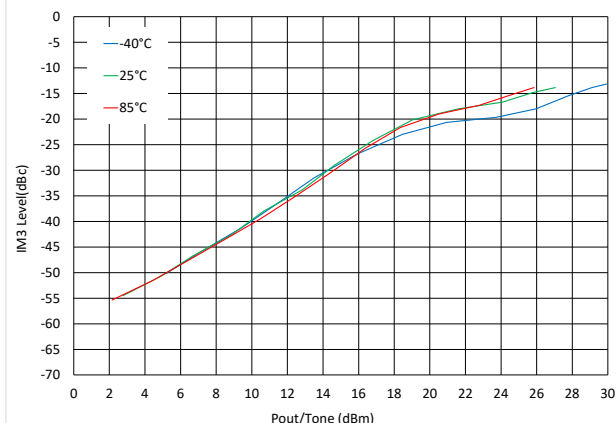
MAAP-011443-DIE  
Rev. V1

## Typical Performance Curves: $V_D = 6\text{ V}$ , $I_{DQ} = 2000\text{ mA}$

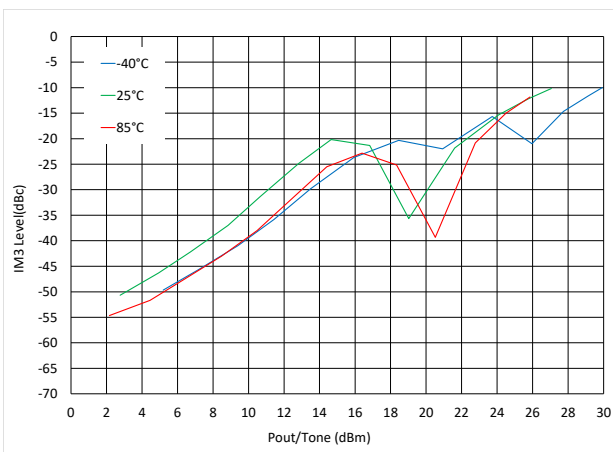
IM3 vs. Output Power (41 GHz) over Temperature



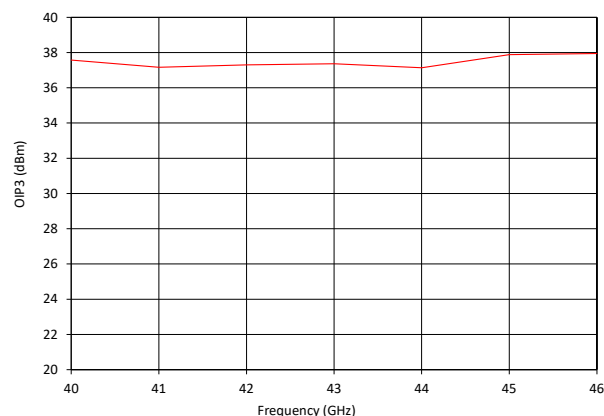
IM3 vs. Output Power (43 GHz) over Temperature



IM3 vs. Output Power (46 GHz) over Temperature



IM3 vs. Frequency @ Output Power = 28 dBm/ton



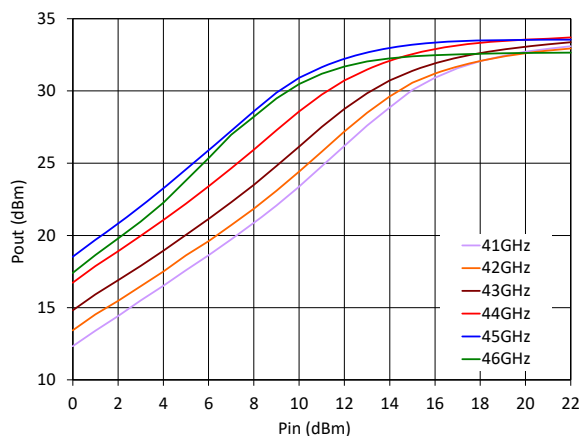
# Power Amplifier, 2 W 41 - 46 GHz



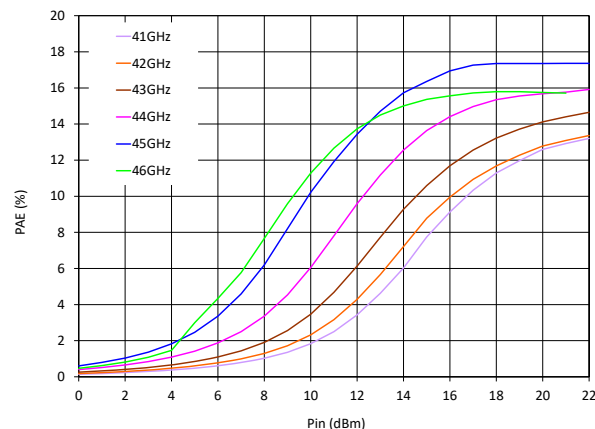
MAAP-011443-DIE  
Rev. V1

Typical Performance Curves:  $V_D = 6\text{ V}$ ,  $I_{DQ} = 2000\text{ mA}$ ,  $25^\circ\text{C}$

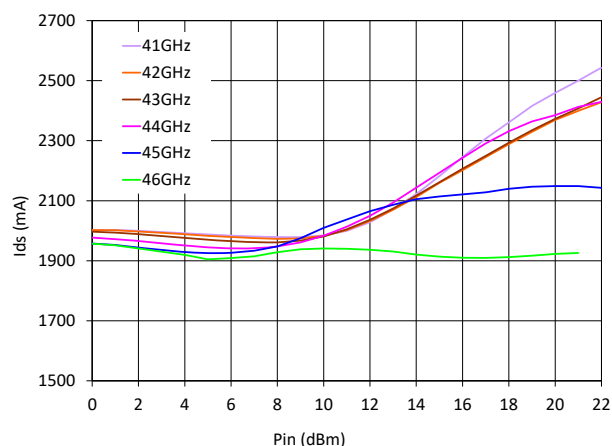
Output Power vs. Input Power over Frequency



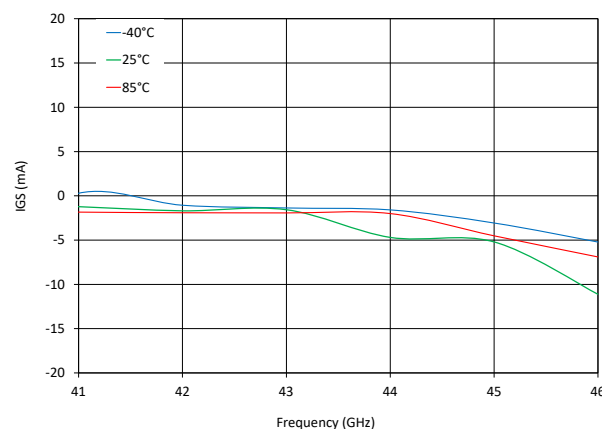
PAE vs. Input Power over Frequency



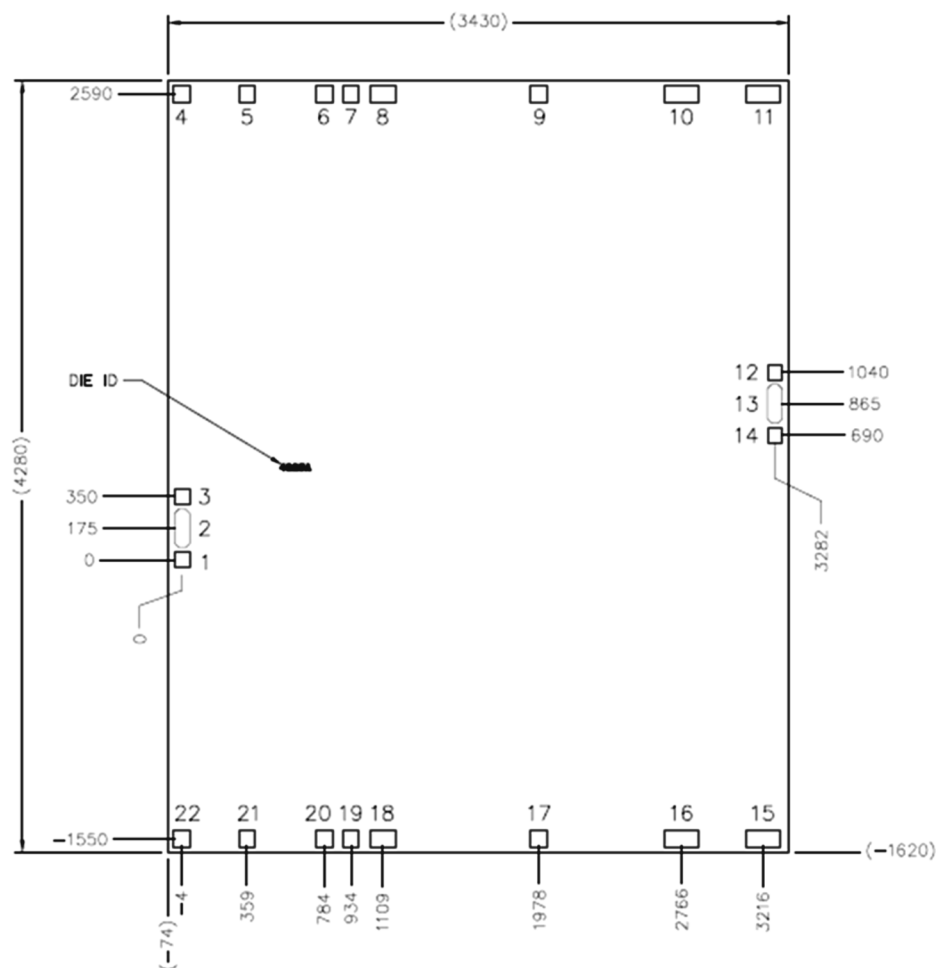
Bias Current vs. Input Power over Frequency



Gate Current @  $P_{SAT}$  over Temperature



## Die Dimensions



BOND PAD DIM. (μm)			
PAD	X	Y	PIN LABEL
1,3,12,14	81	86	GND
2	81	216	RFIN
4,7,19,22	93	93	GND
5,21	93	93	VG1,2
6,20	93	93	VD1
8,18	143	93	VD2
9,17	93	93	VG3
10,16	193	93	GND
11,15	193	93	VD3
13	81	216	RFOUT

Unless otherwise specified, all dimensions shown are μm with a tolerance of ±5 μm.

Die thickness: 100 ±10 μm.

Bond/Pad backside metallization: Gold

Die size reflects final dimensions.

## Revision History

Rev	Date	Change Description
V1	12/19/25	Final Datasheet Released

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