

Rev. V1

Features

High Gain: 22 dB
P1dB: 24 dBm
P_{SAT}: 24.5 dBm
Output IP3: 33 dBm
Bias Voltage: V_{DD} = 5 V
Bias Current: I_{DSQ} = 375 mA
50 Ω Matched Input / Output

- Temperature Compensated Output Power Detector
- Lead-Free 5 mm 12 lead SMT package
- RoHS* Compliant

Applications

• ISM / MM

Description

The MAAP-011377 is a 0.25 W distributed power amplifier offered in a 5 mm SMT package. The power amplifier operates from 20 to 55 GHz and provides 22 dB of linear gain and 24.5 dBm of saturated output power. The device is fully matched across the band and includes a temperature compensated output power detector.

The MAAP-011377 can be used as a power amplifier stage or as a driver stage in higher power applications. This device is ideally suited for test and measurement, 5G FR2, EW, ECM, and radar applications.

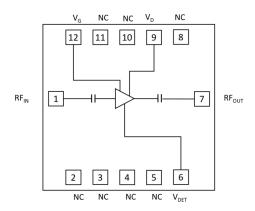
This product is fabricated using a GaAs pHEMT process which features full passivation for enhanced reliability.

Ordering Information^{1,2}

Part Number	Package
MAAP-011377-TR0500	500 Piece Reel
MAAP-011377-SMB	Sample Board

- 1. Reference Application Note M513 for reel size information.
- 2. All sample boards include 3 loose parts.

Functional Schematic



Pin Configuration³

Pad #	Pad Name	Description
1	RFIN	RF Input
2,3,4,5,8,10,11	NC ⁴	Not Internally Connected
6	V_{DET}	Power Detector
7	RFоит	RF Output
9	VD	Drain Voltage
12	VG	Gate Voltage

- 3. Ground paddle must be connected to RF, DC and thermal ground
- It is recommended that these pins are grounded on the application PCB.

^{*} Restrictions on Hazardous Substances, compliant to current RoHS EU directive.



Electrical Specifications: $T_A = +25$ °C, $V_D = 5$ V, $I_{DSQ} = 375$ mA, $Z_0 = 50$ Ω

Parameter	Test Conditions	Units	Min.	Тур.	Max.
Gain	P _{IN} = -5 dBm 20.0 GHz 30.0 GHz 40.0 GHz 48.5 GHz 55.0 GHz	dB	18.5 — — 19.5 —	21.0 19.5 20.0 22.0 20.0	_
Input Return loss	_	dB	_	10	_
Output Return Loss	_	dB	_	10	_
P1dB	20.0 GHz 30.0 GHz 40.0 GHz 48.5 GHz 55.0 GHz	dBm	22.5 — — 22.0 —	24.0 24.0 25.0 24.5 19.0	_
P _{SAT}	20.0 GHz 30.0 GHz 40.0 GHz 48.5 GHz 55.0 GHz	dBm	_	25.0 24.0 24.5 25.0 21.0	_
OIP3	P _{OUT} /Tone = 14 dBm, Δf = 2 MHz	dBm	_	33	_
Drain Current	P _{SAT} , 40 GHz	mA	_	450	_
Power Added Efficiency	P _{SAT} , 40 GHz	%	_	10	_

Maximum Operating Ratings

Parameter	Rating
Input Power	10 dBm
Drain Voltage	5.5 V
Junction Temperature ^{5,6}	+160°C
Operating Temperature	-40°C to +85°C

- 5. Operating at nominal conditions with junction temperature
- \leq +160°C will ensure MTTF > 1 x 10⁶ hours. Junction Temperature (T_J) = T_C + Θ _{JC} * [(V * I) (P_{OUT} P_{IN})]. Typical thermal resistance (Θ _{JC}) = 13°C/W
 - a) For $T_C = +25^{\circ}\text{C}$ at the backside of the die $T_J = 49^{\circ}\text{C}$ @ 5 V, 425 mA, $P_{\text{OUT}} = 24.5$ dBm, $P_{\text{IN}} = 5$ dBm
 - b) For $T_C = +85^{\circ}\text{C}$ at the backside of the die $T_J = 110^{\circ}\text{C}$ @ 5 V, 425 mA, $P_{\text{OUT}} = 23.0 \text{ dBm}$, $P_{\text{IN}} = 5 \text{ dBm}$

Absolute Maximum Ratings^{7,8}

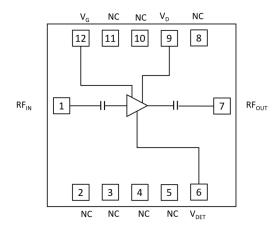
Parameter	Absolute Maximum	
Input Power	17 dBm	
Drain Voltage	6.5 V	
Gate Voltage	-3 to 0 V	
Junction Temperature ⁹	+175°C	
Storage Temperature	-65°C to +125°C	

- 7. Exceeding any one or combination of these limits may cause permanent damage to this device.
- MACOM does not recommend sustained operation near these survivability limits.
- Junction temperature directly effects device MTTF. Junction temperature should be kept as low as possible to maximize lifetime.



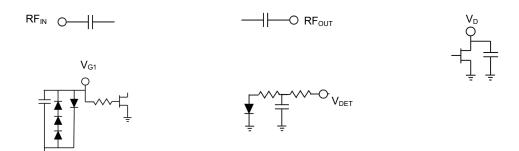
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Pin Configuration and Functional Descriptions



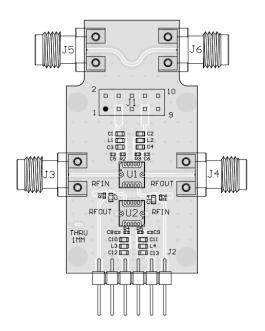
Pin#	Pin Name	Description
1	RF _{IN}	RF Signal Input. This pad is matched to 50 Ω and is AC coupled.
2,3,4,5,8,10,11	NC	These pins are not internally connected (i.e. open circuit). It is recommended that these are connected to ground on the application PCB.
6	V_{DET}	Power detector output voltage. There is an internal 5 k Ω resistor on this pin.
7	RF _{OUT}	RF Signal Output. This pad is matched to 50 Ω and is AC coupled
9	V_D	Drain bias for the amplifier. External bypass capacitors are required as described in the applications schematic.
12		Power amplifier gate control. Adjust VG from -2 V to 0 V to achieve the desired quiescent current. External bypass capacitors are required as described in the applications schematic.

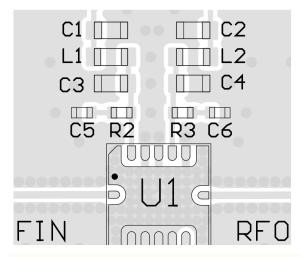
Interface Schematics





Evaluation Board Layout

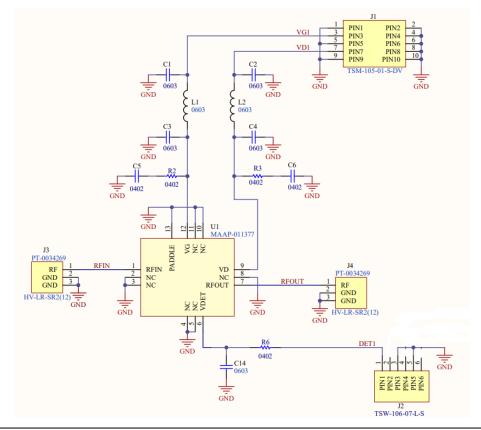




DESIGN NOTES:

RO4003C, 8 MIL THICK, 1/2 COPPER, SOFT GOLD PLATING RF TRACE: 14 MIL WIDTH AND 6.5 MIL SPACING RF PROBE: 8 MIL TRACE WIDTH, 4.5 MIL SPACING EDGE WRAP ON J3, J4, J5, J6.

Evaluation Board Schematic





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Parts List

Part	Value	Case Style
C1, C2	1 µF	0603
C3, C4, C14	0.1 μF	0603
C5, C6	100 pF	0402
R2, R3	10 Ω	0402
R6	0 Ω	0402
L 1, L2	10 nH	0603
R1,R4, R5,C7,C8, C9,C10, C11, C12, C13,L3,L4	DNI	DNI

Evaluation Board Notes

The 100 pF capacitors should be placed as close to the amplifier as practically possible. For the larger 0.1 μ F capacitors proximity to the PA is less important. The circuit is not sensitive to the positioning of the 1 μ F capacitors however these should be on the same PCB as the rest of the biasing components.

The capacitors on the detector output are optional: values will depend on the required response time of the detector output. There is an internal series 5 k Ω resistor on this pin.

To ensure proper grounding the number of ground vias under the device should be maximized (within practical limits imposed by the PCB vendor).

Operating the MAAP-011377

Turn-on

- 1. Apply V_G (-2 V).
- 2. Apply V_D (5.0 V typical).
- 3. Set I_{DQ} by adjusting V_G more positive (typically -0.9 to -1.0 V for I_{DQ} = 375 mA).
- 4. Apply RF_{IN} signal.

Turn-off

- 1. Remove RF_{IN} signal.
- 2. Decrease V_G to -2 V.
- 3. Decrease V_D to 0 V.

Biasing Conditions

Recommended biasing conditions are $V_D = 5$ V, $I_{DQ} = 375$ mA (controlled with V_G). The drain bias voltage range is 4 to 5.5 V, and the quiescent drain current biasing range is 325 to 425 mA.

Handling Procedures

Please observe the following precautions to avoid damage:

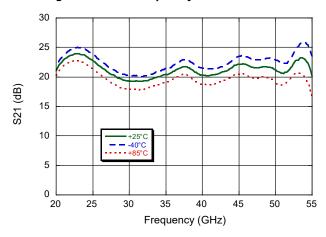
Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices.

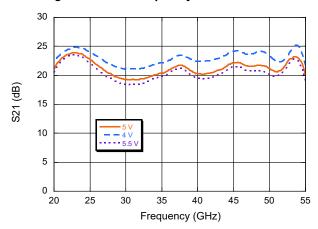


Typical Performance Curves: $V_D = 5 V$, $I_{DSQ} = 375 mA$

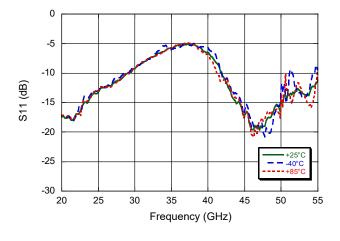
Small Signal Gain vs. Frequency



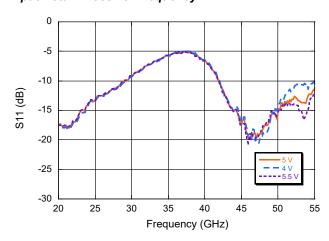
Small Signal Gain vs. Frequency



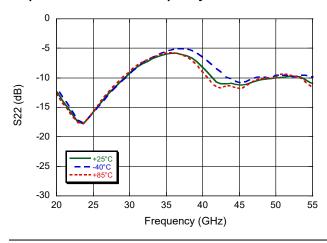
Input Return Loss vs. Frequency



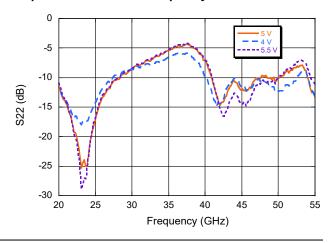
Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



Output Return Loss vs. Frequency



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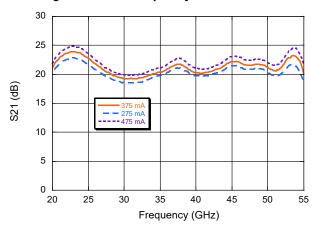
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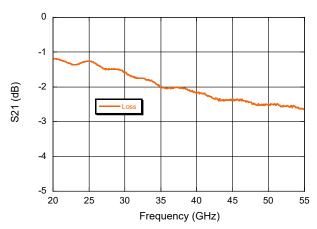


Typical Performance Curves: V_D = 5 V

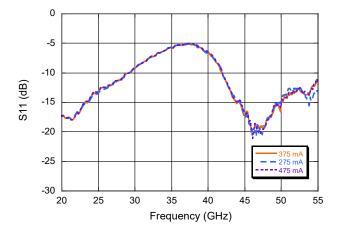
Small Signal Gain vs. Frequency



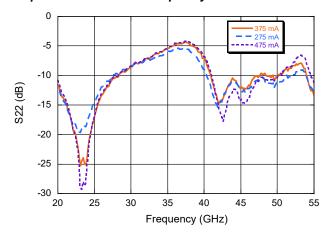
Eval Board Thru Losses



Input Return Loss vs. Frequency



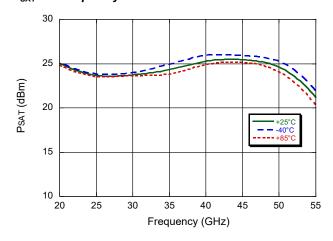
Output Return Loss vs. Frequency



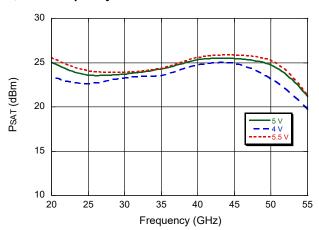


Typical Performance Curves: $V_D = 5 V$, $I_{DSQ} = 375 mA$

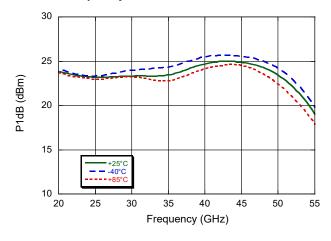
P_{SAT} vs. Frequency



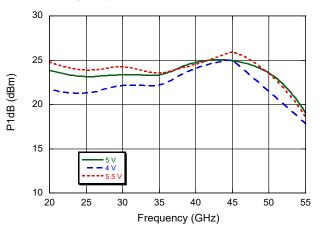
P_{SAT} vs. Frequency



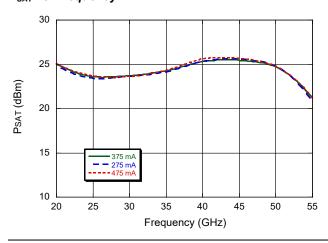
P1dB vs. Frequency



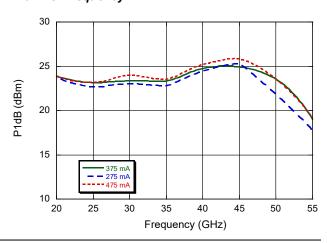
P1dB vs. Frequency



P_{SAT} vs. Frequency



P1dB vs. Frequency



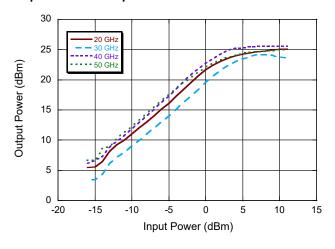
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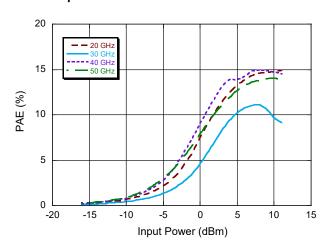


Typical Performance Curves: $V_D = 5 V$, $I_{DSQ} = 375 mA$

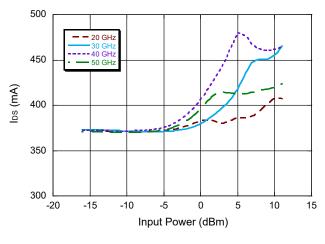
Output Power vs. Input Power



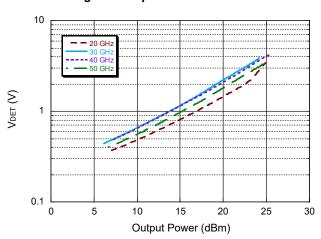
PAE vs. Input Power



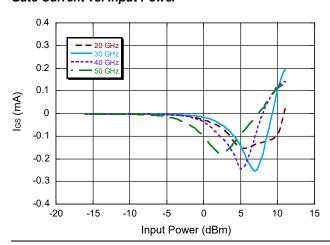
Drain Current vs. Input Power



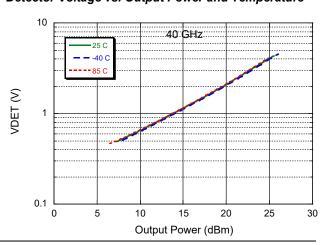
Detector Voltage vs. Output Power



Gate Current vs. Input Power



Detector Voltage vs. Output Power and Temperature



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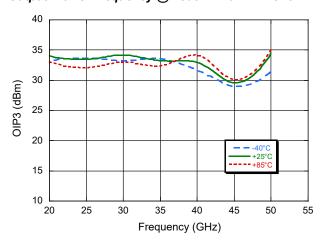
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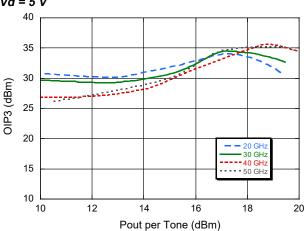
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Typical Performance Curves: V_D = 5 V, I_{DSQ} = 375 mA

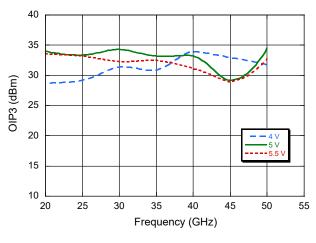
Output IP3 vs. Frequency @ Pout = 17 dBm / Tone



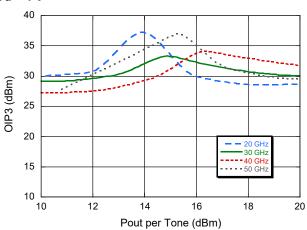
Output IP3 vs. Frequency and Pout per Tone Vd = 5 V



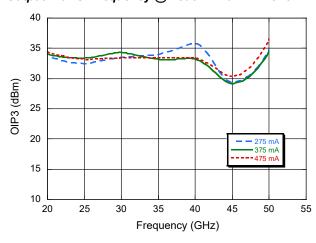
Output IP3 vs. Frequency @ Pout = 17 dBm / Tone



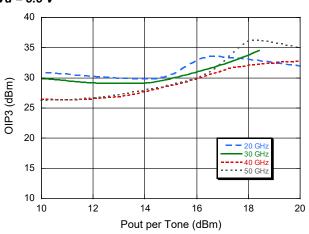
Output IP3 vs. Frequency and Pout per Tone Vd = 4 V



Output IP3 vs. Frequency @ Pout = 17 dBm / Tone



Output IP3 vs. Frequency and Pout per Tone Vd = 5.5 V



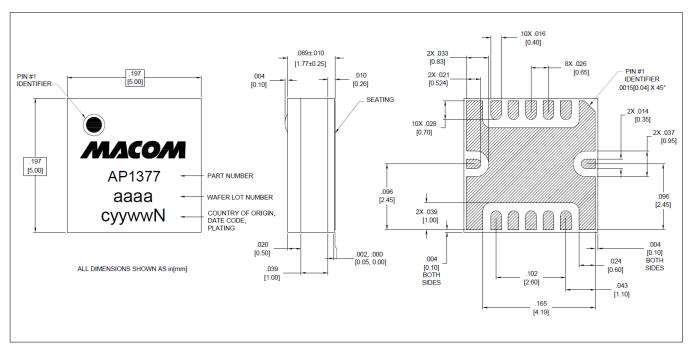
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Lead-Free 5 mm 12-Lead SMT ^{10,11,12,13,14}



- 10. All units in in[mm], unless otherwise noted, with a tolerance of .xxxx = \pm .0005 in and .xxx = \pm .005 in.
- 11. Lead finish: NiPdAu plating
- 12. Marking: line 2 part number; line 3 wafer lot number; line 4 c = country of origin (T = Thailand), yyww = date code, N = Nickel/Palladium/Gold plating
- 13. Reference Application Note S2083 for lead-free solder reflow recommendations.
- 14. Meets JEDEC moisture sensitivity level 3 requirements.

Power Amplifier, 0.25 W 20 - 55 GHz



MAAP-011377

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