Power Amplifier, 2 W
27.5 - 31.5 GHz

Features
- High Gain: 23 dB
- P1dB: 30 dBm
- P_{SAT}: 33 dBm
- IM3 Level: -22 dBC @ P_{OUT} 27 dBm/tone
- Power Added Efficiency: 24% at P_{SAT}
- Lead-Free 5 mm AQFN 32-lead Package
- RoHS* Compliant

Description
The MAAP-011246 is a 2 Watt, 4-stage power amplifier assembled in a lead-free 5 mm 32-lead AQFN plastic package. This power amplifier operates from 27.5 to 31.5 GHz and provides 23 dB of linear gain, 2 W saturated output power and 24% efficiency while biased at 6 V.

The MAAP-011246 can be used as a power amplifier stage or as a driver stage in higher power applications. This device is ideally suited for VSAT and 28 GHz PTP applications.

This product is fabricated using a GaAs pHEMT process which features full passivation for enhanced reliability.

Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAAP-011246-TR0500</td>
<td>500 Piece Reel</td>
</tr>
<tr>
<td>MAAP-011246-1SMB</td>
<td>Sample Board</td>
</tr>
</tbody>
</table>

1. Reference Application Note M513 for reel size information.
2. All sample boards include 3 loose parts.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.
Power Amplifier, 2 W
27.5 - 31.5 GHz

Electrical Specifications:  Freq. = 30 GHz, $T_A = +25^\circ$C, $V_D = 6$ V, $Z_0 = 50$ $\Omega$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Units</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>$P_{IN} = 0$ dBm</td>
<td>dB</td>
<td>19</td>
<td>22</td>
<td>—</td>
</tr>
<tr>
<td>$P_{OUT}$</td>
<td>$P_{IN} = 15$ dBm</td>
<td>dBm</td>
<td>31.5</td>
<td>33</td>
<td>—</td>
</tr>
<tr>
<td>IM3 Level</td>
<td>$P_{OUT} = 27$ dBm / tone</td>
<td>dBc</td>
<td>—</td>
<td>-22</td>
<td>—</td>
</tr>
<tr>
<td>Power Added Efficiency</td>
<td>$P_{SAT} (P_{IN} = 15$ dBm)</td>
<td>%</td>
<td>—</td>
<td>24</td>
<td>—</td>
</tr>
<tr>
<td>Input Return Loss</td>
<td>$P_{IN} = -20$ dBm</td>
<td>dB</td>
<td>—</td>
<td>10</td>
<td>—</td>
</tr>
<tr>
<td>Output Return Loss</td>
<td>$P_{IN} = -20$ dBm</td>
<td>dB</td>
<td>—</td>
<td>14</td>
<td>—</td>
</tr>
<tr>
<td>Quiescent Current</td>
<td>$I_{DO}$ (see bias conditions, page 4)</td>
<td>mA</td>
<td>—</td>
<td>900</td>
<td>—</td>
</tr>
<tr>
<td>Current</td>
<td>$P_{SAT} (P_{IN} = 15$ dBm)</td>
<td>mA</td>
<td>—</td>
<td>1450</td>
<td>—</td>
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</table>

Maximum Operating Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
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</thead>
<tbody>
<tr>
<td>Input Power</td>
<td>15 dBm</td>
</tr>
<tr>
<td>Junction Temperature$^5,6$</td>
<td>+160°C</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-40°C to +85°C</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Power</td>
<td>20 dBm</td>
</tr>
<tr>
<td>Drain Voltage</td>
<td>+6.5 V</td>
</tr>
<tr>
<td>Gate Voltage</td>
<td>-3 to 0 V</td>
</tr>
<tr>
<td>Junction Temperature$^9$</td>
<td>+175°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C to +125°C</td>
</tr>
</tbody>
</table>

5. Operating at nominal conditions with junction temperature ≤ +160°C will ensure MTTF > $1 \times 10^6$ hours.
6. Junction Temperature $(T_J) = T_C + \Theta_{JC} \times ((V \times I) - (P_{OUT} - P_{IN}))$
   Typical thermal resistance $(\Theta_{JC}) = 8^\circ$C/W.
   a) For $T_C = +25^\circ$C, $T_J = +79^\circ$C @ 6 V, 1.45 A, $P_{OUT} = 33.0$ dBm, $P_{IN} = 15$ dBm
   b) For $T_C = +85^\circ$C, $T_J = +136^\circ$C @ 6 V, 1.34 A, $P_{OUT} = 32.4$ dBm, $P_{IN} = 15$ dBm

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices.

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DC-0009231
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Sample Board Layout

Application Schematic

Parts List

<table>
<thead>
<tr>
<th>Part</th>
<th>Value</th>
<th>Case Style</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1 - C6</td>
<td>0.01 µF</td>
<td>0402</td>
</tr>
<tr>
<td>C7 - C10</td>
<td>1 µF</td>
<td>0402</td>
</tr>
<tr>
<td>C11 - C13</td>
<td>10 µF</td>
<td>0603</td>
</tr>
<tr>
<td>R1 - R6</td>
<td>10 Ω</td>
<td>0402</td>
</tr>
<tr>
<td>L1 - L3</td>
<td>600 Ω @ 100 MHz</td>
<td>0603</td>
</tr>
</tbody>
</table>

10. L1 - L3 (chip ferrite bead) supplied from Murata, part number BLM18HE601SN1D.

Sample Board Material Specifications

Top Layer: 1/2 oz Copper Cladding, 0.017 mm thickness
Dielectric Layer: Rogers RO4003C 0.203 mm thickness
Bottom Layer: 1/2 oz Copper Cladding, 0.017 mm thickness
Finished overall thickness: 0.238 mm
**Recommended PCB Layout Detail:**

RF input and output pre-matching circuit patterns are designed to compensate packaging effects. Transmission line dimensions apply to a PCB with 0.203 mm thick Rogers RO4003C laminate dielectric. Performance curves shown in this data sheet were measured with these circuit patterns.

![PCB Layout Diagram](image)

**Biasing Conditions**

Recommended biasing conditions are $V_D = 6 \, \text{V}$, $I_{DQ} = 900 \, \text{mA}$ (controlled with $V_G$). The drain bias voltage range is 3 to 6 V, and the quiescent drain current biasing range is 600 to 1200 mA.

$V_G$ pins 10 and 11 are connected internally; choose either pin for layout convenience. Muting can be accomplished by setting the $V_G$ to the pinched off voltage ($V_G = -2 \, \text{V}$).

$V_D$ bias must be applied to $V_D1$, $V_D2$, $V_D3$, and $V_D4$ pins. $V_D3$ pins 27 and 28 are connected internally: choose either pin for layout convenience. Two $V_D4$ pins 15 and 26 (not connected internally) are required for current symmetry.

**Operating the MAAP-011246**

**Turn-on**
1. Apply $V_G$ (-1.5 V).
2. Apply $V_D$ (6.0 V typical).
3. Set $I_{DQ}$ by adjusting $V_G$ more positive (typically -0.9 to -1.0 V for $I_{DQ} = 900 \, \text{mA}$).
4. Apply RF$_{\text{IN}}$ signal.

**Turn-off**
1. Remove RF$_{\text{IN}}$ signal.
2. Decrease $V_S$ to -1.5 V.
3. Decrease $V_D$ to 0 V.
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Electrical Specifications with the Recommended PCB Layout and bias conditions:
Freq. = 27.5 - 29.5 GHz, \( T_A = +25°C \), \( V_D = 6 \) V, \( Z_0 = 50 \) Ω

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Units</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>( P_{IN} = 0 ) dBm</td>
<td>dB</td>
<td>19</td>
<td>27</td>
<td>30.5</td>
</tr>
<tr>
<td>( P_{SAT} )</td>
<td>dBm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IM3 Level</td>
<td>( P_{OUT} = 27 ) dBm / tone</td>
<td>dBc</td>
<td>—</td>
<td>—</td>
<td>20</td>
</tr>
<tr>
<td>Power Added Efficiency</td>
<td>( P_{SAT} )</td>
<td>%</td>
<td>—</td>
<td>24</td>
<td>—</td>
</tr>
<tr>
<td>Input Return Loss</td>
<td>( P_{IN} = -20 ) dBm</td>
<td>dB</td>
<td>—</td>
<td>15</td>
<td>—</td>
</tr>
<tr>
<td>Output Return Loss</td>
<td>( P_{IN} = -20 ) dBm</td>
<td>dB</td>
<td>—</td>
<td>13</td>
<td>—</td>
</tr>
<tr>
<td>Quiescent Current</td>
<td>( I_{DQ} ) (see bias conditions, page 4 )</td>
<td>mA</td>
<td>—</td>
<td>900</td>
<td>—</td>
</tr>
<tr>
<td>Current</td>
<td>( P_{SAT} )</td>
<td>mA</td>
<td>—</td>
<td>1600</td>
<td>—</td>
</tr>
</tbody>
</table>

Typical Performance Curves

- **Gain vs. Frequency over Temperature**
- **Gain vs. Frequency over Bias Voltage**
- **Input Return Loss vs. Frequency over Temperature**
- **Input Return Loss vs. Frequency over Bias Voltage**

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Typical Performance Curves over Temperature

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**Output Return Loss vs. Frequency over Temperature**

-30 to 0 dB

**Output Return Loss vs. Frequency over Bias Voltage**

-30 to 0 dB

**P1dB Output Power vs. Frequency**

26 to 36 dBm

**PSAT Output Power vs. Frequency**

26 to 36 dBm

**OIP3 vs. Frequency (P_{OUT} = 27 dBm/tone)**

15 to 45 dBm

**IM3 vs. Frequency (P_{OUT} = 27 dBm/tone)**

-45 to -15 dBc
Typical Performance Curves over Bias Voltage

**$P_{1dB}$ Output Power vs. Frequency**

![Diagram showing $P_{1dB}$ output power vs. frequency for different bias voltages.]

**$P_{SAT}$ Output Power vs. Frequency**

![Diagram showing $P_{SAT}$ output power vs. frequency for different bias voltages.]

**OIP3 vs. Frequency ($P_{OUT} = 27 \, dBm/tone$)**

![Diagram showing OIP3 vs. frequency for different bias voltages.]

**IM3 vs. Frequency ($P_{OUT} = 27 \, dBm/tone$)**

![Diagram showing IM3 vs. frequency for different bias voltages.]

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Lead-Free 5 mm AQFN 32-Lead†

Reference Application Note S2083 for lead-free solder reflow recommendations.
Meet JEDEC moisture sensitivity level 3 requirements.
Plating is NiPdAu.
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