Power Amplifier, 4 W
28.5 - 31 GHz

Features
- High Gain: 25 dB @ 30 GHz
- P1dB: 34.5 dBm
- P3dB: 36 dBm
- IM3 Level: -27 dBc @ P_{OUT} 29 dBm/tone
- Power Added Efficiency: 27.5 % at P3dB
- Lead-Free 5 mm 32-lead AQFN Package
- RoHS* Compliant

Description
The MAAP-011233 is a 4-stage, 4 W power amplifier assembled in a lead-free 5 mm 32-lead AQFN plastic package. This power amplifier operates from 28.5 to 31 GHz and provides 26 dB of linear gain, 4 W saturated output power and 27.5 % efficiency while biased at 6 V.

The MAAP-011233 can be used as a power amplifier ideally suited for VSAT communications.

This product is fabricated using a GaAs pHEMT process which features full passivation for enhanced reliability.

Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAAP-011233</td>
<td>Bulk</td>
</tr>
<tr>
<td>MAAP-011233-TR0500</td>
<td>500 Piece Reel</td>
</tr>
<tr>
<td>MAAP-011233-SMB</td>
<td>Sample Board</td>
</tr>
</tbody>
</table>

1. Reference Application Note M513 for reel size information.
2. All sample boards include 3 loose parts.
3. MACOM recommends connecting all No Connection (N/C) pins to ground.
4. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

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Electrical Specifications: Freq. = 30 GHz, \( T_A = +25^\circ C \), \( V_D = 6 \, V \), \( Z_0 = 50 \, \Omega \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Units</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>( P_{IN} = 0 , dBm )</td>
<td>dB</td>
<td>22</td>
<td>25.0</td>
<td>—</td>
</tr>
<tr>
<td>( P_{OUT} )</td>
<td>( P_{IN} = +14 , dBm )</td>
<td>dBm</td>
<td>34.5</td>
<td>36.0</td>
<td>—</td>
</tr>
<tr>
<td>IM3 Level</td>
<td>( P_{OUT} = 29 , dBm / \text{tone} )</td>
<td>dBC</td>
<td>—</td>
<td>-27.0</td>
<td>—</td>
</tr>
<tr>
<td>Power Added Efficiency</td>
<td>( P_{IN} = +14 , dBm )</td>
<td>%</td>
<td>—</td>
<td>27.5</td>
<td>—</td>
</tr>
<tr>
<td>Input Return Loss</td>
<td>( P_{IN} = -20 , dBm )</td>
<td>dB</td>
<td>—</td>
<td>10</td>
<td>—</td>
</tr>
<tr>
<td>Output Return Loss</td>
<td>( P_{IN} = -20 , dBm )</td>
<td>dB</td>
<td>—</td>
<td>10</td>
<td>—</td>
</tr>
<tr>
<td>Quiescent Current</td>
<td>( I_{DO} ) (see bias conditions, page 4)</td>
<td>mA</td>
<td>—</td>
<td>2000</td>
<td>—</td>
</tr>
<tr>
<td>Current</td>
<td>( P_{IN} = +14 , dBm )</td>
<td>mA</td>
<td>—</td>
<td>2800</td>
<td>3600</td>
</tr>
</tbody>
</table>

Maximum Operating Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
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</thead>
<tbody>
<tr>
<td>Input Power</td>
<td>14 dBm</td>
</tr>
<tr>
<td>Junction Temperature(^5,6)</td>
<td>+160°C</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-40°C to +85°C</td>
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</tbody>
</table>

Absolute Maximum Ratings\(^7,8\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Absolute Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Power</td>
<td>20 dBm</td>
</tr>
<tr>
<td>Drain Voltage</td>
<td>6.5 V</td>
</tr>
<tr>
<td>Gate Voltage</td>
<td>-3 to 0 V</td>
</tr>
<tr>
<td>Junction Temperature(^8)</td>
<td>+175°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C to +125°C</td>
</tr>
</tbody>
</table>

5. Operating at nominal conditions with junction temperature \( \leq +160°C \) will ensure MTTF > 1 x 10⁶ hours.
6. Junction Temperature (\( T_j \)) = \( T_C + \Theta_{JC} \times ([V \times I] - [P_{OUT} - P_{IN}]) \).
   Typical thermal resistance (\( \Theta_{JC} \)) = 4.4 °C/W.
   a) For \( T_C = +25°C \), \( T_j = +82°C \) @ 6 V, 2.8 A, \( P_{OUT} = 36 \, dBm \), \( P_{IN} = 14 \, dBm \)
   b) For \( T_C = +85°C \), \( T_j = +137°C \) @ 6 V, 2.5 A, \( P_{OUT} = 35 \, dBm \), \( P_{IN} = 14 \, dBm \)

Handling Procedures
Please observe the following precautions to avoid damage:

Static Sensitivity
These electronics devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices.

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Sample Board Layout

Application Schematic

Parts List

<table>
<thead>
<tr>
<th>Part</th>
<th>Value</th>
<th>Case Style</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1 - C7</td>
<td>0.01 µF</td>
<td>0402</td>
</tr>
<tr>
<td>C8 - C12</td>
<td>1 µF</td>
<td>0603</td>
</tr>
<tr>
<td>C13 - C16</td>
<td>10 µF</td>
<td>0805</td>
</tr>
<tr>
<td>R1 - R7</td>
<td>10 Ω</td>
<td>0402</td>
</tr>
<tr>
<td>L1 - L4</td>
<td>BLM18HE601SN1D</td>
<td>0603</td>
</tr>
</tbody>
</table>

Sample Board Material Specifications

Top Layer: 1/2 oz Copper Cladding, 0.017 mm thickness
Dielectric Layer: Rogers RO4003C 0.203 mm thickness
Bottom Layer: 1/2 oz Copper Cladding, 0.017 mm thickness
Finished overall thickness: 0.238 mm
Sample Board Layout:
RF input and output port pre-matching circuit patterns are designed to compensate for packaging effects. Input and output patterns are identical.

Biasing Conditions
Recommended biasing conditions are $V_D = 6 \text{ V}$, $I_{DO} = 2 \text{ A}$ (controlled with $V_G$). The drain bias voltage range is 3 to 6 V, and the quiescent drain current biasing range is 1.5 to 2.5 A.

$V_G$ pins 10 and 11 are connected internally; choose either pin for layout convenience. Muting can be accomplished by setting the $V_G$ to the pinched off voltage ($V_G = -2 \text{ V}$).

$V_D$ bias must be applied to $V_D1$, $V_D2$, $V_D3$, and $V_D4$ pins.

$V_D3$ pins 14 and either pin 27 or 28 are required for current symmetry. Pins 27 and 28 are connected internally; choose either pin for layout convenience.

Both $V_D4$ pins 15 and 26 are required for current symmetry.

Operating the MAAP-011233

**Turn-on**
1. Apply $V_G (-1.5 \text{ V})$.
2. Apply $V_{D1}$, $V_{D2}$, $V_{D3}$, $V_{D4}$ (6.0 V typical).
3. Set $I_{DO}$ by adjusting $V_G$ more positive (typically -0.9 to -1.0 V for $I_{DO} = 2 \text{ A}$).
4. Apply $RF_{IN}$ signal.

**Turn-off**
1. Remove $RF_{IN}$ signal.
2. Decrease $V_G$ to -1.5 V.
3. Decrease $V_{D1}$, $V_{D2}$, $V_{D3}$, $V_{D4}$ to 0 V.

Application Information
The MAAP-011233 is designed to be easy to use yet high performance. The ultra small size and simple bias allow easy placement on system board. RF input and output ports are DC de-coupled internally.
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Typical Performance Curves

**Small Signal Gain vs. Frequency over Temperature**

**Small Signal Gain vs. Frequency over Bias Voltage**

**Input Return Loss vs. Frequency over Temperature**

**Input Return Loss vs. Frequency over Bias Voltage**

**Output Return Loss vs. Frequency over Temperature**

**Output Return Loss vs. Frequency over Bias Voltage**
Typical Performance Curves

**P3dB vs. Frequency over Temperature**

![Graph showing P3dB vs. Frequency over Temperature](image)

**P3dB vs. Frequency over Bias Voltage**

![Graph showing P3dB vs. Frequency over Bias Voltage](image)

**P1dB vs. Frequency over Temperature**

![Graph showing P1dB vs. Frequency over Temperature](image)

**P1dB vs. Frequency over Bias Voltage**

![Graph showing P1dB vs. Frequency over Bias Voltage](image)
Typical Performance Curves: $P_{\text{OUT}} = 29$ dBm / Tone

**Output IP3 vs. Frequency over Temperature**

![Graph showing Output IP3 vs. Frequency over Temperature](image)

**Output IP3 vs. Frequency over Bias Voltage**

![Graph showing Output IP3 vs. Frequency over Bias Voltage](image)

**IM3 vs. Frequency over Temperature**

![Graph showing IM3 vs. Frequency over Temperature](image)

**IM3 vs. Frequency over Bias Voltage**

![Graph showing IM3 vs. Frequency over Bias Voltage](image)
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Typical Performance Curves

**P1dB & P3dB vs. Frequency**

![P1dB & P3dB vs. Frequency graph]

**PAE & Gain @ P3dB vs. Frequency**

![PAE & Gain @ P3dB vs. Frequency graph]

**IM3 vs. Output Power**

![IM3 vs. Output Power graph]

**Output IP3 vs. Output Power**

![Output IP3 vs. Output Power graph]
Typical Performance Curves

**Output Power vs. Input Power**

![Output Power vs. Input Power graph](image)

**PAE vs. Input Power**

![PAE vs. Input Power graph](image)

**Bias Current vs. Input Power**

![Bias Current vs. Input Power graph](image)

**Quiescent Drain Current vs. Temperature**

![Quiescent Drain Current vs. Temperature graph](image)
Lead-Free 5 mm 32-Lead AQFN Package†

Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 3 requirements.
Plating is NiPdAu.