Features
- 4 Stage Power Amplifier for E-Band
- 20 dB Gain
- 8 dB Input and Output Match
- 27 dBm Saturated Output Power
- 31 dBm OIP3
- Variable Gain with Adjustable Bias
- Integrated Detector
- 2790 × 1950 × 50 µm Bare Die
- RoHS* Compliant

Description
The MAAP-011218 is a bare die power amplifier that operates from 71 - 86 GHz. The amplifier provides 20 dB small signal gain, 27 dBm output power and 31 dBm Output Third Order Intercept Point (OIP3). An integrated temperature compensated power detector is on-chip. The input and output are matched to 50 Ω with bond wires to external board.

This amplifier is designed for use as a power amplifier stage in transmit chains and is ideally suited for E-band point-to-point radios. Each device is 100% RF tested to ensure performance compliance.

Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAAP-011218-DIE</td>
<td>Vacuum Release Gel Pak¹</td>
</tr>
</tbody>
</table>

¹ Die quantity varies.

2. These pads are internally connected to ground.
3. The backside of the die must be connected to RF, DC and thermal ground.

0.5 W Power Amplifier
71 - 86 GHz

Electrical Specifications:
Freq. = 71 - 76 GHz, $T_A = 25°C$, $V_D = 4$ V, $I_{DQ} = 760$ mA (Full Bias), $Z_0 = 50$ Ω

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Units</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
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<tr>
<td>Gain</td>
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<tr>
<td>Output Return Loss</td>
<td>—</td>
<td>dB</td>
<td>—</td>
<td>7</td>
<td>—</td>
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<tr>
<td>Noise Figure</td>
<td>—</td>
<td>dB</td>
<td>—</td>
<td>7</td>
<td>—</td>
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<tr>
<td>OIP3</td>
<td>$P_{IN} = -5$ dBm/tone, 11 MHz Tone Spacing</td>
<td>dBm</td>
<td>—</td>
<td>32</td>
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<tr>
<td>Output P1dB</td>
<td>—</td>
<td>dBm</td>
<td>—</td>
<td>26</td>
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<tr>
<td>$P_{SAT}$</td>
<td>—</td>
<td>dBm</td>
<td>25</td>
<td>28</td>
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<tr>
<td>Efficiency</td>
<td>@ P1dB @ $P_{SAT}$</td>
<td>%</td>
<td>—</td>
<td>12</td>
<td>15</td>
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Electrical Specifications:
Freq. = 81 - 86 GHz, $T_A = 25°C$, $V_D = 4$ V, $I_{DQ} = 760$ mA (Full Bias), $Z_0 = 50$ Ω

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Units</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
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<td>17</td>
<td>—</td>
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<tr>
<td>Input Return Loss</td>
<td>—</td>
<td>dB</td>
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<td>5</td>
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<tr>
<td>Output Return Loss</td>
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<td>dB</td>
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<td>10</td>
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<tr>
<td>Noise Figure</td>
<td>—</td>
<td>dB</td>
<td>—</td>
<td>7</td>
<td>—</td>
</tr>
<tr>
<td>OIP3</td>
<td>$P_{IN} = -5$ dBm/tone, 11 MHz Tone Spacing</td>
<td>dBm</td>
<td>—</td>
<td>31</td>
<td>—</td>
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<tr>
<td>Output P1dB</td>
<td>—</td>
<td>dBm</td>
<td>—</td>
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<td>—</td>
</tr>
<tr>
<td>$P_{SAT}$</td>
<td>—</td>
<td>dBm</td>
<td>25</td>
<td>26</td>
<td>—</td>
</tr>
<tr>
<td>Efficiency</td>
<td>@ P1dB @ $P_{SAT}$</td>
<td>%</td>
<td>—</td>
<td>6</td>
<td>9</td>
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Electrical Specifications:
Freq. = 71 - 76 GHz, $T_A = 25^\circ$C, $V_D = 4$ V, $I_{DQ} = 460$ mA (Reduced Bias), $Z_0 = 50$ Ω

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Units</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
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<td>—</td>
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<tr>
<td>Input Return Loss</td>
<td>—</td>
<td>dB</td>
<td>—</td>
<td>8</td>
<td>—</td>
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<tr>
<td>Output Return Loss</td>
<td>—</td>
<td>dB</td>
<td>—</td>
<td>6</td>
<td>—</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>—</td>
<td>dB</td>
<td>—</td>
<td>7</td>
<td>—</td>
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<tr>
<td>OIP3</td>
<td>$P_{IN} = -5$ dBm/tone, 11 MHz Tone Spacing</td>
<td>dBm</td>
<td>—</td>
<td>29</td>
<td>—</td>
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<tr>
<td>Output P1dB</td>
<td>—</td>
<td>dBm</td>
<td>—</td>
<td>26</td>
<td>—</td>
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<tr>
<td>$P_{SAT}$</td>
<td>—</td>
<td>dBm</td>
<td>—</td>
<td>27</td>
<td>—</td>
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<tr>
<td>Efficiency</td>
<td>@ P1dB @ $P_{SAT}$</td>
<td>%</td>
<td>—</td>
<td>9</td>
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Electrical Specifications:
Freq. = 81 - 86 GHz, $T_A = 25^\circ$C, $V_D = 4$ V, $I_{DQ} = 460$ mA (Reduced Bias), $Z_0 = 50$ Ω

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Units</th>
<th>Min.</th>
<th>Typ.</th>
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<td>5</td>
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<tr>
<td>Output Return Loss</td>
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<td>dB</td>
<td>—</td>
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<tr>
<td>Noise Figure</td>
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<td>dB</td>
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<td>7</td>
<td>—</td>
</tr>
<tr>
<td>OIP3</td>
<td>$P_{IN} = -5$ dBm/tone, 11 MHz Tone Spacing</td>
<td>dBm</td>
<td>—</td>
<td>29</td>
<td>—</td>
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<tr>
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<td>dBm</td>
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<tr>
<td>Efficiency</td>
<td>@ P1dB @ $P_{SAT}$</td>
<td>%</td>
<td>—</td>
<td>6</td>
<td>9</td>
</tr>
</tbody>
</table>
0.5 W Power Amplifier
71 - 86 GHz

Recommended Quiescent Bias Currents, All Drain Supply Voltages are +4 V

<table>
<thead>
<tr>
<th>Bias</th>
<th>I_D1 mA</th>
<th>I_D2 mA</th>
<th>I_D3 mA</th>
<th>I_D4 mA</th>
<th>Total mA</th>
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</thead>
<tbody>
<tr>
<td>Full Bias</td>
<td>120</td>
<td>120</td>
<td>200</td>
<td>320</td>
<td>760</td>
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<tr>
<td>Reduced Bias</td>
<td>70</td>
<td>70</td>
<td>120</td>
<td>200</td>
<td>460</td>
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Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Absolute Maximum</th>
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<tr>
<td>Drain Voltage</td>
<td>+4.3 V</td>
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<tr>
<td>Gate Bias Voltage</td>
<td>-1.5 V &lt; V_G &lt; +0.3 V</td>
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<tr>
<td>Drain Current</td>
<td>1135 mA</td>
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<tr>
<td>Input Power</td>
<td>20 dBm</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>+150°C</td>
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<tr>
<td>Operating Temperature</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-55°C to +150°C</td>
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</table>

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These Class 1B electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

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8. All units in the outline drawing are microns, with a tolerance of ± 5 µm, except for die exterior dimensions which are street-centre-to-centre minus the nominal kerf, ± 20 µm tolerance.
9. Die Thickness is 50 ± 10 µm.

**Bond Pad Opening Detail**

<table>
<thead>
<tr>
<th>Pad</th>
<th>Size (x) µm</th>
<th>Size (y) µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>B, L</td>
<td>65</td>
<td>157</td>
</tr>
<tr>
<td>D, E, F, G, I, J, O, P, Q</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>H, N</td>
<td>250</td>
<td>100</td>
</tr>
<tr>
<td>A, C, K, M</td>
<td>100</td>
<td>80</td>
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</tbody>
</table>
Typical Performance Curves: \( I_{DG} = 760 \, mA, \, V_D = 4 \, V, \, \text{Full Bias} \)

**S21**

![Graph of S21](image)

**S12**

![Graph of S12](image)

**S11**

![Graph of S11](image)

**S22**

![Graph of S22](image)
Typical Performance Curves: \( I_{DQ} = 760 \text{ mA}, V_D = 4 \text{ V}, \) Full Bias

**S21 (Wideband)**

![S21 (Wideband) Graph]

**S12 (Wideband)**

![S12 (Wideband) Graph]

**S11 (Wideband)**

![S11 (Wideband) Graph]

**S22 (Wideband)**

![S22 (Wideband) Graph]
Typical Performance Curves: $I_{DG} = 460$ mA, $V_D = 4$ V, Reduced Bias

$S_{21}$

$S_{11}$

$S_{22}$

$S_{12}$
Typical Performance Curves: $V_D = 4$ V

*Total Drain currents were set at 80, 150, 230, 300, 380, 460, 530, 610, 680, 760, 840, 910, and 980 mA.
Typical Performance Curves: $I_{DQ} = 760 \text{ mA}, V_D = 4 \text{ V (Full Bias)}$

**Saturated Power and PAE**

- PSAT @ +25°C
- PSAT @ +85°C
- PAE @ PSAT @ +25°C
- PAE @ PSAT @ +85°C

**Output P1dB**

- P1dB @ +25°C
- P1dB @ +85°C

**Gain and PAE vs. $P_{\text{OUT}}$ at 71GHz**

- Gain @ 71GHz @ +25°C
- Gain @ 71GHz @ +85°C
- PAE @ 71GHz @ +25°C
- PAE @ 71GHz @ +85°C

**Gain and PAE vs. $P_{\text{OUT}}$ at 76GHz**

- Gain @ 76GHz @ +25°C
- Gain @ 76GHz @ +85°C
- PAE @ 76GHz @ +25°C
- PAE @ 76GHz @ +85°C

**Gain and PAE vs. $P_{\text{OUT}}$ at 81GHz**

- Gain @ 81GHz @ +25°C
- Gain @ 81GHz @ +85°C
- PAE @ 81GHz @ +25°C
- PAE @ 81GHz @ +85°C

**Gain and PAE vs. $P_{\text{OUT}}$ at 86GHz**

- Gain @ 86GHz @ +25°C
- Gain @ 86GHz @ +85°C
- PAE @ 86GHz @ +25°C
- PAE @ 86GHz @ +85°C
Typical Performance Curves: $I_{DQ} = 460$ mA, $V_D = 4$ V (Reduced Bias)

**Saturated Power and PAE**

- **Frequency (GHz)**
- **PSAT (dBm) & PAE (%)**
- **PSAT @ +25ºC**
- **PSAT @ +85ºC**
- **PAE @ PSAT @ +25ºC**
- **PAE @ PSAT @ +85ºC**

**Output P1dB**

- **Frequency (GHz)**
- **P1dB (dBm)**
- **P1dB @ +25ºC**
- **P1dB @ +85ºC**

**Gain and PAE vs. $P_{OUT}$ at 71GHz**

- **Gain (dB) and PAE (%)**
- **Gain @ 71GHz @ +25ºC**
- **Gain @ 71GHz @ +85ºC**
- **PAE @ 71GHz @ +25ºC**
- **PAE @ 71GHz @ +85ºC**

**Gain and PAE vs. $P_{OUT}$ at 76GHz**

- **Gain (dB) and PAE (%)**
- **Gain @ 76GHz @ +25ºC**
- **Gain @ 76GHz @ +85ºC**
- **PAE @ 76GHz @ +25ºC**
- **PAE @ 76GHz @ +85ºC**

**Gain and PAE vs. $P_{OUT}$ at 81GHz**

- **Gain (dB) and PAE (%)**
- **Gain @ 81GHz @ +25ºC**
- **Gain @ 81GHz @ +85ºC**
- **PAE @ 81GHz @ +25ºC**
- **PAE @ 81GHz @ +85ºC**

**Gain and PAE vs. $P_{OUT}$ at 86GHz**

- **Gain (dB) and PAE (%)**
- **Gain @ 86GHz @ +25ºC**
- **Gain @ 86GHz @ +85ºC**
- **PAE @ 86GHz @ +25ºC**
- **PAE @ 86GHz @ +85ºC**
Typical Performance Curves: \( I_{\text{DQ}} = 760 \, \text{mA}, \, V_D = 4 \, \text{V}, \, \text{Full Bias}, \, \text{RF P} \text{IN} = -5 \, \text{dBm/tone} \)

Typical Performance Curves: \( I_{\text{DQ}} = 460 \, \text{mA}, \, V_D = 4 \, \text{V}, \, \text{Reduced Bias}, \, \text{RF P} \text{IN} = -5 \, \text{dBm/tone} \)
Typical Performance Curves: $I_{DQ} = 760$ mA, $V_D = 4$ V, Full Bias

Detector Delta Voltage vs. Output Power, 71–76 GHz

Detector Delta Voltage vs. Output Power, 81–86 GHz

Noise Figure at Full and Reduced Bias
Calibration Plane -  
All data was measured on die with 200 µm pitch probes. All data was measured with an ISS cal.

App Note [1] Biasing -  
All gates should be pinched-off ($V_G < -1 \text{ V}$) before applying drain voltage ($V_D = 4 \text{ V}$). Then the gate voltages can be increased until the desired quiescent drain current is reached in each stage. The recommended quiescent full bias is $V_D = 4 \text{ V}$, $I_{D1} = 120 \text{ mA}$, $I_{D2} = 120 \text{ mA}$, $I_{D3} = 200 \text{ mA}$ and $I_{D4} = 320 \text{ mA}$. The performance in this datasheet has been measured with fixed gate voltage and no drain current regulation under large signal operation. It is also possible to regulate the drain current dynamically, to limit the DC power dissipation under RF drive. To turn off the device, the turn on bias sequence should be followed in reverse.

App Note [2] Bias Arrangement -  
Each DC pin ($V_D1,2,3,4$ and $V_G1,2,3,4$) needs to have bypass capacitors (120 pF and 10 nF) mounted as close to the MMIC as possible.

App Note [3] Common Gates and Drains -  
When biasing the device with only a single gate or drain source additional isolation is required between each stage. On the gate side a 10 Ω resistor should be placed in series and tied together in a star to a common supply. The drain side resistance should be reduced to less than 5 Ω to minimize any voltage drop across the resistor. Suitable bypass capacitors should still accompany each stage as per App Note [2].

App Note [4] Detector Biasing Schematic -  
As shown in the schematic below, the power detector is biased by matched 100 kΩ resistors to a +5 V supply. The difference voltage between $V_{DET}$ and $V_{REF}$ pins can be obtained using a differencing circuit.

App Note [5] Wire Bonding -  
The loop height of the RF bonds should be minimized. Where the die is mounted above the PCB, it is recommended to use Reverse Ball-Stitch-on-Ball bonds (BSOB). If the die is mounted inside a cavity on the board, forward loop bonding may result in a lower loop height. V-shape RF bond with two wires (diameter = 20 µm) is recommended for optimum RF performance. RF bond wire length to be minimized to reduce the inductance effect. Simulations suggest no more than 300 µm. Substrate RF pad can be optimized to improve the microstrip to MMIC bond transition as shown in the example below. Please see App Note [6] for further details.
App Note [6] RF Matching -
MAAP-011218 is designed to be a wideband RF power amplifier covering the 71 - 86 GHz band. By covering the full band, it enables customers to simplify BOM and circuitry for simple wideband performance. In cases where narrower band performance is preferred, external matching can be used to further optimise the return loss of the MMIC.

The board material used for matching was Isola Astra MT77. This has a dielectric constant ($\varepsilon_r$) = 3 and a loss tangent (tan $\delta$) of 0.0015. Simulations of the transition were performed in Analyst and can be provided on request. Transitions have been simulated to maintain return loss of $-8$ dB across the two bands of interest using Analyst.

Results
Low Band
Input Dimensions
Common to every optimisation

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High Band Optimisation
Input Side

High Band Optimisation
Output Side