MAAP-011145

Power Amplifier, 2 W
17.65 - 19.75 GHz

Features
- 25 dB Small Signal Gain
- 43 dBm Third Order Intercept Point (OIP3)
- 2 W Output P1dB
- 34.5 dBm Saturated Output Power
- Integrated Power Detector
- Bias 1330 mA @ 6 V
- Lead-Free 7 mm Cavity Package
- RoHS* Compliant and 260°C Reflow Compatible

Description
The MAAP-011145 is a power amplifier assembled in a 7 mm surface mount package with a temperature compensated integrated power detector operating from 17.65 to 19.75 GHz. The circuit provides 25 dB gain, 43 dBm OIP3, 2 W P1dB and 34.5 dBm saturated output power.

The device includes ESD protection and by-pass capacitors to ease the implementation and volume assembly of the packaged part.

This power amplifier is specifically designed for use in point-to-point radios for cellular backhaul applications in the 18 GHz band.

Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAAP-011145</td>
<td>Bulk Quantity</td>
</tr>
<tr>
<td>MAAP-011145-TR0500</td>
<td>500 Piece Reel</td>
</tr>
<tr>
<td>MAAP-011145-001SMB</td>
<td>Sample Board</td>
</tr>
</tbody>
</table>

1. Reference Application Note M513 for reel size information.

Functional Schematic

Pin Configuration

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Function</th>
<th>Pin No.</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Ground</td>
<td>11</td>
<td>Ground</td>
</tr>
<tr>
<td>2</td>
<td>RF Input</td>
<td>12</td>
<td>RF Output</td>
</tr>
<tr>
<td>3</td>
<td>Ground</td>
<td>13</td>
<td>Power Detector</td>
</tr>
<tr>
<td>4</td>
<td>Ground</td>
<td>14</td>
<td>Reference</td>
</tr>
<tr>
<td>5</td>
<td>Gate 1 Bias</td>
<td>15</td>
<td>Ground</td>
</tr>
<tr>
<td>6</td>
<td>Gate 2 Bias</td>
<td>16</td>
<td>No Connection</td>
</tr>
<tr>
<td>7</td>
<td>Gate 3 Bias</td>
<td>17</td>
<td>Ground</td>
</tr>
<tr>
<td>8</td>
<td>Ground</td>
<td>18</td>
<td>Drain 2 Bias</td>
</tr>
<tr>
<td>9</td>
<td>Drain 3 Bias</td>
<td>19</td>
<td>Drain 1 Bias</td>
</tr>
<tr>
<td>10</td>
<td>Ground</td>
<td>20</td>
<td>Ground</td>
</tr>
<tr>
<td>21</td>
<td>Paddle</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

2. All “No Connection” pins should be grounded.
3. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

### Electrical Specifications: \( V_{DD} = 6 \, \text{V}, \, I_{DQ}^4 = 1330 \, \text{mA}, \, T_A = +25^\circ\text{C} \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Units</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Small Signal Gain</td>
<td>dB</td>
<td>22.7</td>
<td>26</td>
<td>28.3</td>
</tr>
<tr>
<td>Gain variation over temp</td>
<td>dB</td>
<td>—</td>
<td>±1.7</td>
<td>—</td>
</tr>
<tr>
<td>Output IP3, +20 dBm SCL</td>
<td>dBm</td>
<td>40.5</td>
<td>44</td>
<td>—</td>
</tr>
<tr>
<td>Output IP3, +24 dBm SCL</td>
<td>dBm</td>
<td>37.5</td>
<td>42</td>
<td>—</td>
</tr>
<tr>
<td>OIP3 variation over temp</td>
<td>dB</td>
<td>—</td>
<td>±1.0</td>
<td>—</td>
</tr>
<tr>
<td>( P_{SAT} )</td>
<td>dBm</td>
<td>33.2</td>
<td>34.5</td>
<td>—</td>
</tr>
<tr>
<td>( P_{SAT} ) variation over temp</td>
<td>dBm</td>
<td>—</td>
<td>±0.2</td>
<td>—</td>
</tr>
<tr>
<td>( P_{1dB} )</td>
<td>dBm</td>
<td>—</td>
<td>34</td>
<td>—</td>
</tr>
<tr>
<td>Input Return Loss(^5)</td>
<td>dB</td>
<td>8</td>
<td>15</td>
<td>—</td>
</tr>
<tr>
<td>Output Return Loss(^5)</td>
<td>dB</td>
<td>8</td>
<td>10</td>
<td>—</td>
</tr>
<tr>
<td>Detector ( V_{DIFF}, , P_{OUT} = +20 , \text{dBm}^6,^7 )</td>
<td>V</td>
<td>0.5</td>
<td>1.1</td>
<td>1.7</td>
</tr>
<tr>
<td>Noise Figure(^6)</td>
<td>dB</td>
<td>—</td>
<td>7</td>
<td>8</td>
</tr>
<tr>
<td>Gain Dynamic Range (&gt;20 mA/dB)(^6)</td>
<td>dB</td>
<td>12</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Noise Figure at Gain Regulation(^6)</td>
<td>dB/dB</td>
<td>—</td>
<td>—</td>
<td>0.4</td>
</tr>
<tr>
<td>OIP3 at Gain Regulation(^6)</td>
<td>dB/dB</td>
<td>—</td>
<td>—</td>
<td>1.3</td>
</tr>
<tr>
<td>( P_{SAT} ) at Gain Regulation(^6)</td>
<td>dB/dB</td>
<td>—</td>
<td>—</td>
<td>0.2</td>
</tr>
<tr>
<td>Isolation (S21 at ( V_G ) off)(^5)</td>
<td>dB</td>
<td>—</td>
<td>—</td>
<td>-15</td>
</tr>
<tr>
<td>Gain Ripple over frequency(^5)</td>
<td>dB</td>
<td>—</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>Power consumption @ ( P_{OUT} \leq 27 , \text{dBm} )</td>
<td>W</td>
<td>—</td>
<td>—</td>
<td>8.4</td>
</tr>
<tr>
<td>Power variation over temp(^5)</td>
<td>dB/\degree\text{C}</td>
<td>—</td>
<td>—</td>
<td>0.02</td>
</tr>
<tr>
<td>Gate Voltage</td>
<td>V</td>
<td>—</td>
<td>-1.0</td>
<td>-0.8</td>
</tr>
<tr>
<td>Detector Output Voltage range(^6,^7)</td>
<td>mV</td>
<td>10</td>
<td>—</td>
<td>4000</td>
</tr>
<tr>
<td>Detector Measure Range(^6,^7)</td>
<td>dBm</td>
<td>-8</td>
<td>—</td>
<td>30</td>
</tr>
<tr>
<td>Detector Precision(^6,^7)</td>
<td>mV/dB</td>
<td>2</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

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4. Adjust \( V_G1, V_G2 \) and \( V_G3 \) between -1.2 and -0.8V to achieve specified \( I_{DQ} \) (\( I_{DQ} = I_{D1}+I_{D2}+I_{D3} \)). \( V_G1, V_G2 \) and \( V_G3 \) are nominally the same voltage.
5. Only guaranteed on MACOM probe board.
6. May require adjusting the current on each stage separately.
7. Detector only tested @ 20 dBm/SCL at production
Absolute Maximum Ratings\(^8,9,10\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Power</td>
<td>18 dBm</td>
</tr>
<tr>
<td>Drain Voltage ((V_{D1,2,3}))</td>
<td>+7 V</td>
</tr>
<tr>
<td>Gate Voltage ((V_{G1,2,3}))</td>
<td>-3 V to -0.74 V</td>
</tr>
<tr>
<td>Drain to Gate Voltage ((V_{D-VG}))</td>
<td>+10 V</td>
</tr>
<tr>
<td>Current ((I_{DQ} = I_{D1}+I_{D2}+I_{D3}))</td>
<td>2000 mA</td>
</tr>
<tr>
<td>Detector Pin</td>
<td>+6 V</td>
</tr>
<tr>
<td>Detector Reference Pin</td>
<td>+6 V</td>
</tr>
<tr>
<td>Detector (P_{OUT})</td>
<td>35 dBm</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>+175°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C to +150°C</td>
</tr>
</tbody>
</table>

Maximum Operating Ratings\(^11,12\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>(P_{DISS})</td>
<td>11.2 W</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>+150°C</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-40°C to +85°C</td>
</tr>
</tbody>
</table>

11. Channel temperature directly affects device MTTF. Channel temperature should be kept as low as possible to maximize lifetime. Thermal resistance, \(\Theta_{jc}\), is 5.8 °C/W.
12. For saturated performance, it is recommended that the sum of \((2V_{DD} + \text{abs}(V_{GG}))\) < 15 V.

Handling Procedures

Please observe the following precautions to avoid damage:

**Static Sensitivity**

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these CDM class 2, HBM class 1B devices.
Typical Performance Curves: 8 W Quiescent Bias, $V_D = 6$ V

**Gain**

![Gain Graph](image1)

**Input Return Loss**

![Input Return Loss Graph](image2)

**Output Return Loss**

![Output Return Loss Graph](image3)

**$P_{1dB}$**

![P1dB Graph](image4)

**$P_{3dB}$**

![P3dB Graph](image5)

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Power Amplifier, 2 W
17.65 - 19.75 GHz

Typical Performance Curves: \( V_D = 6 \, V \)

**Gain @ 17.7 GHz**

**Gain @ 18.7 GHz**

**Gain @ 19.7 GHz**

**OIP3 @ 17.7 GHz**

**OIP3 @ 18.7 GHz**

**OIP3 @ 19.7 GHz**

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Typical Performance Curves: 8 W Quiescent Bias, $V_D = 6$ V

**Lower and Upper Intermodulation Tones @ 17.7 GHz**

![Graph showing lower and upper intermodulation tones at 17.7 GHz](graph1)

**OIP3 vs. Output Power**

![Graph showing OIP3 vs. output power](graph2)

**Lower and Upper Intermodulation Tones @ 18.7 GHz**

![Graph showing lower and upper intermodulation tones at 18.7 GHz](graph3)

**Detector Delta Voltage vs. Output Power**

![Graph showing detector delta voltage vs. output power](graph4)

**Lower and Upper Intermodulation Tones @ 19.7 GHz**

![Graph showing lower and upper intermodulation tones at 19.7 GHz](graph5)
Biasing -
All gates should be pinched-off ($V_G < -2$ V) before applying drain voltage ($V_D = 6$ V). Then the gate voltages can be increased until the desired quiescent drain current is reached in each stage. The recommended quiescent bias is $V_D = 6$ V, $I_{D1} = 190$ mA, $I_{D2} = 380$ mA and $I_{D3} = 762$ mA. The performance in this datasheet has been measured with fixed gate voltage and no drain current regulation under large signal operation. It is also possible to regulate the drain current dynamically, to limit the DC power dissipation under RF drive. To turn off the device, the turn on bias sequence should be followed in reverse.

Bias Arrangement -
Each DC pin ($V_{D1,2,3}$ and $V_{G1,2,3}$) needs to have bypass capacitance (120 pF and 10 nF) mounted as close to the MMIC as possible.

Power Detector -
As shown in the schematic below, the power detector is implemented by providing +5 V bias and measuring the difference in output voltage with standard op-amp in a differential mode configuration.

Application Schematic
Package Outline Drawing and Recommended Land Pattern†

All dimensions are in mm.

† Meets JEDEC moisture sensitivity level 3 requirements.