MAAP-011140-DIE

Power Amplifier, 6 W
27.5 - 30.0 GHz

Rev. V3

Features

- High Gain: 24 dB
- P1dB: 37.5 dBm
- P\text{SAT}: 38.5 dBm
- IM3 Level: -24 dBc @ P\text{OUT} = 33 dBm/tone
- Power Added Efficiency: 23% @ P\text{SAT}
- Return Loss: 12 dB
- Bare Die Dimensions: 3.6 x 3.8 x 0.05 mm
- RoHS* Compliant

Description

The MAAP-011140-DIE is a 4-stage, 6 W power amplifier in bare die form. This power amplifier operates from 27.5 to 30.0 GHz and provides 24 dB of linear gain, 6 W saturated output power, and 23% efficiency while biased at 6 V.

The MAAP-011140-DIE is a power amplifier ideally suited for VSAT communications.

This product is fabricated using a GaAs pHEMT device process which features full passivation for enhanced reliability.

Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAAP-011140-DIE</td>
<td>Die in Gel Pack\textsuperscript{1}</td>
</tr>
</tbody>
</table>

1. Die quantity varies

Functional Diagram

Pin Configuration\textsuperscript{2}

<table>
<thead>
<tr>
<th>Pad</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RF\text{IN}</td>
<td>RF Input</td>
</tr>
<tr>
<td>2, 4, 7, 9, 11, 13, 15, 16, 18 &amp; backside</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>3</td>
<td>V\text{D}1</td>
<td>Drain Voltage Stage 1</td>
</tr>
<tr>
<td>5</td>
<td>V\text{D}2</td>
<td>Drain Voltage Stage 2</td>
</tr>
<tr>
<td>6, 14</td>
<td>V\text{D}3</td>
<td>Drain Voltage Stage 3</td>
</tr>
<tr>
<td>8, 12</td>
<td>V\text{D}4</td>
<td>Drain Voltage Stage 4</td>
</tr>
<tr>
<td>10</td>
<td>RF\text{OUT}</td>
<td>RF Output</td>
</tr>
<tr>
<td>17</td>
<td>V\text{G}</td>
<td>Gate Voltage</td>
</tr>
</tbody>
</table>

2. Backside metal is RF, DC and thermal ground.

\textsuperscript{1} Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.
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Electrical Specifications\(^3\): Freq. = 30 GHz, \(T_C = +25^\circ C\), \(V_D = +6 \, V\), \(Z_0 = 50 \, \Omega\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Units</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>(P_{IN} = 0 , dBm)</td>
<td>dB</td>
<td>22</td>
<td>24</td>
<td>—</td>
</tr>
<tr>
<td>(P_{OUT})</td>
<td>(P_{IN} = 17 , dBm)</td>
<td>dBm</td>
<td>36.0</td>
<td>37.5</td>
<td>—</td>
</tr>
<tr>
<td>IM3 Level</td>
<td>(P_{OUT} = 33 , dBm / tone)</td>
<td>dBc</td>
<td>—</td>
<td>-24</td>
<td>—</td>
</tr>
<tr>
<td>Power Added Efficiency</td>
<td>(P_{SAT} (P_{IN} = 17 , dBm))</td>
<td>%</td>
<td>23</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Input Return Loss</td>
<td>(P_{IN} = -20 , dBm)</td>
<td>dB</td>
<td>—</td>
<td>12</td>
<td>—</td>
</tr>
<tr>
<td>Output Return Loss</td>
<td>(P_{IN} = -20 , dBm)</td>
<td>dB</td>
<td>—</td>
<td>12</td>
<td>—</td>
</tr>
<tr>
<td>Quiescent Current</td>
<td>(I_{DO}) (see bias conditions, page 5)</td>
<td>mA</td>
<td>—</td>
<td>3000</td>
<td>—</td>
</tr>
<tr>
<td>Current</td>
<td>(P_{SAT} (P_{IN} = 17 , dBm))</td>
<td>mA</td>
<td>—</td>
<td>5250</td>
<td>—</td>
</tr>
</tbody>
</table>

3. Specifications apply to MMIC die with two RF input and two RF output bond wires, and tested with 50 \(\Omega\) GSG probes. Further performance tuning to optimize the RF input and RF output impedance matching is shown on Recommended Bonding Diagram and PCB Layout Details (pg. 4). Typical performance curves are achieved by using the recommended bonding diagram and PCB layout detail.

Maximum Operating Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Power</td>
<td>+19 dBm</td>
</tr>
<tr>
<td>Junction Temperature(^4,5)</td>
<td>+160°C</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-40°C to +85°C</td>
</tr>
</tbody>
</table>

4. Operating at nominal conditions with \(T_C \leq +160°C\) will ensure MTTF > 1 \times 10^6 hours.
5. Junction Temperature (\(T_J\)) = \(T_C + \Theta_{JC} \times (V \times I) - (P_{OUT} - P_{IN})\)
   Typical thermal resistance (\(\Theta_{JC}\)) = 3.4°C/W.
   a) For \(T_C = +25°C\), \(T_J = 108°C @ 6 \, V, 5.25 \, A, P_{OUT} = 38.5, P_{IN} = 17 \, dBm\)
   b) For \(T_C = +80°C\), \(T_J = 159°C @ 6 \, V, 4.96 \, A, P_{OUT} = 38.1, P_{IN} = 17 \, dBm\)

Absolute Maximum Ratings\(^6,7\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Absolute Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Power</td>
<td>+24 dBm</td>
</tr>
<tr>
<td>Drain Voltage</td>
<td>+6.5 V</td>
</tr>
<tr>
<td>Gate Voltage</td>
<td>-3 to 0 V</td>
</tr>
<tr>
<td>Junction Temperature(^8)</td>
<td>+175°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C to +150°C</td>
</tr>
</tbody>
</table>

6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. MACOM does not recommend sustained operation near these survivability limits.
8. Junction Temperature directly effects device MTTF. Junction temperature should be kept as low as possible to maximize lifetime.
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Application PCB Layout

Application Diagram

Application Parts List

<table>
<thead>
<tr>
<th>Part</th>
<th>Value</th>
<th>Case Style</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1 - C7</td>
<td>0.01 µF</td>
<td>0402</td>
</tr>
<tr>
<td>C8 - C12</td>
<td>1 µF</td>
<td>0603</td>
</tr>
<tr>
<td>C13 - C16</td>
<td>10 µF</td>
<td>0805</td>
</tr>
<tr>
<td>R1 - R7</td>
<td>10 Ω</td>
<td>0402</td>
</tr>
<tr>
<td>L1 - L4 (Chip Ferrite Bead)</td>
<td>BLM18HE601SN1D</td>
<td>0603</td>
</tr>
</tbody>
</table>

PCB Material Specifications

Top Layer: 1/2 oz Copper Cladding, 0.017 mm thickness
Dielectric Layer: Rogers RO4350B, 0.101 mm thickness
Bottom Layer: 1/2 oz Copper Cladding, 0.017 mm thickness
Finished overall thickness: 0.135 mm
Recommended Bonding Diagram and PCB Layout Detail:

For optimum power match, RF input and output microstrip lines require open stubs on the application board for bonding wire inductance compensation. Optimum bonding wire inductance for the RF I/O connection is 0.2 nH, and physical length for the gold bond wire (.001” dia.) is approximately 350 µm each for the two wire connection.
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Application Information
The MAAP-011140 is designed to be easy to use yet high performance. The ultra small size and simple bias allows easy placement on system board. RF input and output ports are DC de-coupled internally.

Biasing conditions
Recommended biasing conditions are $V_D = 6$ V, $I_{DQ} = 3000$ mA (controlled with $V_G$). The drain bias voltage range, $V_D$, is 3 to 6.5 V, and the quiescent drain current biasing range, $I_{DQ}$, is 2000 to 4000 mA.

$V_D$ bias must be applied to $V_D1$, $V_D2$, $V_D3$, and $V_D4$ pads.

Both $V_D3$ pads (6 and 14) are required for current symmetry.

Both $V_D4$ pads (8 and 12), are required for current symmetry.

A single DC voltage ($V_G$) will bias all amplifier stages. Muting can be accomplished by setting the $V_G$ to the pinched off voltage ($V_G = -2$ V).

Die Attachment
This product is manufactured from 0.050 mm (0.002”) thick GaAs substrate and has vias through to the backside to enable grounding to the circuit.

Recommended conductive epoxy is Namics Unimec XH9890-6. Epoxy should be applied and cured in accordance with the manufacturer’s specifications and should avoid contact with the top of the die.

Operating the MAAP-01140-DIE

Turn-on
1. Apply $V_G$ (-1.5 V).
2. Apply $V_D$ (6.0 V typical).
3. Set $I_{DQ}$ by adjusting $V_G$ more positive (typically $V_G \sim -0.9$ V for $I_{DQ} = 3000$ mA).
4. Apply RF$_{IN}$ signal.

Turn-off
1. Remove RF$_{IN}$ signal.
2. Decrease $V_G$ to -1.5 V.
3. Decrease $V_D$ to 0 V.

Handling Procedures
Please observe the following precautions to avoid damage:

Static Sensitivity
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.
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Typical Performance Curves

Small Signal Gain vs. Frequency over Temperature

Small Signal Gain vs. Frequency over Bias Voltage

Input Return Loss vs. Frequency over Temperature

Input Return Loss vs. Frequency over Bias Voltage

Output Return Loss vs. Frequency over Temperature

Output Return Loss vs. Frequency over Bias Voltage
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Typical Performance Curves

$P_{\text{SAT}}$ vs. Frequency over Temperature

$P_{\text{SAT}}$ vs. Frequency over Bias Voltage

$P_{1\text{dB}}$ vs. Frequency over Temperature

$P_{1\text{dB}}$ vs. Frequency over Bias Voltage

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Typical Performance Curves

**Output IP3 vs. Frequency over Temperature**

![Graph showing Output IP3 vs. Frequency over Temperature](image)

**Output IP3 vs. Frequency over Bias Voltage**

![Graph showing Output IP3 vs. Frequency over Bias Voltage](image)

**IM3 vs. Frequency over Temperature**  
\( P_{\text{OUT}} = +33 \text{ dBm/Tone} \)

![Graph showing IM3 vs. Frequency over Temperature](image)

**IM3 vs. Frequency over Bias Voltage**  
\( P_{\text{OUT}} = +33 \text{ dBm/Tone} \)

![Graph showing IM3 vs. Frequency over Bias Voltage](image)
**Typical Performance Curves**

**P1dB, P_{SAT} vs. Frequency**

![P1dB, P_{SAT} vs. Frequency Graph]

**PAE, Gain vs. Frequency**

![PAE, Gain vs. Frequency Graph]

**IM3 vs. Output Power per Tone**

![IM3 vs. Output Power per Tone Graph]

**Output IP3 vs. Output Power per Tone**

![Output IP3 vs. Output Power per Tone Graph]
Typical Performance Curves

Output Power vs. Input Power

PAE vs. Input Power

Drain Current vs. Input Power

Quiescent Drain Current over Temperature

9. Typical performance curves are achieved by using the recommended bonding diagram and PCB layout detail.
MMIC Die Outline

Bond Pad Detail

<table>
<thead>
<tr>
<th>Pad</th>
<th>Size (x)</th>
<th>Size (y)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A, B, C</td>
<td>88</td>
<td>88</td>
</tr>
<tr>
<td>D, M</td>
<td>169</td>
<td>88</td>
</tr>
<tr>
<td>E, L, O</td>
<td>161</td>
<td>88</td>
</tr>
<tr>
<td>F</td>
<td>84</td>
<td>84</td>
</tr>
<tr>
<td>G, K</td>
<td>249</td>
<td>88</td>
</tr>
<tr>
<td>H, J, Q, S</td>
<td>89</td>
<td>99</td>
</tr>
<tr>
<td>I, R</td>
<td>89</td>
<td>159</td>
</tr>
<tr>
<td>N, P</td>
<td>158</td>
<td>88</td>
</tr>
</tbody>
</table>

Notes:
1. All units are in µm, unless otherwise noted, with a tolerance of ±5 µm.
2. Die thickness is 50 ±10 µm.
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