Features

- High Gain: 22 dB @ 30 GHz
- P1dB: 34.5 dBm
- PSAT: 36 dBm
- IM3 Level: -27 dBc @ POUT 29 dBm/tone
- Power Added Efficiency: 23% @ PSAT
- Lead-Free 5 mm 32-lead AQFN Plastic Package
- RoHS* Compliant

Description

The MAAP-011139 is a 4-stage, 4 W power amplifier assembled in a lead-free 5 mm 32-lead AQFN plastic package. This power amplifier operates from 28.5 to 31 GHz and provides 22 dB of linear gain, 4 W saturated output power, and 23% efficiency while biased at 6 V.

The MAAP-011139 is a power amplifier ideally suited for VSAT communications.

This product is fabricated using a GaAs pHEMT process which features full passivation for enhanced reliability.

Ordering Information1,2

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAAP-011139-TR0500</td>
<td>500 piece reel</td>
</tr>
<tr>
<td>MAAP-011139-SMB</td>
<td>Sample Board</td>
</tr>
</tbody>
</table>

1. Reference Application Note M513 for reel size information.
2. All sample boards include 3 loose parts.


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Power Amplifier, 4 W  
28.5 - 31 GHz

Electrical Specifications: Freq. = 30 GHz, $T_A = +25^\circ C$, $V_D = 6$ V, $Z_0 = 50$ Ω

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Units</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>$P_{IN} = 0$ dBm</td>
<td>dB</td>
<td>19</td>
<td>22</td>
<td>-</td>
</tr>
<tr>
<td>$P_{OUT}$</td>
<td>$P_{IN} = +17$ dBm</td>
<td>dBm</td>
<td>34.5</td>
<td>36.0</td>
<td>-</td>
</tr>
<tr>
<td>IM3 Level</td>
<td>$P_{OUT} = +29$ dBm / tone</td>
<td>dBc</td>
<td>-27</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Power Added Efficiency</td>
<td>$P_{SAT}$ ($P_{IN} = +17$ dBm)</td>
<td>%</td>
<td>-</td>
<td>23</td>
<td>-</td>
</tr>
<tr>
<td>Input Return Loss</td>
<td>$P_{IN} = -20$ dBm</td>
<td>dB</td>
<td>-</td>
<td>10</td>
<td>-</td>
</tr>
<tr>
<td>Output Return Loss</td>
<td>$P_{IN} = -20$ dBm</td>
<td>dB</td>
<td>-</td>
<td>10</td>
<td>-</td>
</tr>
<tr>
<td>Quiescent Current</td>
<td>$I_{DO}$ (see bias conditions, page 5)</td>
<td>mA</td>
<td>-</td>
<td>2000</td>
<td>-</td>
</tr>
<tr>
<td>Current</td>
<td>$P_{SAT}$ ($P_{IN} = +17$ dBm)</td>
<td>mA</td>
<td>-</td>
<td>2700</td>
<td>-</td>
</tr>
</tbody>
</table>

Maximum Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Power</td>
<td>$+17$ dBm</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>$+160^\circ$C</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>$-40^\circ$C to $+85^\circ$C</td>
</tr>
</tbody>
</table>

5. Operating at nominal conditions with junction temperature ≤ $+160^\circ$C will ensure MTTF > $1 \times 10^6$ hours.
6. Junction Temperature ($T_J = T_C + \Theta_{JC} \times (V^* I) - (P_{OUT} - P_{IN})$).
   Typical thermal resistance ($\Theta_{JC}$) = 4.4 °C/W.
   a) For $T_C = +25^\circ$C,
      $T_J = +79^\circ$C @ 6 V, 2.7 A, $P_{OUT} = 36$ dBm, $P_{IN} = 17$ dBm
   b) For $T_C = +85^\circ$C,
      $T_J = +143^\circ$C @ 6 V, 2.7 A, $P_{OUT} = 35.1$ dBm, $P_{IN} = 17$ dBm

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Absolute Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Power</td>
<td>$+23$ dBm</td>
</tr>
<tr>
<td>Drain Voltage</td>
<td>$+6.5$ V</td>
</tr>
<tr>
<td>Gate Voltage</td>
<td>-3 to 0 V</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>$+175^\circ$C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C to $+125^\circ$C</td>
</tr>
</tbody>
</table>

7. Exceeding any one or combination of these limits may cause permanent damage to this device.
8. MACOM does not recommend sustained operation near these survivability limits.
9. Junction Temperature directly effects device MTTF. Junction temperature should be kept as low as possible to maximize lifetime.
Sample Board Layout

![Sample Board Layout Diagram]

Application Schematic

![Application Schematic Diagram]

Parts List

<table>
<thead>
<tr>
<th>Part</th>
<th>Value</th>
<th>Case Style</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1 - C7</td>
<td>0.01 µF</td>
<td>0402</td>
</tr>
<tr>
<td>C8 - C12</td>
<td>1 µF</td>
<td>0603</td>
</tr>
<tr>
<td>C13 - C16</td>
<td>10 µF</td>
<td>0805</td>
</tr>
<tr>
<td>R1 - R7</td>
<td>10 Ω</td>
<td>0402</td>
</tr>
<tr>
<td>L1 - L4</td>
<td>BLM18HE601SN1D</td>
<td>0603</td>
</tr>
</tbody>
</table>

Sample Board Material Specifications

Top Layer: 1/2 oz Copper Cladding, 0.017 mm thickness
Dielectric Layer: Rogers RO4003C 0.203 mm thickness
Bottom Layer: 1/2 oz Copper Cladding, 0.017 mm thickness
Finished overall thickness: 0.238 mm
Sample Board Layout: RF input and output port pre-matching circuit patterns are designed to compensate for packaging effects. Input and output match patterns are identical.

Copper-filled vias are required beneath the package. Diameter = 0.3 mm, Spacing = 0.5 mm, 7x7 array

All units are in microns.
Application Information
The MAAP-011139 is designed to be easy to use yet high performance. The ultra small size and simple bias allow easy placement on system board. RF input and output ports are DC de-coupled internally.

Biasing conditions
Recommended biasing conditions are \( V_D = 6 \text{ V}, \) \( I_{DQ} = 2000 \text{ mA} \) (controlled with \( V_G \)). The drain bias voltage range is 3 to 6 V, and the quiescent drain current biasing range is 1500 to 2500 mA.

\( V_G \) pins 10 and 11 are connected internally; choose either pin for layout convenience. Muting can be accomplished by setting the \( V_G \) to the pinched off voltage \( (V_G = -2 \text{ V}) \).

\( V_D \) bias must be applied to \( V_{D1}, V_{D2}, V_{D3}, \) and \( V_{D4} \) pins.

\( V_{D3} \) pins 14 and either pin 27 or 28 are required for current symmetry. Pins 27 and 28 are connected internally; choose either pin for layout convenience.

Both \( V_{D4} \) pins 15 and 26 are required for current symmetry.

Operating the MAAP-011139

Turn-on
1. Apply \( V_G \) (-1.5 V).
2. Apply \( V_D \) (6.0 V typical).
3. Set \( I_{DQ} \) by adjusting \( V_G \) more positive (typically \( V_G \approx -0.9 \text{ V} \) for \( I_{DQ} = 2000 \text{ mA} \)).
4. Apply RF\(_{IN}\) signal.

Turn-off
1. Remove RF\(_{IN}\) signal.
2. Decrease \( V_G \) to -1.5 V.
3. Decrease \( V_D \) to 0 V.

Handling Procedures
Please observe the following precautions to avoid damage:

Static Sensitivity
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices.
Typical Performance Curves

Small Signal Gain vs. Frequency over Temperature

![Small Signal Gain vs. Frequency over Temperature graph]

Small Signal Gain vs. Frequency over Bias Voltage

![Small Signal Gain vs. Frequency over Bias Voltage graph]

Input Return Loss vs. Frequency over Temperature

![Input Return Loss vs. Frequency over Temperature graph]

Input Return Loss vs. Frequency over Bias Voltage

![Input Return Loss vs. Frequency over Bias Voltage graph]

Output Return Loss vs. Frequency over Temperature

![Output Return Loss vs. Frequency over Temperature graph]

Output Return Loss vs. Frequency over Bias Voltage

![Output Return Loss vs. Frequency over Bias Voltage graph]
Typical Performance Curves

$P_{\text{SAT}}$ vs. Frequency over Temperature

$P_{\text{SAT}}$ vs. Frequency over Bias Voltage

$P_{\text{1dB}}$ vs. Frequency over Temperature

$P_{\text{1dB}}$ vs. Frequency over Bias Voltage

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Typical Performance Curves

Output IP3 over Temperature (Pout=29 dBm/tone)

Output IP3 over Bias Voltage (Pout=29 dBm/Tone)

IM3 over Temperature (Pout=29 dBm/tone)

IM3 over Bias Voltage (Pout=29 dBm/tone)
Typical Performance Curves

\( P_{1\text{dB}}, P_{\text{SAT}} \) vs. Frequency

\[ \begin{align*}
\text{Output Power per tone (dBm)} & = 30, 35, 40, 45, 50 \\
\text{Frequency (GHz)} & = 28.5, 29, 30, 31
\end{align*} \]

\( \text{PAE, Gain vs. Frequency} \)

\[ \begin{align*}
\text{Output Power per tone (dBm)} & = 30, 35, 40, 45, 50 \\
\text{Frequency (GHz)} & = 28.5, 29, 30, 31
\end{align*} \]

\( \text{IM3 vs. Output Power (per tone)} \)

\[ \begin{align*}
\text{Output Power per tone (dBm)} & = 5, 10, 15, 20, 25, 30, 35 \\
\text{IM3 (dBc)} & = -70, -60, -50, -40, -30, -20, -10
\end{align*} \]

\( \text{Output IP3 vs. Output Power (per tone)} \)

\[ \begin{align*}
\text{Output Power per tone (dBm)} & = 5, 10, 15, 20, 25, 30, 35 \\
\text{Output IP3 (dBm)} & = 30, 35, 40, 45, 50
\end{align*} \]

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Typical Performance Curves

Output Power vs. Input Power

PAE vs. Input Power

Bias Current vs. Input Power

Quiescent Drain Current vs. Temperature

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Lead-Free 5 mm QFN 32-Lead†

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 3 requirements.
Plating is NiPdAu.

All Dimensions shown as inches [mm]

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