Features
- High Gain: 24 dB @ 30 GHz
- P1dB: 34.5 dBm
- PSAT: 36.5 dBm
- IM3 Level: -27 dBc @ POUT = 29 dBm/tone
- Power Added Efficiency: 23% @ PSAT
- Return Loss: 10 dB
- Bare Die Dimensions: 3.1 x 2.8 x 0.05 mm
- RoHS* Compliant

Description
The MAAP-011139-DIE is a 4-stage, 4 W power amplifier in bare die form. This power amplifier operates from 28.5 to 31.0 GHz and provides 24 dB of linear gain, 4 W saturated output power, and 23% efficiency while biased at 6 V.

The MAAP-011139-DIE is a power amplifier ideally suited for VSAT communications.

This product is fabricated using a GaAs pHEMT device process which features full passivation for enhanced reliability.

Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAAP-011139-DIE</td>
<td>Die in Gel Pack</td>
</tr>
</tbody>
</table>

1. Die quantity varies

Functional Diagram

Pin Configuration

<table>
<thead>
<tr>
<th>Pad</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RF_IN</td>
<td>RF Input</td>
</tr>
<tr>
<td>2, 16</td>
<td>V_G</td>
<td>Gate Voltage</td>
</tr>
<tr>
<td>3, 7, 11, 15 &amp; backside</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>4, 14</td>
<td>V_D1</td>
<td>Drain Voltage 1</td>
</tr>
<tr>
<td>5, 13</td>
<td>V_D2</td>
<td>Drain Voltage 2</td>
</tr>
<tr>
<td>6, 12</td>
<td>V_D3</td>
<td>Drain Voltage 3</td>
</tr>
<tr>
<td>8, 10</td>
<td>V_D4</td>
<td>Drain Voltage 4</td>
</tr>
<tr>
<td>9</td>
<td>RF_OUT</td>
<td>RF Output</td>
</tr>
</tbody>
</table>

2. Backside metal is RF, DC and thermal ground.

Electrical Specifications\(^3\): Freq. = 30 GHz, \(T_C = +25°C\), \(V_D = +6\) V, \(Z_0 = 50\) \(Ω\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Units</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>(P_{IN} = 0) dBm</td>
<td>dB</td>
<td>22</td>
<td>24</td>
<td></td>
</tr>
<tr>
<td>(P_{OUT})</td>
<td>(P_{IN} = 17) dBm</td>
<td>dBm</td>
<td>35.0</td>
<td>36.5</td>
<td></td>
</tr>
<tr>
<td>IM3 Level</td>
<td>(P_{OUT} = 29) dBm / tone</td>
<td>dBc</td>
<td></td>
<td>-27</td>
<td></td>
</tr>
<tr>
<td>Power Added Efficiency</td>
<td>(P_{SAT}(P_{IN} = 17) dBm)</td>
<td>%</td>
<td></td>
<td>23</td>
<td></td>
</tr>
<tr>
<td>Input Return Loss</td>
<td>(P_{IN} = -20) dBm</td>
<td>dB</td>
<td></td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>Output Return Loss</td>
<td>(P_{IN} = -20) dBm</td>
<td>dB</td>
<td></td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>Quiescent Current</td>
<td>(I_{DQ}) (see bias conditions, page 5)</td>
<td>mA</td>
<td></td>
<td>2000</td>
<td></td>
</tr>
<tr>
<td>Current</td>
<td>(P_{SAT}(P_{IN} = +17) dBm)</td>
<td>mA</td>
<td></td>
<td>3200</td>
<td></td>
</tr>
</tbody>
</table>

3. Specifications apply to MMIC die with two RF input and two RF output bond wires.

Maximum Operating Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Power</td>
<td>+17 dBm</td>
</tr>
<tr>
<td>Junction Temperature(^4,5)</td>
<td>+160°C</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-40°C to +85°C</td>
</tr>
</tbody>
</table>

4. Operating at nominal conditions with junction temperature \(\leq +160°C\) will ensure MTTF > 1 \(\times 10^8\) hours.

5. Junction Temperature \((T_J) = T_C + \Theta_{JC} \times ((V * I) - (P_{OUT} - P_{IN}))\)
   Typical thermal resistance \((\Theta_{JC}) = 3.4°C/W\).
   a) For \(T_C = +25°C\), \(T_J = +75°C \at 6\) V, 3.2 A, \(P_{OUT} = 36.5\) dBm, \(P_{IN} = 17\) dBm
   b) For \(T_C = +85°C\), \(T_J = +133°C \at 6\) V, 3.0 A, \(P_{OUT} = 36.0\) dBm, \(P_{IN} = 17\) dBm

Absolute Maximum Ratings\(^6,7\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Absolute Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Power</td>
<td>+23 dBm</td>
</tr>
<tr>
<td>Drain Voltage</td>
<td>+6.5 V</td>
</tr>
<tr>
<td>Gate Voltage</td>
<td>-3 to 0 V</td>
</tr>
<tr>
<td>Junction Temperature(^6)</td>
<td>+175°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C to +150°C</td>
</tr>
</tbody>
</table>

6. Exceeding any one or combination of these limits may cause permanent damage to this device.

7. MACOM does not recommend sustained operation near these survivability limits.

8. Junction temperature directly affects device MTTF. Junction temperature should be kept as low as possible to maximize lifetime.
Application PCB Layout

Application Diagram

Application Parts List

<table>
<thead>
<tr>
<th>Part</th>
<th>Value</th>
<th>Case Style</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1 - C7</td>
<td>0.01 µF</td>
<td>0402</td>
</tr>
<tr>
<td>C8 - C12</td>
<td>1 µF</td>
<td>0603</td>
</tr>
<tr>
<td>C13 - C16</td>
<td>10 µF</td>
<td>0805</td>
</tr>
<tr>
<td>R1 - R7</td>
<td>10 Ω</td>
<td>0402</td>
</tr>
<tr>
<td>L1 - L4</td>
<td>BLM18HE601SN1D</td>
<td>0603</td>
</tr>
</tbody>
</table>

PCB Material Specifications

Top Layer: 1/2 oz Copper Cladding, 0.017 mm thickness
Dielectric Layer: Rogers RO4350B, 0.101 mm thickness
Bottom Layer: 1/2 oz Copper Cladding, 0.017 mm thickness
Finished overall thickness: 0.135 mm
Recommended Bonding Diagram and PCB Layout Detail:

For optimum power match, RF input and output microstrip lines require open stubs on the application board for bonding wire inductance compensation. Optimum bonding wire inductance for the RF I/O connection is 0.2 nH, and physical length for the gold bond wire (.001” dia.) is approximately 350 µm each for the two wire connection.

All units are in microns.
Application Information
The MAAP-011139 is designed to be easy to use yet high performance. The ultra small size and simple bias allow easy placement on system board. RF input and output ports are DC de-coupled internally.

Biasing conditions
Recommended biasing conditions are \( V_D = 6 \text{ V} \), \( I_{DQ} = 2000 \text{ mA} \) (controlled with \( V_G \)). The drain bias voltage range is 3 to 6 V, and the quiescent drain current biasing range is 1500 to 2500 mA.

\( V_G \) pads 2 and 16 are connected internally; choose either pad for layout convenience. Muting can be accomplished by setting the \( V_G \) to the pinched off voltage (\( V_G = -2 \text{ V} \)).

\( V_D \) bias must be applied to \( V_D1, V_D2, V_D3, \) and \( V_D4 \) pads.

\( V_D1 \) pads 4 and 14 are connected internally, and only one pad is required for biasing. Choose either pad for layout convenience.

\( V_D2 \) pads 5 and 13 are connected internally, and only one pad is required for biasing. Choose either pad for layout convenience.

Both \( V_D3 \) pads (6 and 12) are required for current symmetry.

Both \( V_D4 \) pads (8 and 10) are required for current symmetry.

Operating the MAAP-011139-DIE

Turn-on
1. Apply \( V_G \) (-1.5 V).
2. Apply \( V_D \) (6.0 V typical).
3. Set \( I_{DQ} \) by adjusting \( V_G \) more positive (typically \( V_G \approx -0.9 \text{ V} \) for \( I_{DQ} = 2000 \text{ mA} \)).
4. Apply RF\(_{IN}\) signal.

Turn-off
1. Remove RF\(_{IN}\) signal.
2. Decrease \( V_G \) to -1.5 V.
3. Decrease \( V_D \) to 0 V.

Handling Procedures
Please observe the following precautions to avoid damage:

Static Sensitivity
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices.

Die Attachment
This product is manufactured from 0.050 mm (0.002”) thick GaAs substrate and has vias through to the backside to enable grounding to the circuit.

Recommended conductive epoxy is Namics Unimec XH9890-6. Epoxy should be applied and cured in accordance with the manufacturer’s specifications and should avoid contact with the top of the die.
Typical Performance Curves

**Small Signal Gain vs. Frequency over Temperature**

![Small Signal Gain vs. Frequency over Temperature graph](image)

**Small Signal Gain vs. Frequency over Bias Voltage**

![Small Signal Gain vs. Frequency over Bias Voltage graph](image)

**Input Return Loss vs. Frequency over Temperature**

![Input Return Loss vs. Frequency over Temperature graph](image)

**Input Return Loss vs. Frequency over Bias Voltage**

![Input Return Loss vs. Frequency over Bias Voltage graph](image)

**Output Return Loss vs. Frequency over Temperature**

![Output Return Loss vs. Frequency over Temperature graph](image)

**Output Return Loss vs. Frequency over Bias Voltage**

![Output Return Loss vs. Frequency over Bias Voltage graph](image)
Power Amplifier, 4 W
28.5 - 31.0 GHz

Typical Performance Curves

$P_{\text{SAT}}$ vs. Frequency over Temperature

$P_{\text{SAT}}$ vs. Frequency over Bias Voltage

$P_{1\text{dB}}$ vs. Frequency over Temperature

$P_{1\text{dB}}$ vs. Frequency over Bias Voltage
Typical Performance Curves

Output IP3 vs. Frequency over Temperature

Output IP3 vs. Frequency over Bias Voltage

IM3 vs. Frequency over Temperature
$(P_{OUT} = +29 \text{ dBm/Tone})$

IM3 vs. Frequency over Bias Voltage
$(P_{OUT} = +29 \text{ dBm/Tone})$
Power Amplifier, 4 W
28.5 - 31.0 GHz

Typical Performance Curves

P1dB, P_{SAT} vs. Frequency

PAE vs. Frequency

IM3 vs. Output Power per Tone

Output IP3 vs. Output Power per Tone
Typical Performance Curves

Output Power vs. Input Power

PAE vs. Input Power

Drain Current vs. Input Power

Quiescent Drain Current over Temperature

9. Typical performance curves are achieved by using the recommended bonding diagram and PCB layout detail.
Power Amplifier, 4 W
28.5 - 31.0 GHz

MMIC Die Outline

Bond Pad Detail

<table>
<thead>
<tr>
<th>Pad</th>
<th>Size (x)</th>
<th>Size (y)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A, Q</td>
<td>88</td>
<td>112</td>
</tr>
<tr>
<td>B, P</td>
<td>105</td>
<td>96</td>
</tr>
<tr>
<td>C, D, O, N</td>
<td>108</td>
<td>83</td>
</tr>
<tr>
<td>E, M</td>
<td>163</td>
<td>83</td>
</tr>
<tr>
<td>F, L</td>
<td>169</td>
<td>88</td>
</tr>
<tr>
<td>G, K</td>
<td>248</td>
<td>88</td>
</tr>
<tr>
<td>H, J, R, T</td>
<td>89</td>
<td>99</td>
</tr>
<tr>
<td>I, S</td>
<td>89</td>
<td>159</td>
</tr>
</tbody>
</table>

Notes:
1. All units are in µm, unless otherwise noted, with a tolerance of ±5 µm.
2. Die thickness is 50 ±10 µm.
Power Amplifier, 4 W
28.5 - 31.0 GHz

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