10 W Power Amplifier
0.5 - 3 GHz

Features
- Saturated Output Power: 41 dBm
- Linear Gain: 24 dB
- Power Added Efficiency: 30% at $P_{\text{SAT}}$
- $50 \, \Omega$ Input / Output Match
- Ceramic Flange Mount Package
- RoHS* Compliant and 260°C Re-flow Compatible

Description
The MAAP-010168 is a two stage MMIC power amplifier designed for broadband high power applications. It can be used as either a driver or an output stage amplifier. This device is fully matched input and output to $50 \, \Omega$ which eliminates any sensitive external RF tuning components.

The device is packaged in a lead free 10-lead flanged hermetic package for high volume manufacturing.

The MAAP-010168 is fabricated using a fully passivated high reliability pHEMT process. The device provides excellent power added efficiency and gain.

Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAAP-010168-000000</td>
<td>Bulk</td>
</tr>
<tr>
<td>MAAP-010168-001SMB</td>
<td>Sample Board</td>
</tr>
</tbody>
</table>

2. Flange is DC and RF ground.
3. RF Input & RF Output ports have shunt DC paths to ground. No External DC voltage should be applied to the RF ports.

Pin Configuration

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$V_{GG2}$</td>
</tr>
<tr>
<td>2</td>
<td>$V_{GG1}$</td>
</tr>
<tr>
<td>3</td>
<td>RF Input$^3$</td>
</tr>
<tr>
<td>4</td>
<td>$V_{GG1}$</td>
</tr>
<tr>
<td>5</td>
<td>$V_{GG2}$</td>
</tr>
<tr>
<td>6</td>
<td>$V_{DD1}$</td>
</tr>
<tr>
<td>7</td>
<td>$V_{DD2}$</td>
</tr>
<tr>
<td>8</td>
<td>RF Output$^3$</td>
</tr>
<tr>
<td>9</td>
<td>$V_{DD2}$</td>
</tr>
<tr>
<td>10</td>
<td>$V_{DD1}$</td>
</tr>
</tbody>
</table>

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.
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Electrical Specifications:
Freq. = 0.5 - 3.0 GHz, \( V_{DD} = 10 \) V, \( I_{DQ} = 3.5 \) A, \( T_A = 25^\circ C \), \( Z_0 = 50 \) Ω

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Units</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>Small signal</td>
<td>dB</td>
<td>19</td>
<td>24</td>
<td>—</td>
</tr>
<tr>
<td>Input Return Loss</td>
<td>—</td>
<td>dB</td>
<td>—</td>
<td>10</td>
<td>—</td>
</tr>
<tr>
<td>Output Return Loss</td>
<td>—</td>
<td>dB</td>
<td>—</td>
<td>10</td>
<td>—</td>
</tr>
<tr>
<td>P1dB</td>
<td>—</td>
<td>dBm</td>
<td>—</td>
<td>39</td>
<td>—</td>
</tr>
<tr>
<td>( P_{SAT} )</td>
<td>—</td>
<td>dBm</td>
<td>38</td>
<td>41</td>
<td>—</td>
</tr>
<tr>
<td>Current ( I_{DQ} )</td>
<td>( P_{SAT} )</td>
<td>A</td>
<td>—</td>
<td>3.5</td>
<td>5.5</td>
</tr>
<tr>
<td>PAE</td>
<td>( P_{SAT} )</td>
<td>%</td>
<td>—</td>
<td>30</td>
<td>—</td>
</tr>
<tr>
<td>Gate Bias</td>
<td>—</td>
<td>V</td>
<td>—</td>
<td>-0.7</td>
<td>—</td>
</tr>
<tr>
<td>Duty Cycle</td>
<td>—</td>
<td>%</td>
<td>—</td>
<td>—</td>
<td>100</td>
</tr>
</tbody>
</table>

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Absolute Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Power</td>
<td>24 dBm</td>
</tr>
<tr>
<td>Operating Supply Voltage</td>
<td>+11 V</td>
</tr>
<tr>
<td>Operating Gate Voltage</td>
<td>-2 V</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Channel Temperature</td>
<td>+150°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C to +150°C</td>
</tr>
</tbody>
</table>

4. Exceeding any one or combination of these limits may cause permanent damage to this device.
5. MACOM does not recommend sustained operation near these survivability limits.
6. Operating at nominal conditions with \( T_J \leq 150^\circ C \) will ensure MTTF > 1 x 10⁶ hours.
7. Junction Temperature (\( T_J \)) = \( T_C + \Theta_{JC} * ((V * I) - (P_{OUT} - P_{IN})) \)
   Typical thermal resistance (\( \Theta_{JC} \)) = 2.0°C/W
   a) For \( T_C = 25^\circ C \) @ 1.5 GHz
      \( T_J = +80^\circ C @ +10 \) V, 4 A, \( P_{OUT} = 41 \) dBm, \( P_{IN} = 21 \) dBm
   b) For \( T_C = 85^\circ C \) @ 1.5 GHz
      \( T_J = +138^\circ C @ +10 \) V, 3.9 A, \( P_{OUT} = 41 \) dBm, \( P_{IN} = 21 \) dBm

Operating the MAAP-010168
The MAAP-010168 is static sensitive. Please handle with care. To operate the device, follow these steps. Ramp down or shutdown in reverse order (gate bias on first and off last). All \( V_{GG} \) pins should have the same voltage applied at all times.
1. Apply \( V_{GG} \) (-1.5 V).
2. Apply \( V_{DD} \) (10.0 V Typical).
3. Set \( I_{DQ} \) by adjusting \( V_{GG} \).
4. Apply RF\(_{IN}\).

Handling Procedures
Please observe the following precautions to avoid damage:

Static Sensitivity
Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.
Recommended Bias Configuration

Sample Board Layout
MAAP-010168 Recommended Layout

Below is the recommended layout for the MAAP-010168. For optimal stability MACOM recommends adding bias decoupling capacitors of 10 µF at the entry point of $V_G$ and $V_{DD}$ (At the DC connections Header PIN). It is also recommended to add shunt decoupling capacitors of 1 µF & 1000 pF at the gate and drain pins of MAAP-010168 as shown in the details A below.

MACOM can provide gerber files of the sample board layout upon request.

MAAP-010168 Sample Board Layout

![Board Layout Diagram]

Parts List

<table>
<thead>
<tr>
<th>Item #</th>
<th>Component / Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>Test Board, RO4350, ½ Oz copper, 10 mil thick</td>
</tr>
<tr>
<td>20</td>
<td>SMA Edge Mount Connectors</td>
</tr>
<tr>
<td>30</td>
<td>2x15 Right Angle Connector, 0.1 Grid</td>
</tr>
<tr>
<td>40</td>
<td>Capacitor, 10 µF, 10%, 16 V, 1210, X5R</td>
</tr>
<tr>
<td>50</td>
<td>Capacitor, 1 µF, 10%, 16 V, 0402, X5R</td>
</tr>
<tr>
<td>60</td>
<td>Capacitor, 1000 pF, 10%, 25 V, 0402, X5R</td>
</tr>
</tbody>
</table>
Typical Performance Curves

**Gain**

![Gain Chart]

**Input Return Loss**

![Input Return Loss Chart]

**Output Return Loss**

![Output Return Loss Chart]

**Reverse Isolation**

![Reverse Isolation Chart]

**Output Power (dBm)**

![Output Power (dBm) Chart]

**Output Power (W)**

![Output Power (W) Chart]
Typical Performance Curves

**Power Gain**

![Power Gain Graph](image)

**Power Added Efficiency**

![Power Added Efficiency Graph](image)

**Drain Current**

![Drain Current Graph](image)

**Output Power Sweep @ 0.7 GHz**

![Output Power Sweep @ 0.7 GHz Graph](image)

**Output Power Sweep @ 1.5 GHz**

![Output Power Sweep @ 1.5 GHz Graph](image)

**Output Power Sweep @ 2.5 GHz**

![Output Power Sweep @ 2.5 GHz Graph](image)
Typical Performance Curves

**Power Gain vs. Input Power @ 0.7 GHz**

- **Power Gain vs. Output Power @ 0.7 GHz**
  - Variation with temperature

**Power Gain vs. Input Power @ 1.5 GHz**

- **Power Gain vs. Output Power @ 1.5 GHz**
  - Temperature variation

**Power Gain vs. Input Power @ 2.5 GHz**

- **Power Gain vs. Output Power @ 2.5 GHz**
  - Temperature variation

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Typical Performance Curves

**Max. Power Dissipation vs. Base Plate Temperature**

- Power dissipation should not exceed the maximum plot shown above to maintain $T_J < 150^\circ C$. It is recommended to monitor power dissipation and decrease power dissipation in the device as required.

**Junction Temperature vs. Base Plate Temperature with 50 W Power Dissipation**

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**Ceramic Flange Mount Package**

- This is a high frequency, low thermal resistance package. The package consists of a cofired ceramic construction with a copper-tungsten base and iron-nickel-cobalt leads. The finish consists of electrolytic gold over nickel plate.

† Reference Application Note M538 for lead-free solder reflow recommendations.

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