

Features

- Saturated Output Power: 30.5 dBm Typical
- Gain: 20 dB Typical
- Power Added Efficiency: 30% Typical
- On-Chip Bias Network
- DC Decoupled RF Input and Output
- Lead-Free High Performance Ceramic Package
- RoHS* Compliant and 260°C Reflow Compatible

Description

The MAAM26100-P1 is a GaAs MMIC two stage high efficiency power amplifier in a lead-free high performance bolt down ceramic package. The MAAM26100-P1 is a fully monolithic design which eliminates the need for external circuitry in 50-ohm systems.

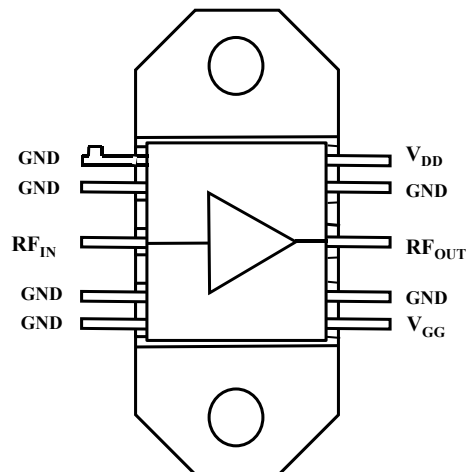
The MAAM26100-P1 is ideally suited for driver amplifiers and transmitter outputs in UMTS applications, test equipment, electronic warfare jammers, missile subsystems and phased array radars.

The MAAM26100-P1 is fabricated using a mature 0.5-micron gate length GaAs process. The process features full passivation for increased performance reliability.

Ordering Information

| Part Number | Package |
|--------------|-------------------|
| MAAM26100-P1 | Ceramic Bolt Down |

Functional Diagram



Pin Configuration

| Pin No. | Function | Pin No. | Function |
|---------|------------------|---------|-------------------|
| 1 | GND | 6 | V _{DD} |
| 2 | GND | 7 | GND |
| 3 | RF _{IN} | 8 | RF _{OUT} |
| 4 | GND | 9 | GND |
| 5 | GND | 10 | V _{GG} |

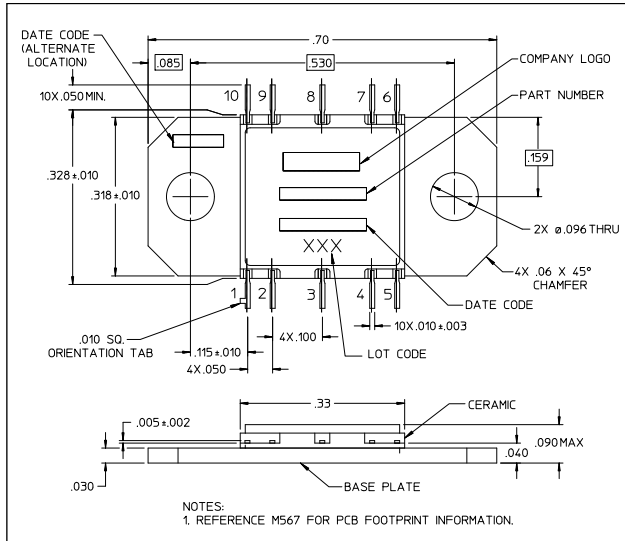
Absolute Maximum Ratings ^{1,2}

| Parameter | Absolute Maximum |
|--------------------------------------|------------------|
| V _{DD} | +9 V |
| V _{GG} | -6 V to -3 V |
| RF Input Power | +17 dBm |
| Channel Temperature | 150°C |
| Storage Temperature | -65°C to +150°C |
| Thermal Resistance (Channel to Case) | 15°C/W |

1. Exceeding any one or combination of these limits may cause permanent damage to this device and will void product warranty.
2. M/A-COM does not recommend sustained operation near these survivability limits.

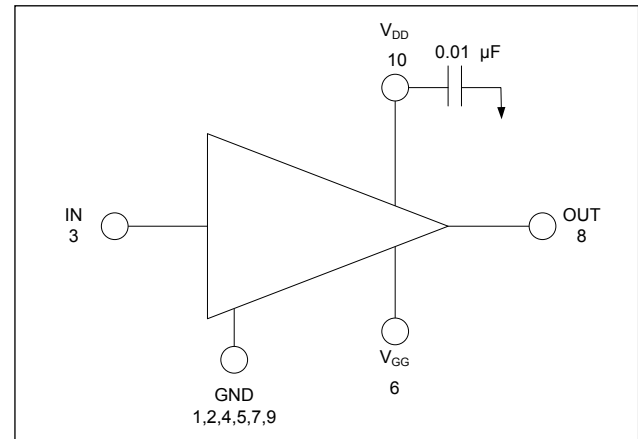
* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

Lead-Free CR-15[†]



[†] Reference Application Note M538 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.

Functional Schematic^{3,4}



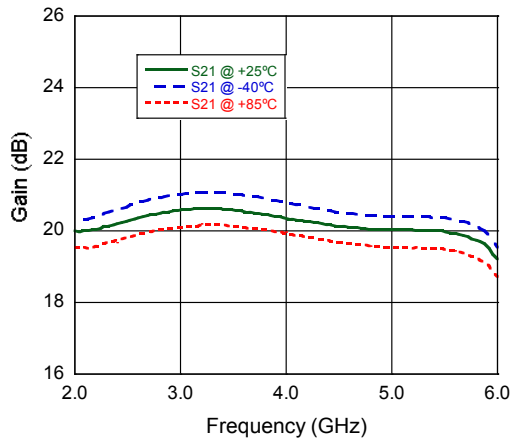
- Nominal bias is obtained by first connecting -5 volts to pin 6 (V_{GG}), followed by connecting $+8$ volts to pin 10 (V_{DD}). Note sequence.
- RF ground and thermal interface is the flange (case bottom). Adequate heat sinking is required.

Electrical Specifications: $T_A = 25^\circ\text{C}$, $V_{DD} = +8\text{ V}$, $V_{GG} = -5\text{ V}$

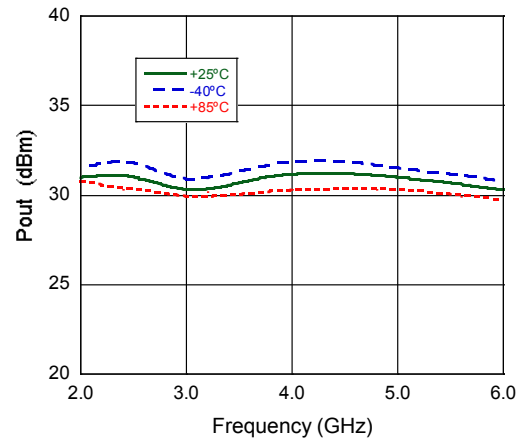
| Parameter | Test Conditions | Units | Min. | Typ. | Max. |
|------------------------|-----------------------------|-------|------|-------|-------|
| Small Signal Gain | Pin ≤ -10 dBm, 2-6 GHz | dB | — | 20 | — |
| Input VSWR | Pin ≤ -10 dBm, 2-6 GHz | Ratio | — | 1.8:1 | 2.1:1 |
| Output VSWR | Pin ≤ -10 dBm, 2-6 GHz | Ratio | — | 2.2:1 | — |
| Output Power | Pin = $+14$ dBm, 2-6 GHz | dBm | 29 | 30.5 | — |
| P1dB | 2-6 GHz | dBm | — | 28 | — |
| Power Added Efficiency | Pin = $+14$ dBm, 2-6 GHz | % | — | 30 | — |
| Output IP3 | 2-6 GHz | dBm | — | 40 | — |
| IDS | Pin = $+14$ dBm, 2-6 GHz | mA | — | 475 | 650 |

Typical Performance Curves

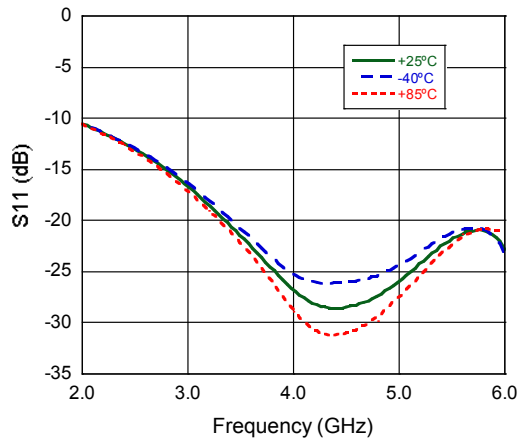
Gain



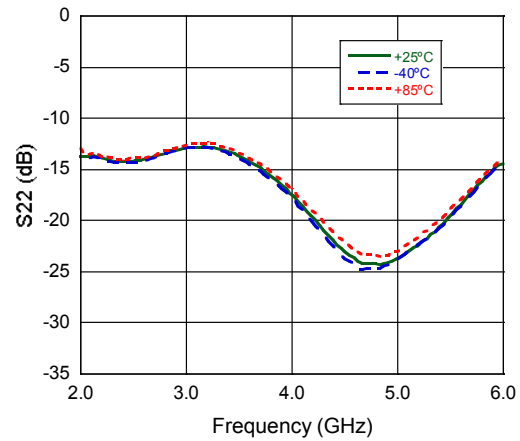
Pout



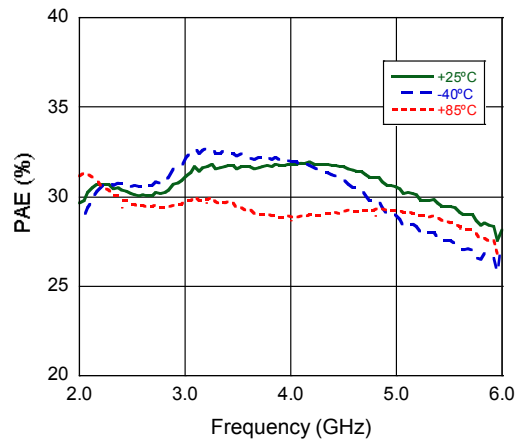
Input Return Loss



Output Return Loss



Power Added Efficiency



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