High Gain Broadband 27.5 dBm Driver Amplifier 1.4 - 2.5 GHz

MAAM-011395
Rev. V2

Features

- 2-Stage Driver Amplifier with bias control circuit
- 1.4 - 2.5 GHz wideband operation frequency
- Differential RF Input
- No external matching components required
- Gain: 37.5 dB
- OP1dB: 27.5 dBm
- OP3dB: 29.5 dBm
- Output IP3: 37 dBm
- Noise figure: 4 dB
- Single supply voltage: 5 V
- Supply current adjustable with an external resistor
- Standby logic voltage: 1.8 or 3.3 V
- Lead-Free 3 mm 16 Lead QFN package
- RoHS* compliant

Applications

- 5G Macro, Massive MIMO, and Small Cell
- Wireless Infrastructure
- Multi Market
- TDD or FDD Systems
- D2D and D2C
- L and S Band Satellite Applications

Description

The MAAM-011395 is a wideband high gain, high efficiency driver amplifier packaged in a compact 3 mm16-Lead QFN package. This driver amplifier provides 37.5 dB gain, 27.5 dBm OP1dB, and 37 dBm OIP3 with 180 mA quiescent current and device ON/OFF function to support TDD system application. RF differential inputs and output ports are internally matched at the entire operating frequency range of 1.4 - 2.5 GHz.

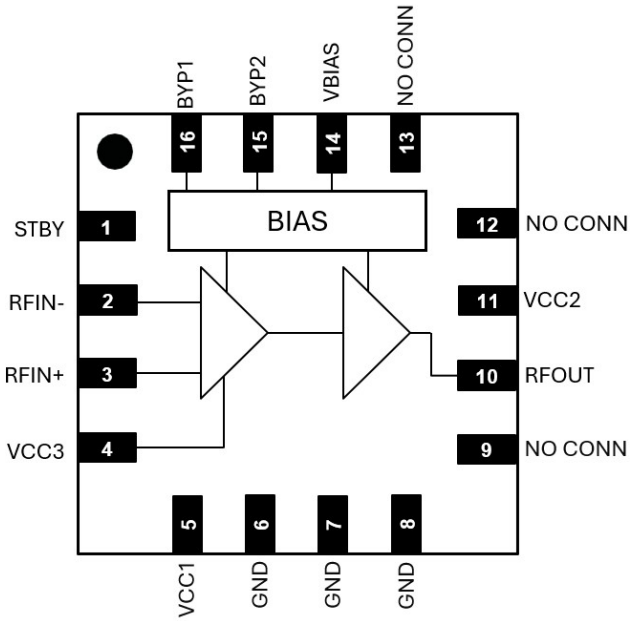
This driver amplifier has low memory effects, operates 100 MHz above and below its band edges and features a smooth AM/AM and AM/PM characteristic across frequency, making it ideal for memoryless digital predistortion (DPD) applications.

Ordering Information[1]

Part Number	Package
MAAM-011395-TR1000	1000 piece reel
MAAM-011395-002SMB	Sample Board

1. Reference Application Note M513 for reel size information.

Functional Schematic



Pin Function

Pin #	Pin Function
1	Standby
2, 3	Differential RF Inputs
4, 5, 11	5V DC Supply Voltage
6, 7, 8	Ground
9, 12, 13	Internal Connection[2]
10	RF Output
14	Bias Voltage to Adjust Current
15, 16	Bias Bypass
17[3]	Ground Paddle

2. Pins 9, 12, and 13 must be left unconnected.
3. The exposed pad centered on the package bottom must be connected to PCB ground with low electrical and thermal resistances.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Pin Description

Pin #	Name	Description
1	STBY	Amplifier ON/OFF logic control voltage. A logic high (1.17 to 3.6 V) turns on the amplifier; a logic low (0 to 0.63 V) turns off the amplifier.
2	RFIN-	Differential RF input 1, dc blocked, 100 ohms differential.
3	RFIN+	Differential RF input 2, dc blocked, 100 ohms differential.
4	VCC3	DC supply voltage for bias circuits. It must be externally decoupled with a 100 nF, 10 V capacitor located approximately 1 mm from the package edge.
5	VCC1	DC supply voltage for stage 1. It must be externally decoupled with a 100 nF, 10 V capacitor located at 1 mm from the package edge; this distance is critical, for which it is recommended to follow the provided evaluation board layout.
6, 7	GND	Ground connection; pins must be grounded. Internally connected to a center ground paddle.
8	GND	Ground connection; recommend to be grounded. Not connected internally (floating pin).
9, 12, 13	NO CONN	These pins have internal connection; pins must be left unconnected. The application board must use a pad not larger than needed for the pin connection in order not to negatively affect the internal connection.
10	RFOUT	Single ended RF out, 50 ohms. External dc blocking capacitor is required.
11	VCC2	DC supply voltage for stage 2. It must be externally decoupled with a 100 nF, 10 V capacitor located at 0.5 mm from the package edge; this distance is critical, for which it is recommended to follow the provided evaluation board layout.
14	VBIAS	Bias voltage to adjust 2nd stage idle current. It must be connected to a stable 5 V dc supply reference through a resistor. The temperature coefficient of this resistor and the supply voltage will affect the bias current of the 2nd stage accordingly. See “Application Notes” and Table I for more details on how to calculate the value of this resistor.
15, 16	BYP1, BYP2	Bias voltage bypass. It must be externally decoupled with a 4.7 nF, 10 V capacitor located approximately 1 mm from the package edge. These capacitors are used to provide a low impedance termination to the envelope frequencies of the modulated signal applied to the input of the amplifier.
17	Paddle	Must be connected to RF, DC, and thermal ground; this pin is grounded internally.

AC Electrical Specifications:

Freq = 2.2 GHz, T_A = 25°C, VCC1 = VCC2 = VCC3 = VBIAS = 5 V,
Z_{IN} = 100 Ω Differential, Z_{OUT} = 50 Ω Single Ended

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	P_{IN} = -30 dBm	dB	35	37.5	—
Gain Flatness	Any 300 MHz	dB	—	0.5	—
Output P1dB	—	dBm	—	27.5	—
Output P3dB	—	dBm	—	29.5	—
Output IP3	50 MHz Tone Spacing, P_{OUT} = 12 dBm/Tone	dBm	—	37	—
Input Return Loss	P_{IN} = -30 dBm	dB	—	10	—
Output Return Loss	—	dB	—	12.5	—
Noise Figure	—	dB	—	4	—
Standby to Active Mode Settling Time	RFIN to RFOUT gain settled within 0.1 dB of final value after STBY command	ns	—	300	—
Active to Standby Mode Settling Time	RFIN to RFOUT signal reduced at least 30 dB after STBY command	ns	—	300	—

DC Electrical Specifications:

T_A = 25°C, VCC1 = VCC2 = VCC3 = VBIAS = 5 V

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Supply Voltage	VCC1, VCC2, VCC3	V	4.75	5.0	5.25
Supply Current	Sum of VCC1, VCC2, VCC3	mA	—	180[4]	—
Logic Control Voltage	Logic High, STBY Logic Low, STBY	V	1.17 0	—	3.60 0.63
Logic input Current	Logic High (1.8 V) / High (3.3 V), STBY	µA	—	110 / 440	—
	Logic Low (0 V), STBY	µA	—	-280	—
Power Consumption (STBY=high)	No input power applied	W	—	0.9	—
Power Consumption (STBY=low)	Power Down Mode	W	—	0.03	—

4. Adjusted VBIAS (pin-14) voltage through an external resistor of 240 Ω connected to a stable 5 V dc supply.

Control Truth Table

Device state	STBY pin
ON	Logic High
OFF	Logic Low

Recommended Operating Conditions

Parameter	Symbol	Unit	Min.	Typ.	Max.
DC Power Supply	VCC1, VCC2, VCC3, VBIAS	V	4.75	5.0	5.25
Operating Temperature[5]	T_c	°C	-40	—	125
Junction Temperature[6,7]	T_J	°C	—	—	150

5. Tc is defined by exposed paddle temperature.
6. Operating at nominal conditions with $T_J \leq +150$ °C will ensure MTTF > 1 x 10^6 hours.
7. Junction Temperature (TJ) = TC + ΘJC * P_{DISS} where P_{DISS} is the total DC & RF dissipated power.
   Typical thermal resistance (ΘJC) = 28 ºC/W.
   a) For T_C = +25°C, T_J = 50 °C @ 5 V, 0.9 W.
   b) For T_C = +125°C, T_J = 150 °C @ 5 V, 0.9 W.

Absolute Maximum Ratings[8,9]

Parameter	Symbol	Unit	Min.	Max.
Input Power	RFIN	dBm	—	10
DC Supply Voltage	VCC1, VCC2, VCC3, VBIAS	V	-0.5	6.0
Logic Control Voltage	STBY	V	-0.5	3.9
Maximum external DC Voltage sustained by DC-blocked pins	RFIN-, RFIN+	V	—	10
Operating Temperature[5]	T_c	°C	-40	125
Storage Temperature	T_c	°C	-65	150

8. Exceeding any one or combination of these limits may cause permanent damage to this device.
9. MACOM does not recommend sustained operation near these survivability limits.

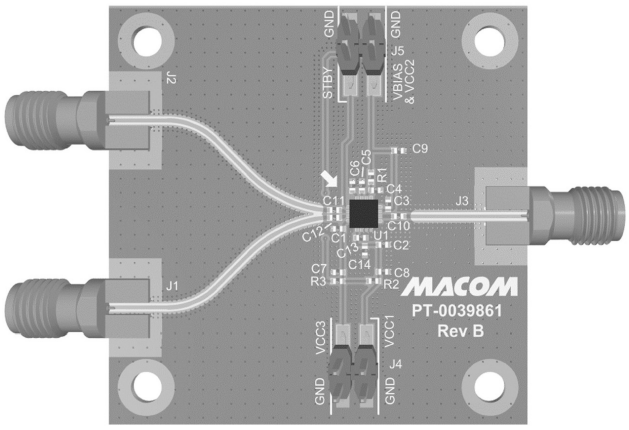
Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1C and CDM Class C3 devices.

PCB Layout



Parts List

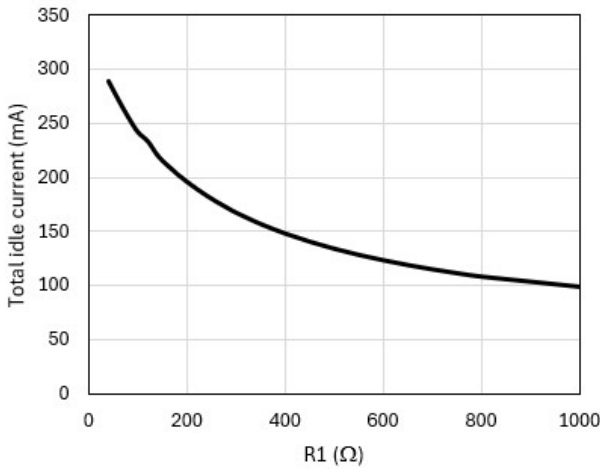
Part	Value	Case Style [inch]
C1 - C4	100 nF	0402
C5 - C6	4.7 nF	0402
C7, C13, C14	NA	NA
C8 - C9	1 µF	0402
C10	18 pF	0402
C11 - C12	0 Ω	0402
R1	240 Ω	0402
R2, R3	0 Ω	0402

Application Notes

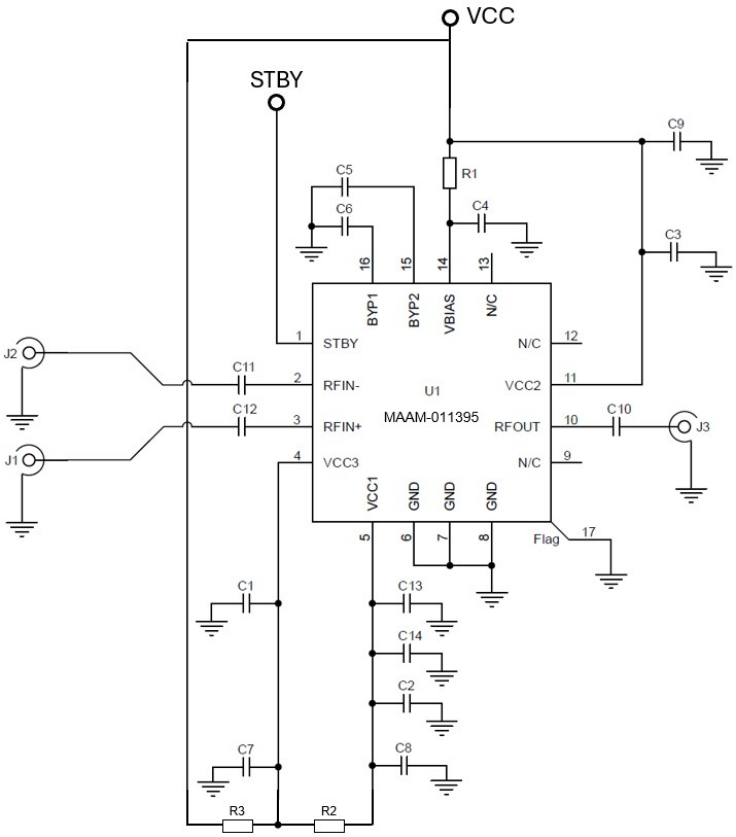
The value of R1 can be adjusted to control the idle current of the second stage to trade off linearity for current consumption. Table I shows the approximate total idle current of the amplifier as a function of R1. The power dissipated by R1 can be up to 2.5 mW.

The variation of the resistance value of R1 as a function of temperature will proportionally affect the idle current over temperature. This also applies to the external voltage applied to this resistor.

Table I. Total idle current versus R1



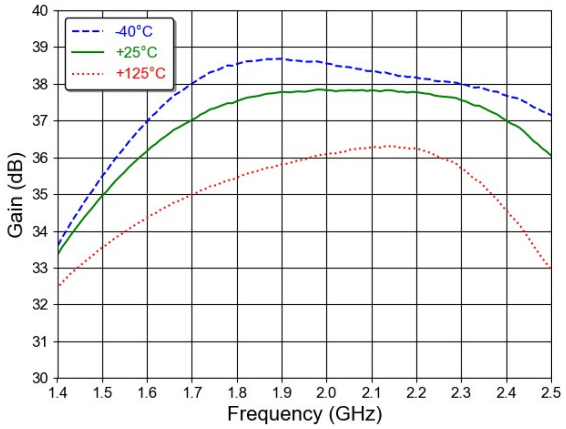
Application Schematic



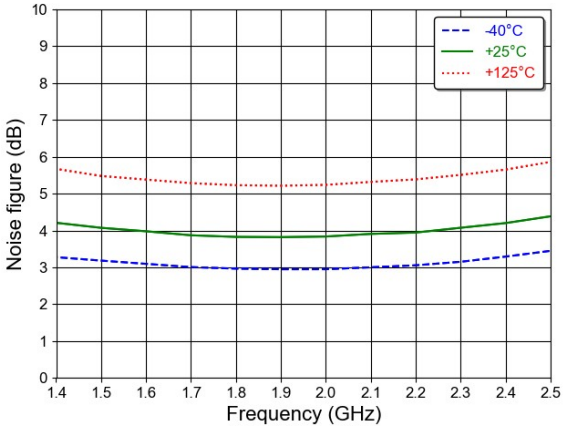
Typical Performance Curves:

P_{IN} = -30 dBm, VCC1 = VCC2 = VCC3 = VBIAS = 5 V, Z_{IN} = 100 Ω Differential, Z_{OUT} = 50 Ω Single Ended, R1 = 240 Ω, C5 = C6 = 4.7 nF

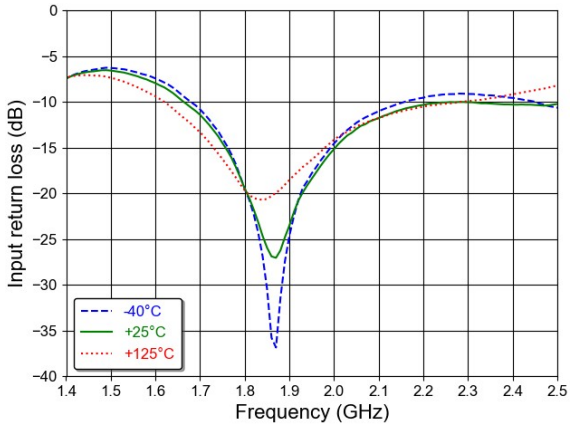
Gain



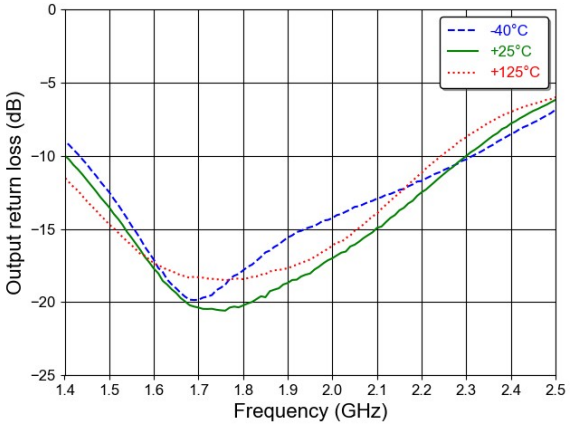
Noise Figure



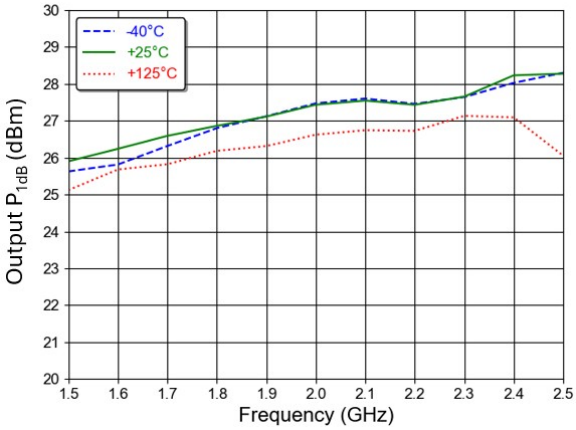
Input return loss



Output return loss



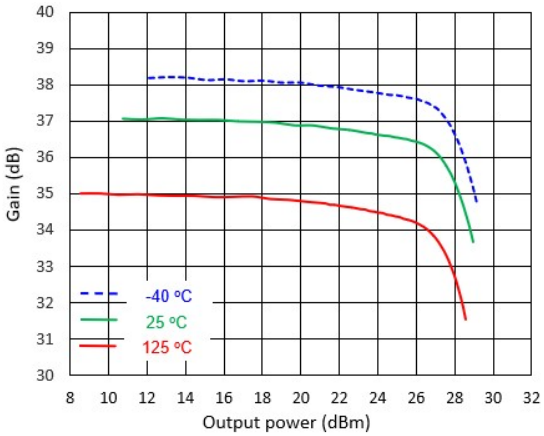
Output P_{1dB}



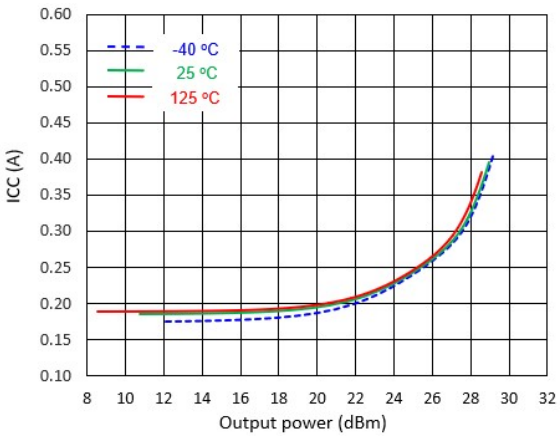
Typical Performance Curves:

VCC1 = VCC2 = VCC3 = VBIAS = 5 V, Z_{IN} = 100 Ω Differential, Z_{OUT} = 50 Ω Single Ended, R1 = 240 Ω, C5 = C6 = 4.7nF

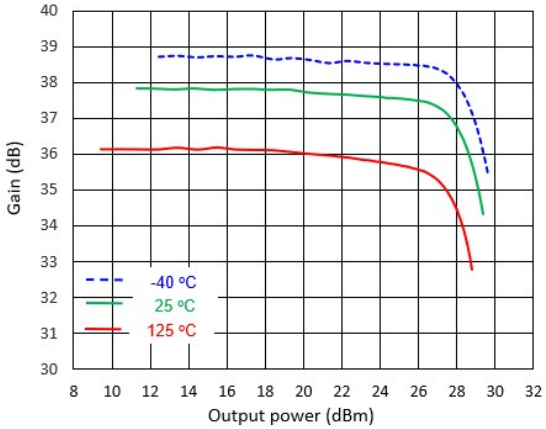
Gain vs. Output power, 1.7 GHz



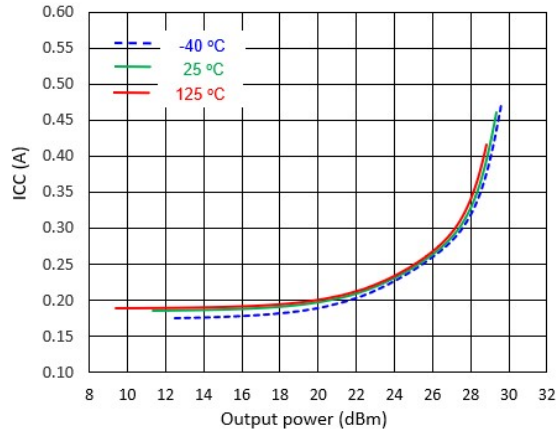
ICC vs. Output power, 1.7 GHz



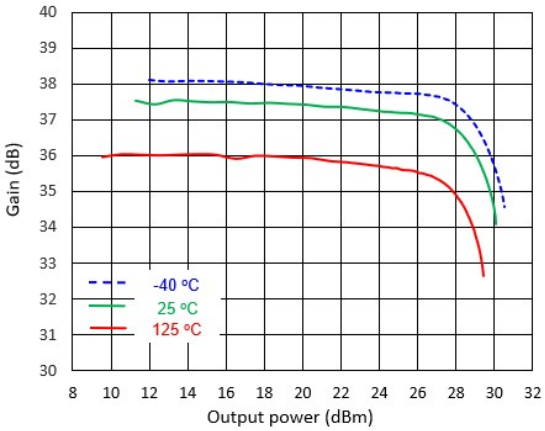
Gain vs. Output power, 2.0 GHz



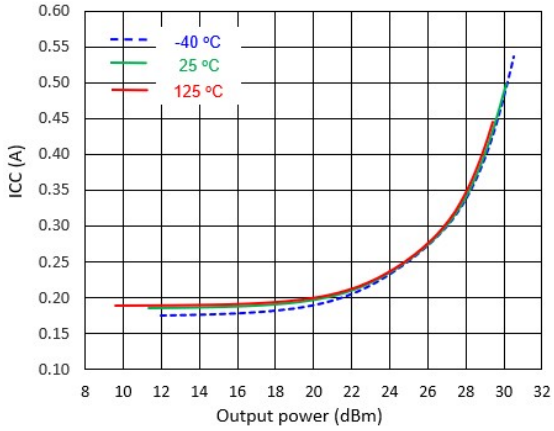
ICC vs. Output power, 2.0 GHz



Gain vs. Output power, 2.3 GHz



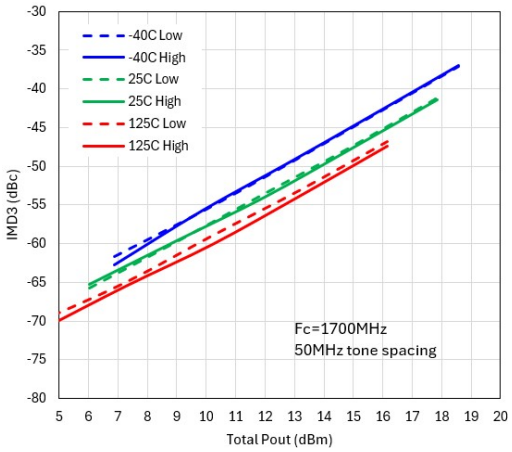
ICC vs. Output power, 2.3 GHz



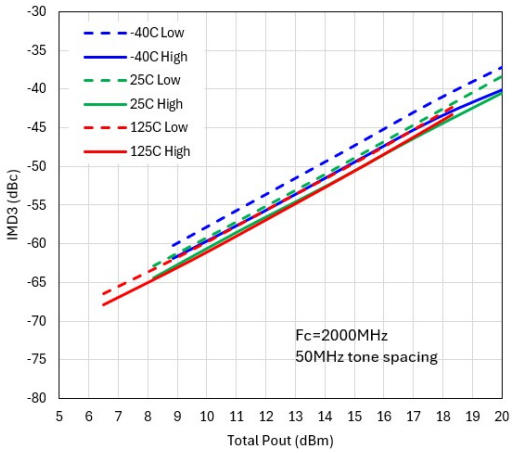
Typical Performance Curves:

VCC1 = VCC2 = VCC3 = VBIAS = 5 V, Z_{IN} = 100 Ω Differential, Z_{OUT} = 50 Ω Single Ended, R1 = 240 Ω, C5 = C6 = 4.7 nF

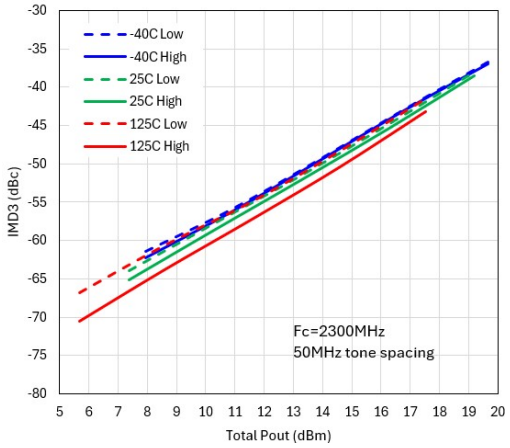
IMD3 vs. Total output power, 1.7 GHz



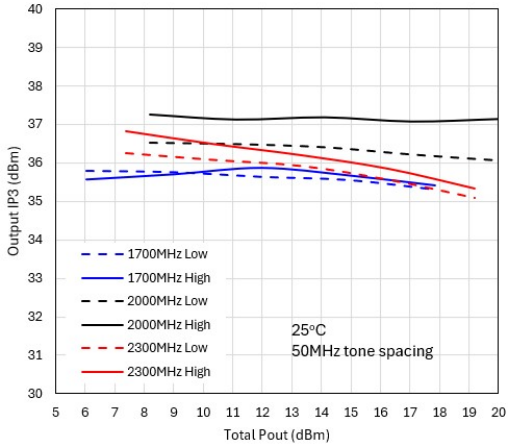
IMD3 vs. Total output power, 2.0 GHz



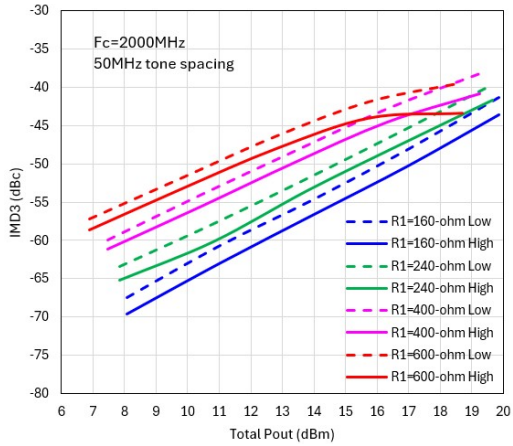
IMD3 vs. Total output power, 2.3 GHz



Output IP3 vs. Total output power, 25 °C

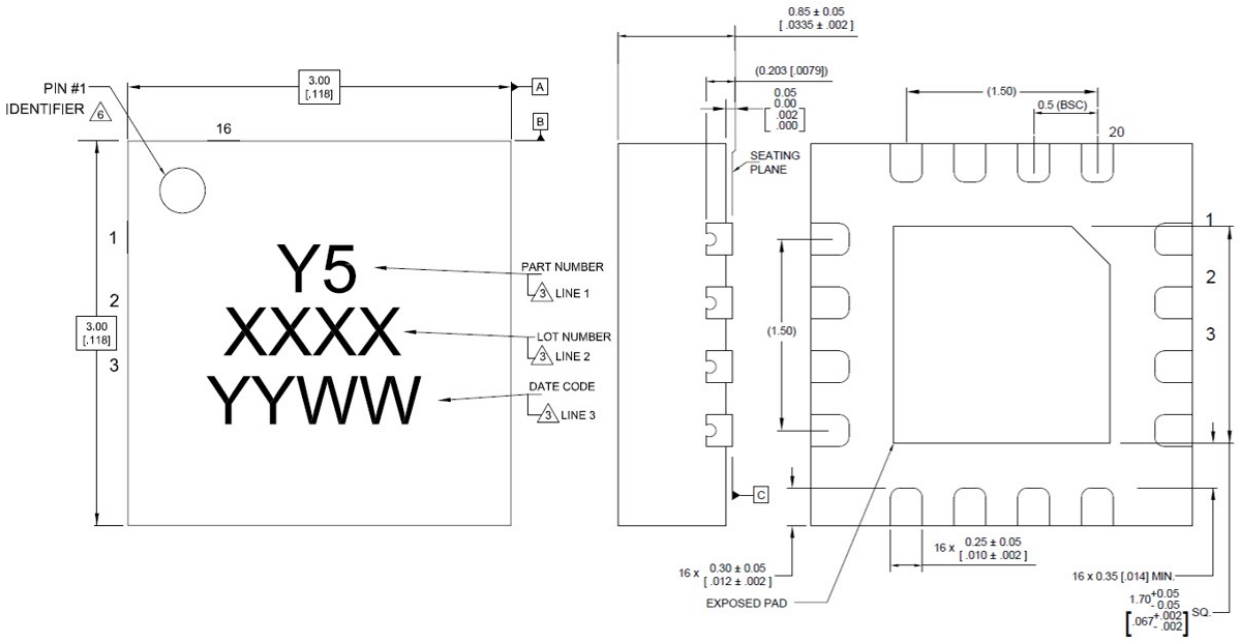


IMD3 vs. Total output power[10], 2.0 GHz, 25 °C



10. Total idle current versus R1 value shows in Table I on p. 5.

Lead-Free 3 mm 16-Lead PQFN†



Notes:
1. Dimensions are in mm [in]
2. Reference JEDEC MO-220 for additional dimensional and tolerance information

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements in accordance to JEDEC J-STD-020D.
Plating is NiPdAu over Copper.

Revision History

Rev	Date	Change Description
V1	9/08/25	Production release
V2	10/15/25	Updated a frequency range and the related graphs. Added a graph about IMD3 versus R1.