Broadband Low Noise Gain Block Amplifier
0.025 - 8 GHz

MAAM-011252-CQ3
Rev. V2

Features

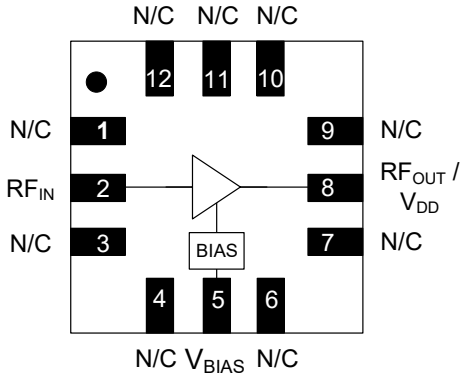
- 19.5 dB Flat Broadband Gain to 8 GHz
- Low Noise Figure:
  - 1.4 dB Noise Figure to 1.5 GHz
  - 1.5 dB Noise Figure @ 6 GHz
  - 2.0 dB Noise Figure @ 8 GHz
- High Linearity OIP3:
  - 34 dBm @ 2.5 GHz
  - 32 dBm @ 6 GHz
  - 22 dBm @ 8 GHz
- Internal Matching to 50 ohm
- Single Voltage Bias: 3 - 5 V
- Integrated Active Bias Circuit
- Current Adjustable 20 - 100 mA
- Lead-Free 3 mm 12-Lead Hermetic Ceramic Package
- RoHS* Compliant

Description

The MAAM-011252-CQ3 is a broadband high dynamic range, single stage MMIC LNA assembled in a lead-free 3 mm 12-Lead hermetic ceramic package. The amplifier is internally matched to provide flat gain and good return losses to 8 GHz without any external matching components.

This low noise amplifier has an integrated active bias circuit allowing direct connection to 3 V or 5 V bias and minimizing variations over temperature and process. The bias current can be set by an optional external resistor, so the user can customize the power consumption to fit the application. V_{BIAS} can be utilized as an enable pin to power the device up and down during operation.

Functional Block Diagram



Pin Configuration[1,2]

Pin #	Pin Name	Description
1, 3, 4, 6, 7, 9 - 12	N/C	No Connection
2	RF_{IN}	RF Input
5	V_{BIAS}	Bias Voltage
8	RF_{OUT} / V_{DD}	RF Output / Drain Voltage

1. MACOM recommends connecting all No Connection (N/C) pins to ground.
2. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

Ordering Information

Part Number	Package
MAAM-011252-CQ3	Bulk
MAAM-011252-CQS	Sample Board

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications: V_{DD} = 5 V, +25ºC, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	0.03 - 8 GHz	dB	17	19.5	—
Noise Figure	0.1 - 1.5 GHz 6.0 GHz 8.0 GHz	dB	—	1.4 1.5 2.0	1.8 2.3 —
Input Return Loss	0.03 - 8 GHz	dB	—	12	—
Output Return Loss	0.03 - 8 GHz	dB	—	12	—
Output IP3	P_{IN} = -15 dBm per tone, 6 MHz spacing 0.03 - 2.5 GHz 6 GHz 8 GHz	dBm	—	34 32 22	—
Output IP2	P_{IN} = -15 dBm per tone, 6 MHz spacing 0.03 - 3 GHz 6 GHz 8 GHz	dBm	—	42 46 42	—
Output P1dB	0.03 - 3 GHz 6 GHz 8 GHz	dBm	—	20 17 11	—
Current	I_{DD}	mA	—	65	75

Recommended Operating Conditions

Parameter	Maximum
RF Input Power CW	10 dBm
V_{DD}	6 V
I_{DQ}	100 mA
Operating Temperature	-40ºC to +85ºC
Junction Temperature[3,4]	+150ºC

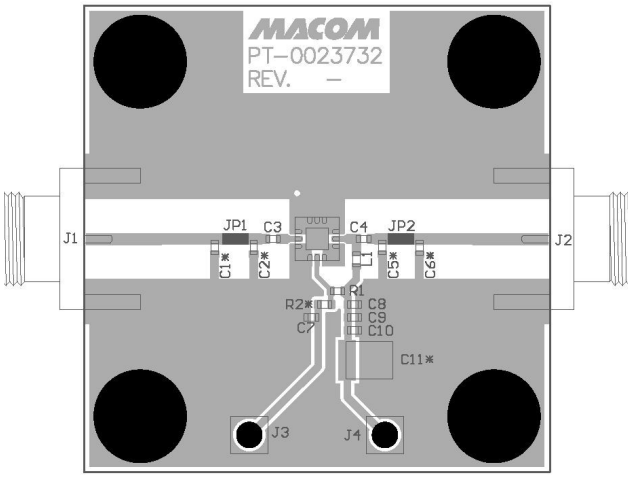
3. Operating at nominal conditions with $T_J \leq 150°C$ will ensure MTTF > 1 x 10^6 hours.
4. Junction Temperature (T_J) = $T_C + \Theta_{JC} * ((V * I) - (P_{OUT} - P_{IN}))$
   Typical thermal resistance (Θ_{JC}) = 43°C/W

Absolute Maximum Ratings[5,6]

Parameter	Absolute Maximum
RF Input Power CW	22.5 dBm
V_{DD}	7 V
Storage Temperature	-55ºC to +150ºC

5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. MACOM does not recommend sustained operation near these survivability limits.

Sample Board

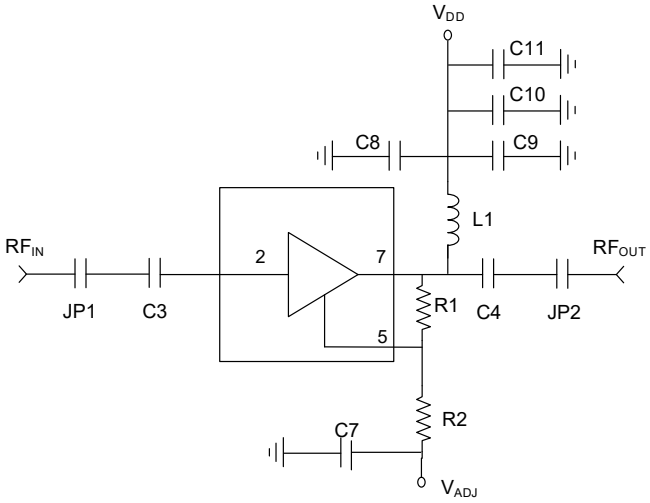


Sample Board Parts List[7]

Component	Value	Package
C1, C2, C5, C6, C7, C11	DNP[9]	—
C3, C4, C9	1000 pF	0402
C8	47 pF	0402
C10	0.1 µF	0402
JP1, JP2	0 Ω	0402
R1, R2	DNP[9]	0402
L1	Ferrite Bead[8]	0402

7. Typical application.
8. Murata, part number BLM15HD182SN.
9. Do not populate.

Sample Board Schematic



Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

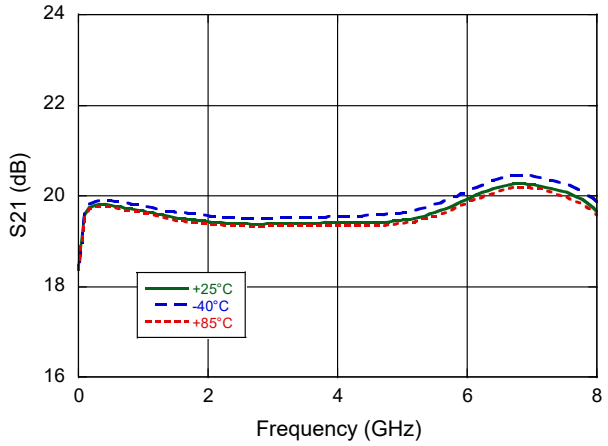
Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Pin Description

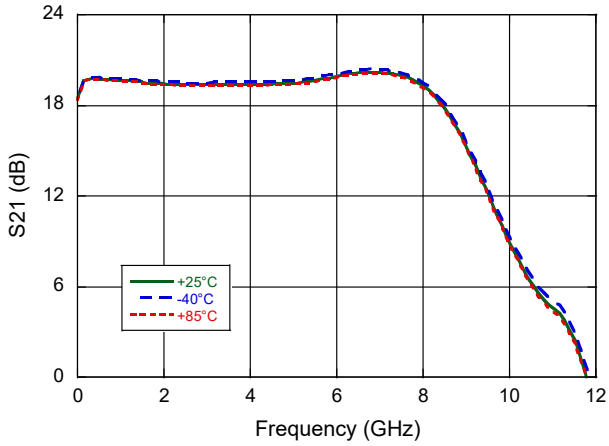
Pin #	Pin Name	Description
1,3,4,6,7,9	N/C	No internal connection. Grounding this pin on the board is recommended to maximize isolation.
2	RF_{IN}	RF Input, an external DC block is required
5	V_{BIAS}	Optional Bias Voltage may be applied to adjust current. If the typical bias current is desired, leave this pin open.
8	RF_{OUT} / V_{DD}	RF Output / Drain Voltage, external bias tee required (see next page)
	Paddle	Ground with as many board vias as practical, stating at the perimeter of the paddle

Typical Performance Curves @ 5 V / 65 mA, Z_0 = 50 Ω

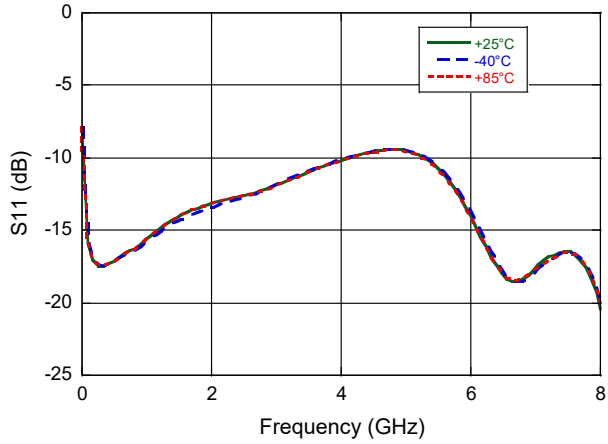
Gain



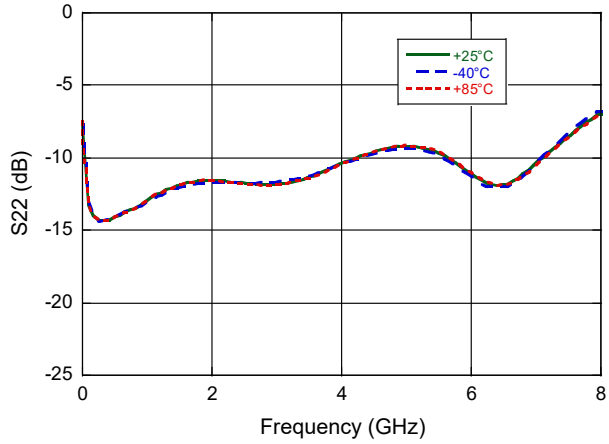
Gain to 12 GHz



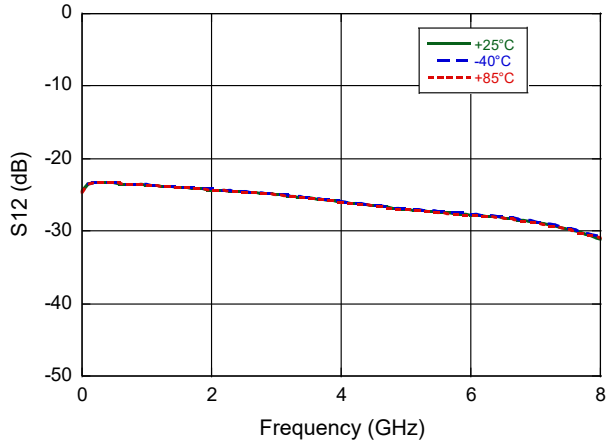
Input Return Loss



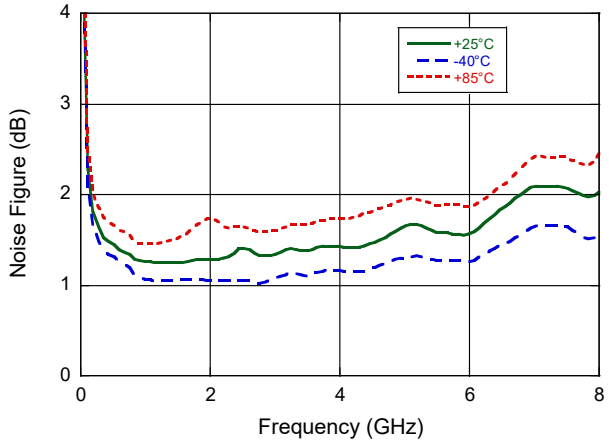
Output Return Loss



Reverse Isolation

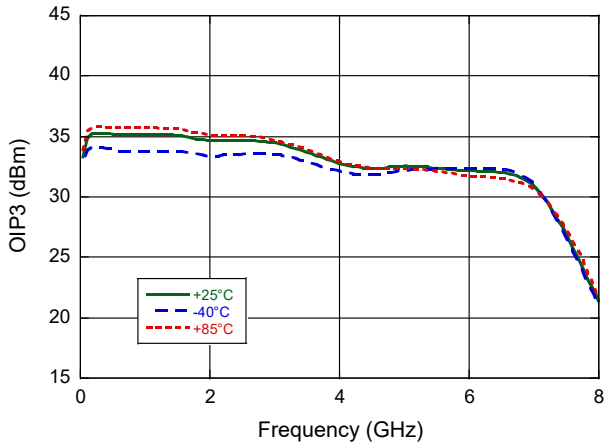


Noise Figure

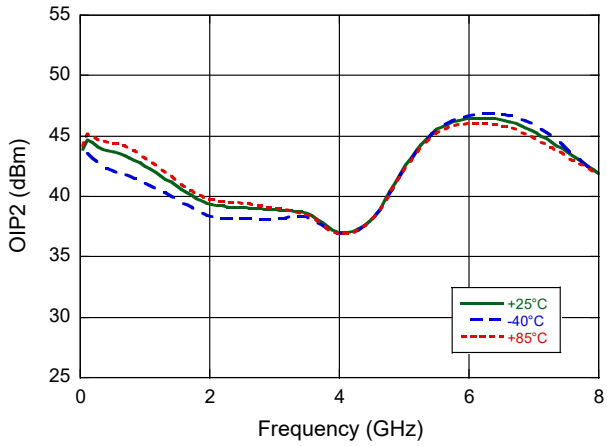


Typical Performance Curves @ 5 V / 65 mA, Z_0 = 50 Ω

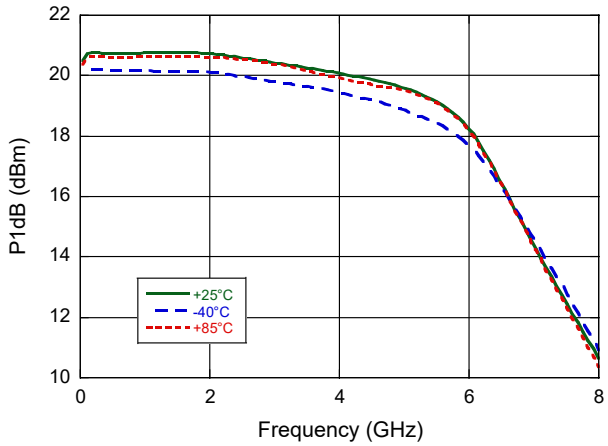
OIP3 @ P_{IN} = -15 dBm/tone, 6 MHz Spacing



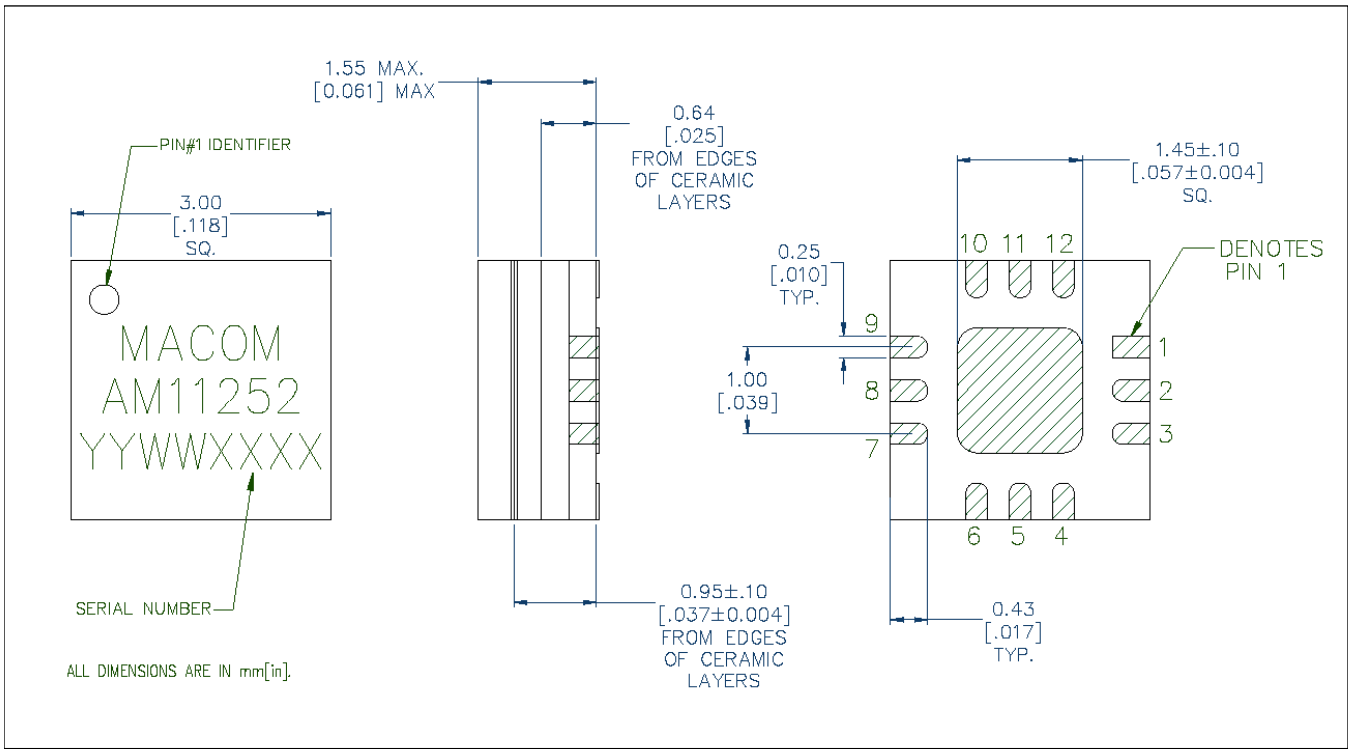
OIP2 @ P_{IN} = -15 dBm/tone, 6 MHz Spacing



Output P1dB



Lead-Free 3 mm 12-Lead Ceramic Package†



† Plating is ENEPIG
Reference Application Note S2083 for surface mount instructions